TP65H150LSG

650V GaN FET PQFN Series

Preliminary

Description

The TP65H150LSG 650V, 150mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

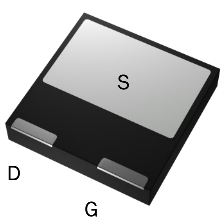
Related Literature

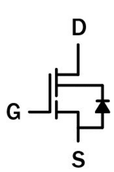
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs

Ordering Information

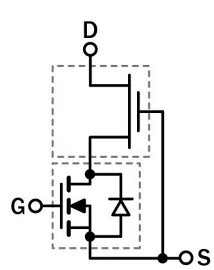
Part Number	Package	Package Configuration
TP65H150LSG	8 x 8mm PQFN	Source

TP65H150LSG
8x8 PQFN
(bottom view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Improves efficiency/operation frequencies over Si
- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DSS} (V)	650
$V_{(TR)DSS}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	180
Q_{RR} (nC) typ	47
Q_G (nC) typ	10

* Dynamic on-resistance; see Figures 5 and 6

Absolute Maximum Ratings (T_C=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		78	W
I_D	Continuous drain current @T_C=25°C [b]		16	A
	Continuous drain current @T_C=100°C [b]		10	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		60	A
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [c]		1000	A/µs
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]		1800	A/µs
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [e]		260	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <1µs

b. For increased stability at high current operation, see Circuit Implementation on page 3

c. Continuous switching operation

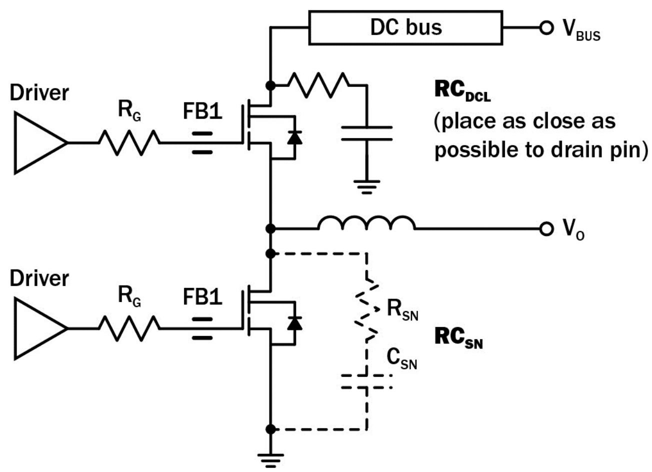
d. ≤300 pulses per second for a total duration ≤20 minutes

e. For 10 sec., 1.6mm from the case

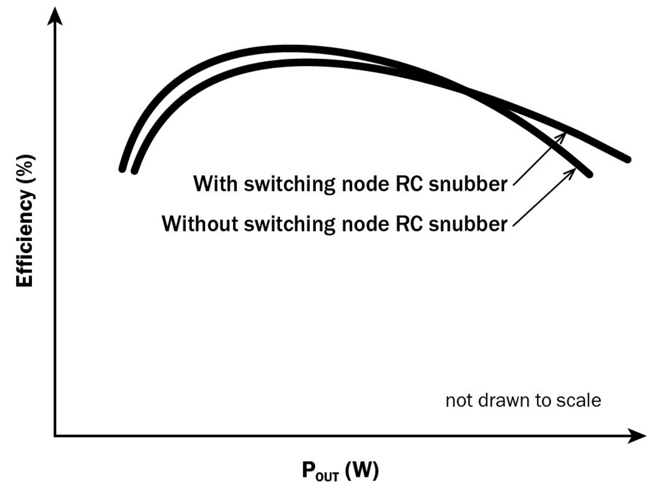
Thermal Resistance

Symbol	Parameter	Maximum	Unit
$R_{\Theta JC}$	Junction-to-case	1.6	°C/W
$R_{\Theta JA}$	Junction-to-ambient [f]	62	°C/W

Circuit Implementation



Simplified Half-bridge Schematic



Efficiency vs Output Power

Recommended gate drive: (0V, 12V) with $R_{G(tot)}$ = 60-70Ω, where $R_{G(tot)} = R_G + R_{DRIVER}$

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [a]	Recommended Switching Node RC Snubber (RC_{SN}) [b, c]
MMZ1608Q121BTA00	{4.7nF + 5Ω} x 2	22pF + 15Ω

Notes:

a. RC_{DCL} should be placed as close as possible to the drain pin

b. A switching node RC snubber (C, R) is recommended for high switching currents (>70% of I_{RDMC1} or I_{RDMC2}; see page 5 for I_{RDMC1} and I_{RDMC2})

c. I_{RDM} values can be increased by increasing R_G and C_{SN}

Electrical Parameter (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS}=V_{GS}, I_D=0.5mA
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	150	180	mΩ	V_{GS}=10V, I_D=10A, T_J=25°C
		—	307	—		V_{GS}=10V, I_D=10A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	2	20	μA	V_{DS}=650V, V_{GS}=0V, T_J=25°C
		—	10	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	600	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	46	—		
C_{RSS}	Reverse transfer capacitance	—	4	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	80	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	120	—		
Q_G	Total gate charge	—	10	—	nC	V_{DS}=400V, V_{GS}=0V to 12V, I_D=10A
Q_{GS}	Gate-source charge	—	3.5	—		
Q_{GD}	Gate-drain charge	—	3	—		
Q_{OSS}	Output charge	—	47	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	TBD	—	ns	V_{DS}=400V, V_{GS}=0V to 12V, I_D=10A, R_G=65Ω
t_R	Rise time	—	TBD	—		
$t_{D(off)}$	Turn-off delay	—	TBD	—		
t_F	Fall time	—	TBD	—		

Notes:
a. Dynamic on-resistance; see Figures 5 and 6 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V
c. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	10	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	1.9	—	V	V_{GS}=0V, I_S=10A
		—	1.4	—		V_{GS}=0V, I_S=5A
t_{RR}	Reverse recovery time	—	TBD	—	ns	I_S=10A, V_{DD}=400V, di/dt=1000A/ms
Q_{RR}	Reverse recovery charge	—	45	—	nC	
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [b]	—	—	1000	A/µs	
I_{RDMC1}	Reverse diode switching current, repetitive (dc) [c, e]	—	—	11	A	Circuit implementation and parameters on page 3
I_{RDMC2}	Reverse diode switching current, repetitive (ac) [c, e]	—	—	15	A	Circuit implementation and parameters on page 3
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]	—	—	1800	A/µs	
I_{RDMT}	Reverse diode switching current, transient [d,e]	—	—	18	A	Circuit implementation and parameters on page 3

Notes:

a. Includes dynamic $R_{DS(on)}$ effect
b. Continuous switching operation
c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
d. ≤300 pulses per second for a total duration ≤20 minutes
e. I_{RDM} values can be increased by increasing R_G and C_{SN} on page 3

Test Circuits and Waveforms

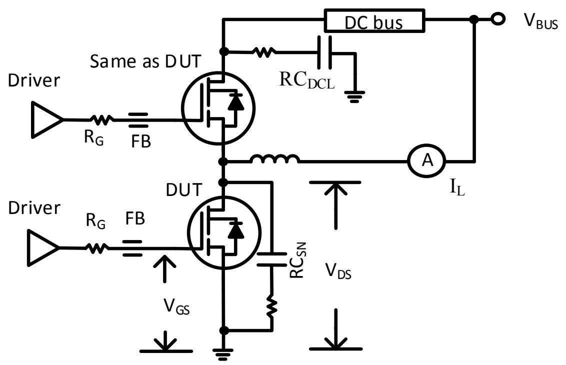


Figure 1. Switching Time Test Circuit
(see circuit implementation on page 3 for methods to ensure clean switching)

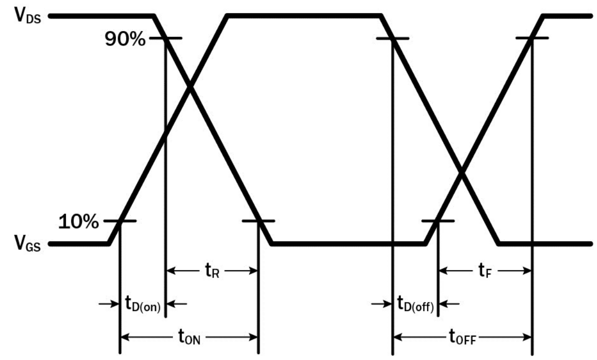


Figure 2. Switching Time Waveform

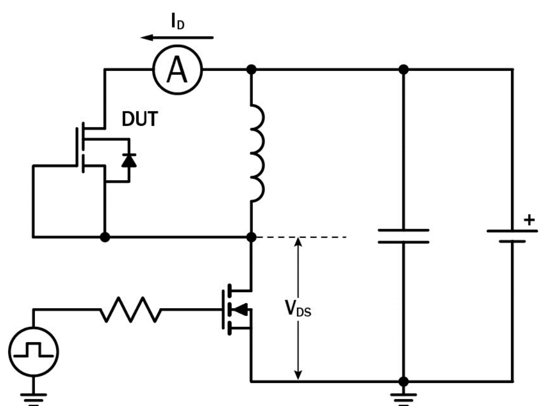


Figure 3. Diode Characteristics Test Circuit

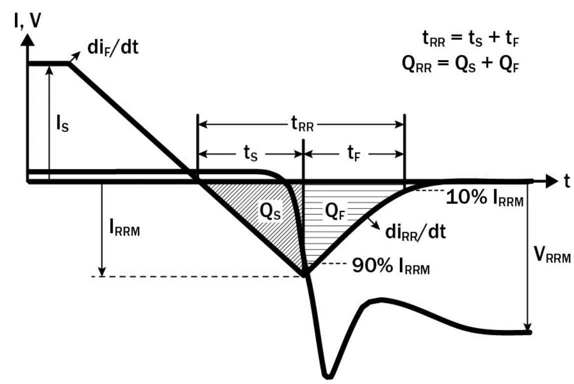


Figure 4. Diode Recovery Waveform

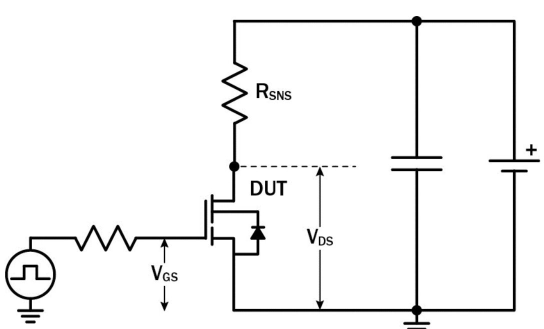
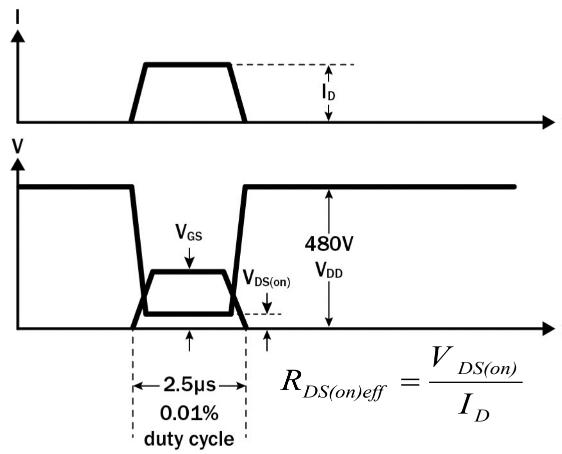


Figure 5. Dynamic $R_{DS(on)eff}$ Test Circuit



$$R_{DS(on)eff} = \frac{V_{DS(on)}}{I_D}$$

Figure 6. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

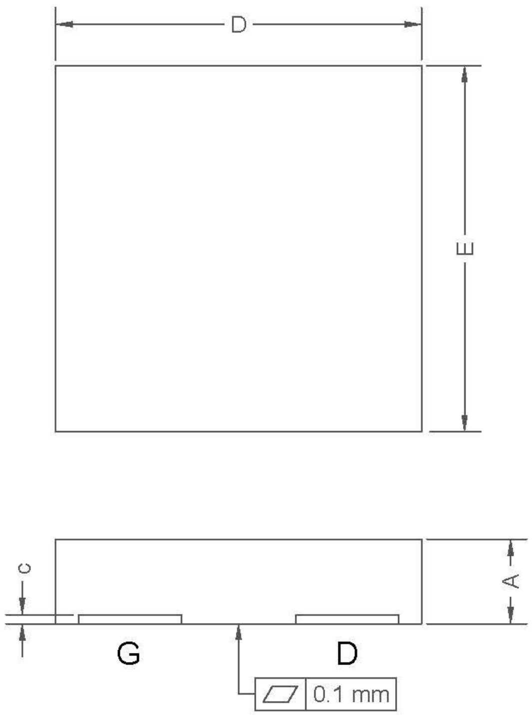
GaN Design Resources

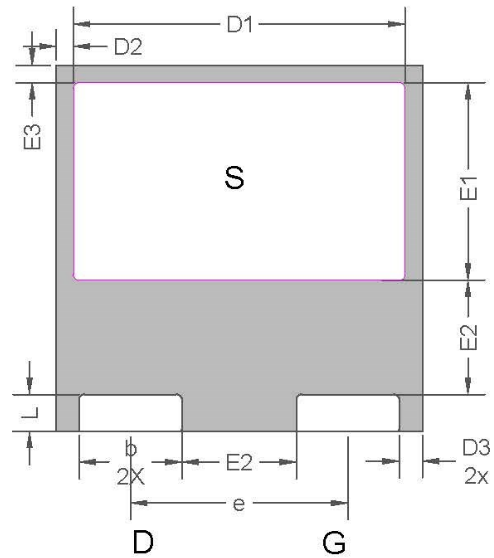
The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

8x8 PQFN (LSG) Package





G: Gate
S: Source
D: Drain
Lead finish: Sn plating

DIM	mm		inch	
	min	max	min	max
A	1.73	1.97	0.068	0.078
b	2.15	2.35	0.085	0.093
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.11	7.37	0.280	0.290
E	7.90	8.10	0.311	0.319
E1	4.18	4.44	0.165	0.175
E2	2.40	2.60	0.094	0.102
E3/D2	0.28	0.48	0.011	0.019
D3	0.45	0.55	0.018	0.022
e	4.75 (BSC)		0.187 (BSC)	
L	0.76	0.86	0.030	0.034

PQFN 8mm x 8mm POD (TPHxxxxLSG)

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Revision History

Version	Date	Change(s)
0	2/14/2019	Preliminary Datasheet