TP65H300G4LSG

650V SuperGaN™ GaN FET in PQFN (source tab)

Preliminary Datasheet

Description

The TP65H300G4WS 650V, 240 mΩ Super Gallium Nitride (SuperGaN™) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

SuperGaN is Transphorm's latest GaN platform, which uses advanced epi and patented design technologies to reduce cost through simplified manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

Related Literature

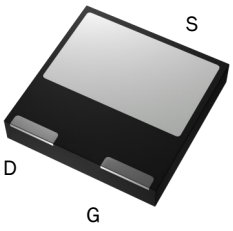
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs

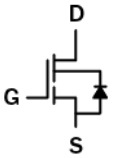
Product Series and Ordering Information

Part Number	Package	Package Configuration
TP65H300G4LSG-TR	8x8mm PQFN	Source

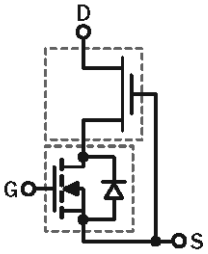
* Add "-TR" suffix for tape and reel

TP65H300G4LSG
PQFN
(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DS} (V) min	650
$V_{(TR)DSS}$ (V) max	720
$R_{DS(on)}$ (mΩ) max*	288
Q_{RR} (nC) typ	23
Q_G (nC) typ	7

* Dynamic $R_{DS(on)}$; see Figures 19 and 20

Absolute Maximum Ratings (T_C=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Transient drain to source voltage [a]		720	
V_{GSS}	Gate to source voltage		±18	
P_D	Maximum power dissipation @T_C=25°C		21	W
I_D	Continuous drain current @T_C=25°C [b]		6.5	A
	Continuous drain current @T_C=100°C [b]		4.1	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		30	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [c]		260	°C

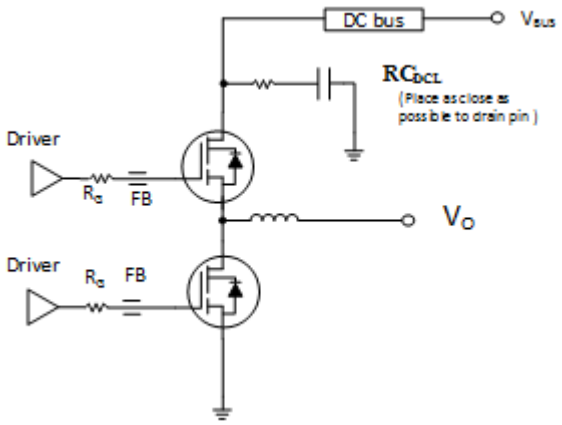
Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <1µs
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Maximum	Unit
$R_{\Theta JC}$	Junction-to-case	6	°C/W
$R_{\Theta JA}$	Junction-to-ambient [e]	50	°C/W

Notes:
e. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70µm thickness)

Circuit Implementation



Simplified Half-bridge Schematic

Recommended gate drive: (0V, 12V) with $R_{G(tot)}$ = 30 Ω[a]

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [b]
240Ω@100MHz	4.7-10nF + 5Ω

Notes:
a. For bridge topologies only. R_G could be much smaller in single ended topologies.
b. RC_{DCL} should be placed as close as possible to the drain pin.

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.5mA
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	240	288	mΩ	V_{GS}=8V, I_D=5A
		—	492	—		V_{GS}=8V, I_D=5A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	1.2	12	μA	V_{DS}=650V, V_{GS}=0V
		—	8	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	760	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	16	—		
C_{RSS}	Reverse transfer capacitance	—	2	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	24	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	47	—		
Q_G	Total gate charge	—	7	—	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A
Q_{GS}	Gate-source charge	—	2.6	—		
Q_{GD}	Gate-drain charge	—	1.3	—		
Q_{OSS}	Output charge	—	19	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	19.4	—	ns	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A,R_G=30Ω,4A driver
t_R	Rise time	—	3.4	—		
$t_{D(off)}$	Turn-off delay	—	53	—		
t_F	Fall time	—	10	—		

Notes:
a. Dynamic $R_{DS(on)}$ value; see Figures 19 and 20 for conditions
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	3.7	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	1.7	—	V	V_{GS}=0V, I_S=5A
		—	1.2	—		V_{GS}=0V, I_S=2A
t_{RR}	Reverse recovery time	—	16	—	ns	I_S=5A, V_{DD}=400V, di/dt=1000A/us
Q_{RR}	Reverse recovery charge	—	23	—	nC	

Notes:
a. Includes dynamic $R_{DS(on)}$ effect

Typical Characteristics (T_C=25 °C unless otherwise stated)

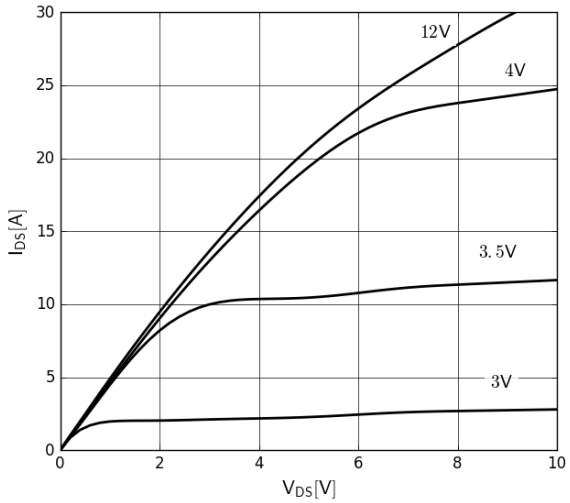


Figure 1. Typical Output Characteristics T_J=25 °C
Parameter: V_{GS}

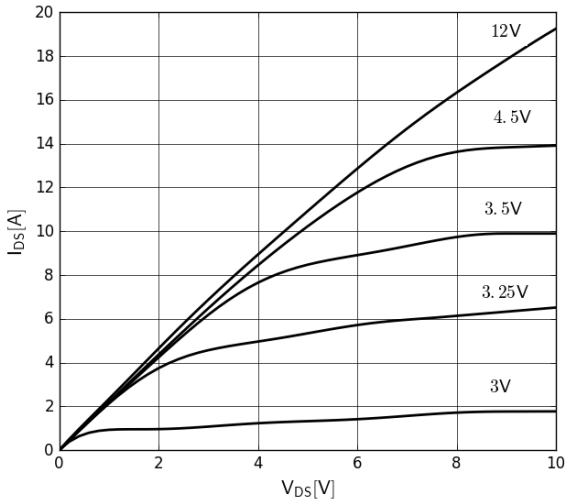


Figure 2. Typical Output Characteristics T_J=150 °C
Parameter: V_{GS}

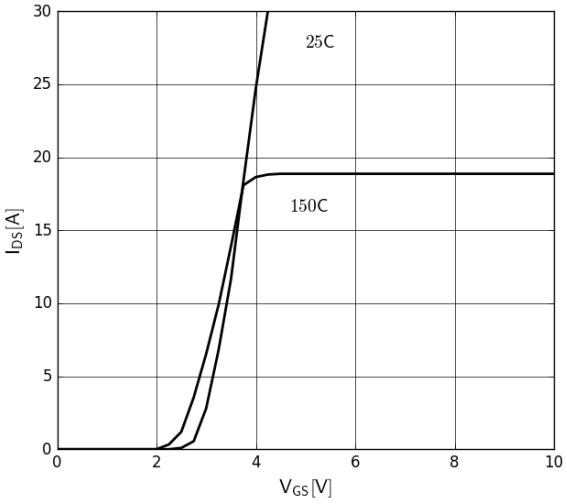


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

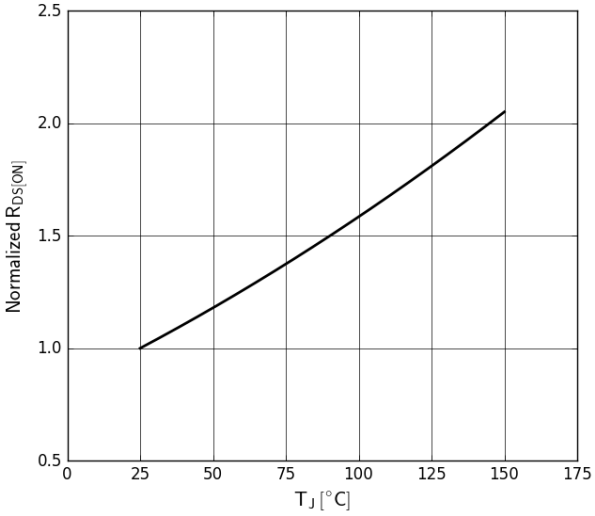


Figure 4. Normalized On-resistance
I_D=16A, V_{GS}=10V

Typical Characteristics (T_C=25 °C unless otherwise stated)

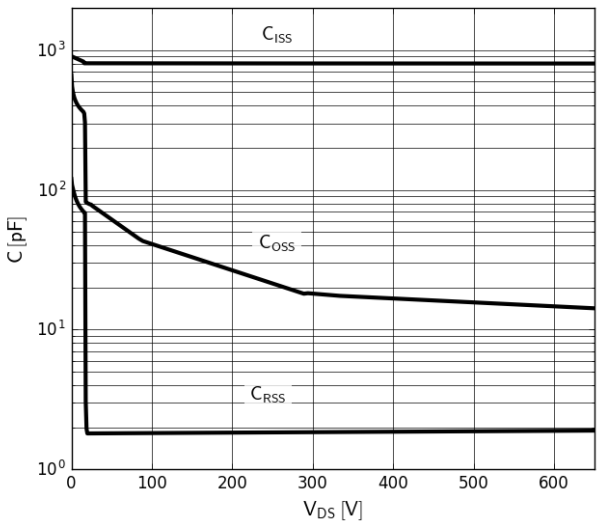


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

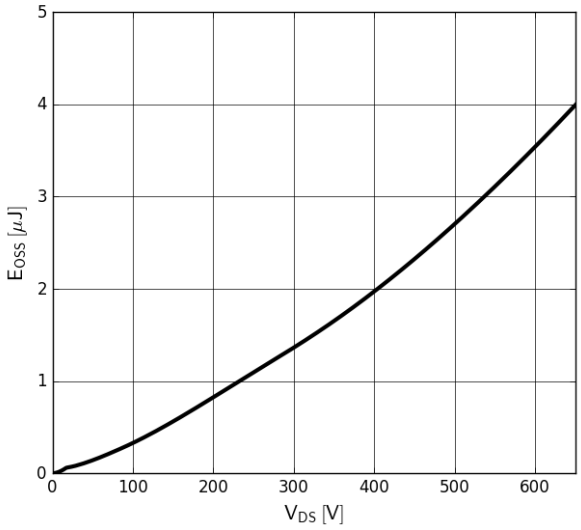


Figure 6. Typical C_{oss} Stored Energy

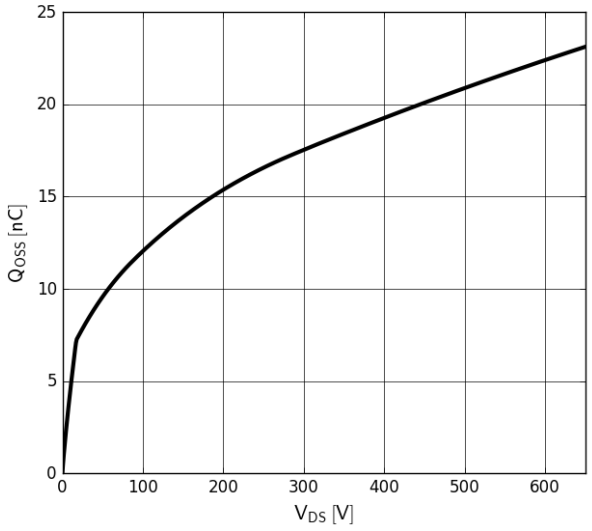


Figure 7. Typical Q_{oss}

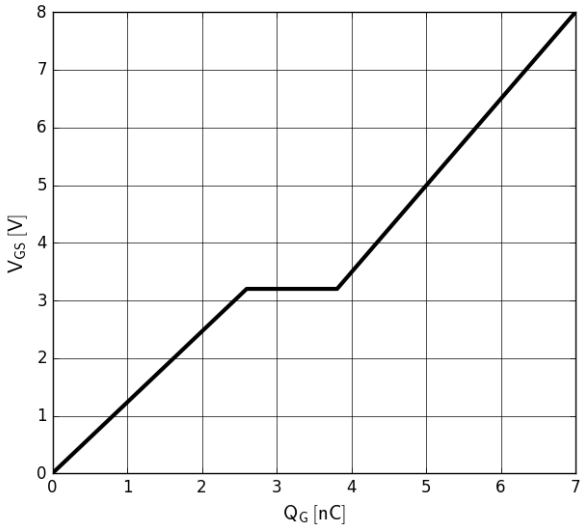


Figure 8. Typical Gate Charge
I_{DS}=4A, V_{DS}=400V

Typical Characteristics (T_C=25 °C unless otherwise stated)

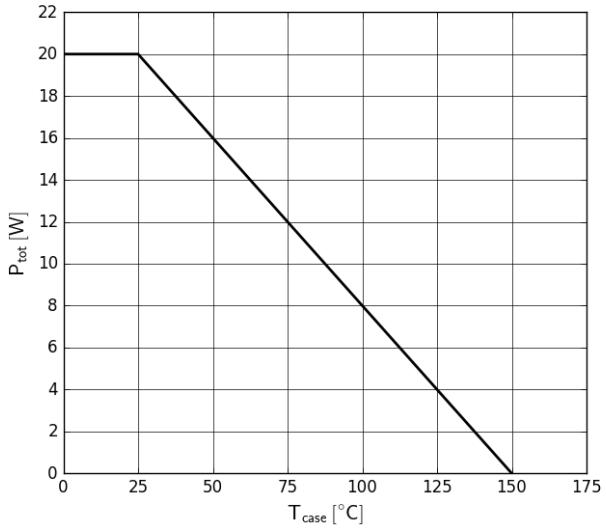


Figure 9. Power Dissipation

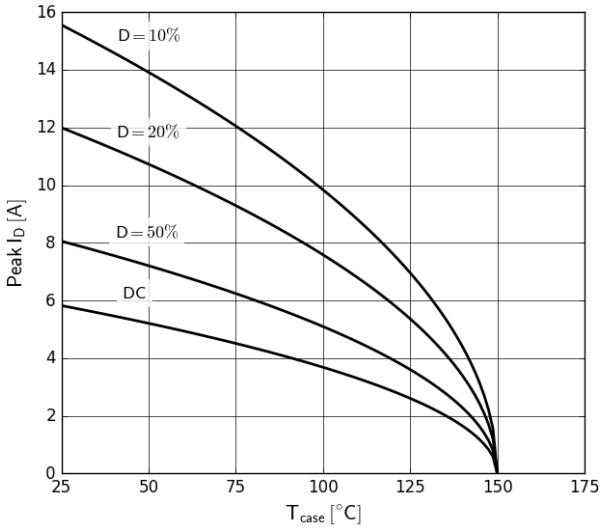


Figure 10. Current Derating
Pulse width ≤ 10µs, V_{GS} ≥ 10V

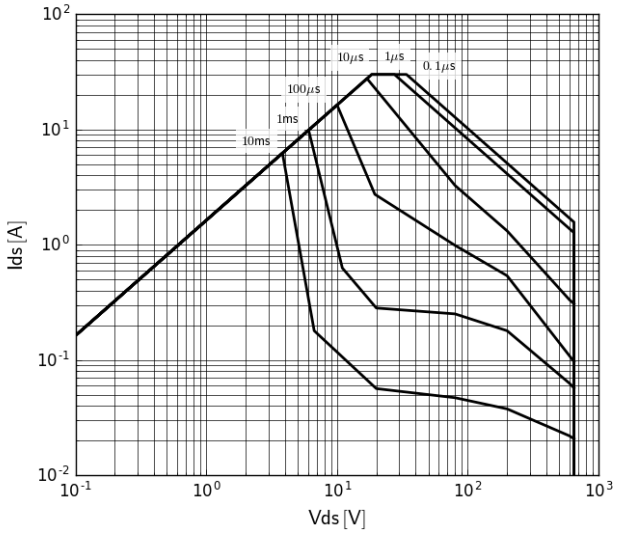


Figure 11. Safe Operating Area T_C=25 °C

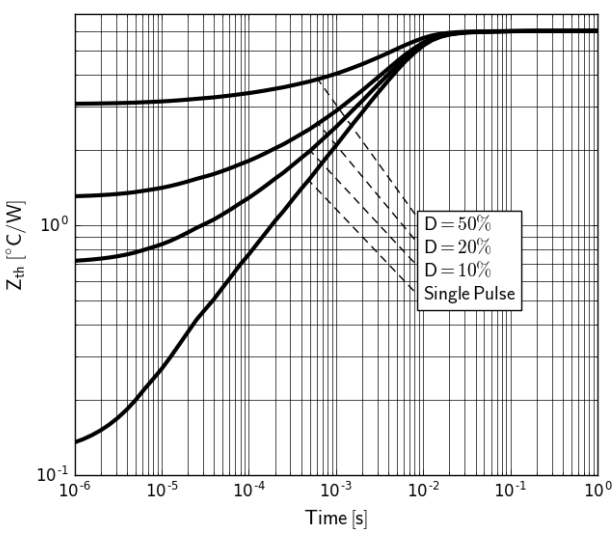


Figure 12. Transient Thermal Resistance

Typical Characteristics (T_C=25 °C unless otherwise stated)

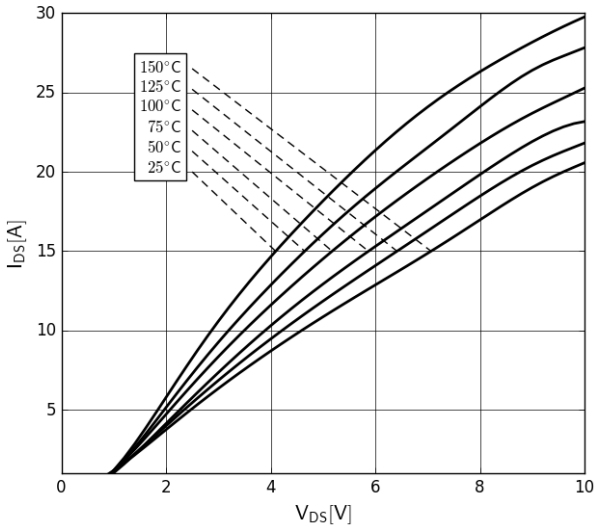


Figure 13. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$, Parameter T_J

Test Circuits and Waveforms

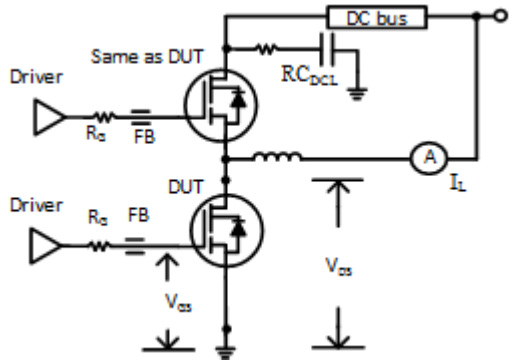


Figure 14. Switching Time Test Circuit
(see circuit implementation on page 3
for methods to ensure clean switching)

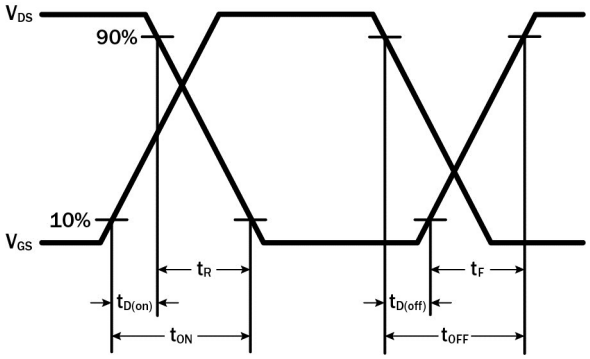


Figure 15. Switching Time Waveform

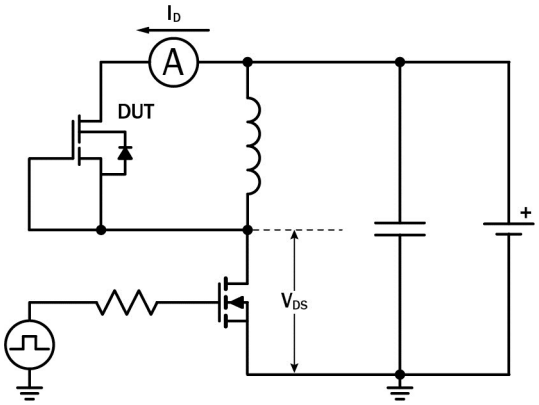


Figure 16. Diode Characteristics Test Circuit

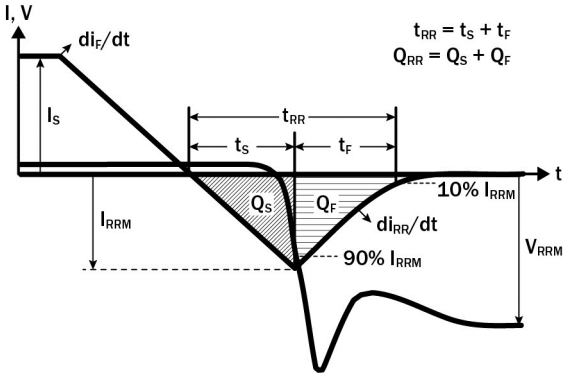
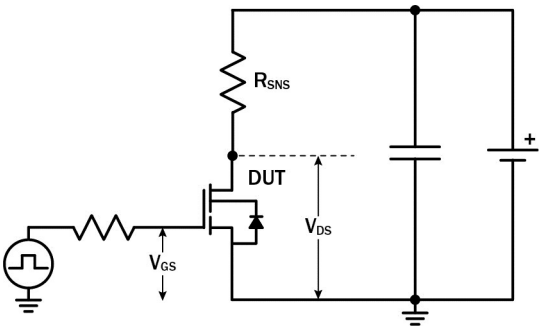
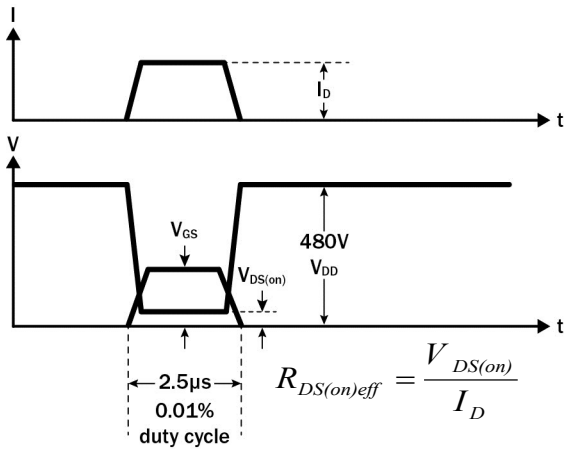


Figure 17. Diode Recovery Waveform





Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

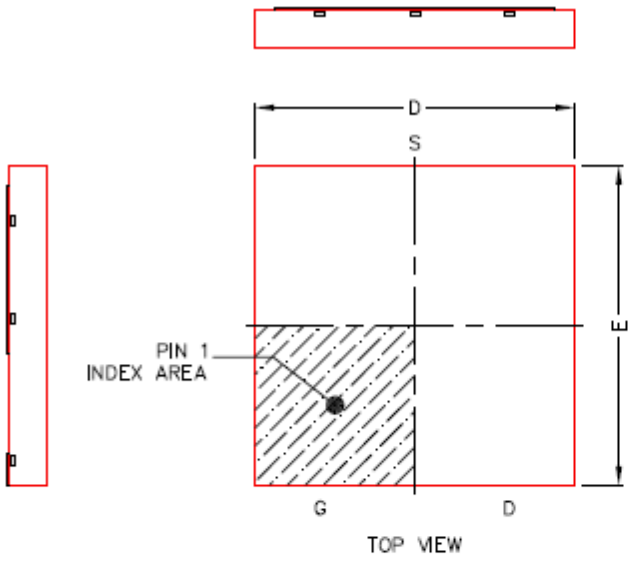
When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

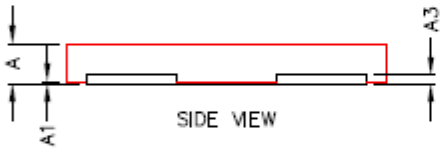
GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

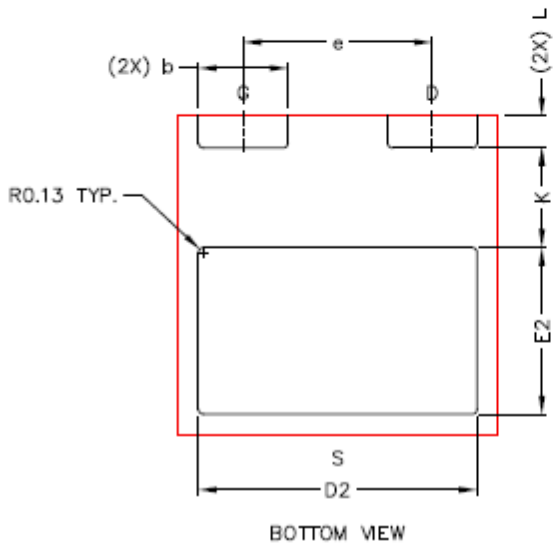
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–	0.05
A3		0.20 REF.	
b	2.20	2.25	2.30
D	7.90	8.00	8.10
D2	6.85	7	7.15
E	7.90	8.00	8.10
e		4.75 BSC	
E2	4.03	4.18	4.33
K	2.50	–	–
L	0.70	0.80	0.90

NOTES:

1. PIN 1 INDICATOR IS LASER MARKED.
   RADIUS AND LOCATION WITHIN THE PIN 1 INDEX AREA.
2. EXPOSED DIE PAD TIE BARS AND LEAD SIDE TERMINALS ARE NOT PLATED.

Revision History

Version	Date	Change(s)
0	3/1/2018	Preliminary Datasheet
1	8/20/2019	Preliminary Datasheet