



十速科技股份有限公司  
tenx technology inc.

**Advance  
Information**

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# **TP6801**

## **USB Full Speed Controller (Preliminary)**

### **Data Sheet**

**Tenx reserves the right to change or  
discontinue this product without notice.**

**tenx technology inc.**

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**Preliminary**

**tenx technology, inc.**

Rev 1.0, 2008/09/16

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## 1. General Description

The TP6801 is a 12T 8051 embedded device tailored to the USB full speed general purpose application. TP6801 was designed for connecting PC or operating at stand-alone (non-PC) mode.

## 2. Features

### (1). Operation Frequency

- FAST mode: 24MHz crystal oscillation with internal 48MHz PLL at 5.0V for USB mode
- SLOW mode: Adjustable ext. R/C, RC oscillator at 2.0V~3.6V for battery system (optional)
- STOP mode

### (2). On-Chip Memory

- 16k x 8 internal program OTP-ROM
- Internal RAM 256bytes and external XRAM up to 384bytes

### (3). USB interface

- Compliance with the Universal Serial Bus specification v2.0 Full Speed
- Built-in USB Transceiver, 3.3V regulator
- Support USB Suspend /Resume and Remote Wakeup function
- Endpoint 0: Control SETUP/IN/OUT transfer (each 8 bytes)
- Endpoint 1: BULK-IN transfer with Pin-Pong feature (2\*64 bytes)
- Endpoint 2: BULK-OUT transfer with Pin-Pong feature (2\*64 bytes)
- Endpoint 3: BULK-IN transfer (64 bytes)
- Endpoint 4: BULK-OUT transfer (64 bytes)
- Endpoint 5: INTERRUPT IN transfer (8 bytes)

### (4). Smart Card Interface

- Support I/O 1.8V/3.0V/3.3V/5.0V/Vbattery by chip configuration
- Support clock rate 12MHz/6MHz/3MHz

### (5). PWM

- Support 2 channels of Pulse Width Modulation (PWM) function with 8-bit resolution

**(6). Reset Controller**

- Power On Reset, Low Voltage Reset, Watch-Dog Timer, USB Plug-out Reset

**(7). Full-Duplex UART interface**

- Tx/Rx FIFO (each 8bytes, each 8 depth)
- Baud rate clock up to 3Mbps
- Break function

**(8). SPI interface**

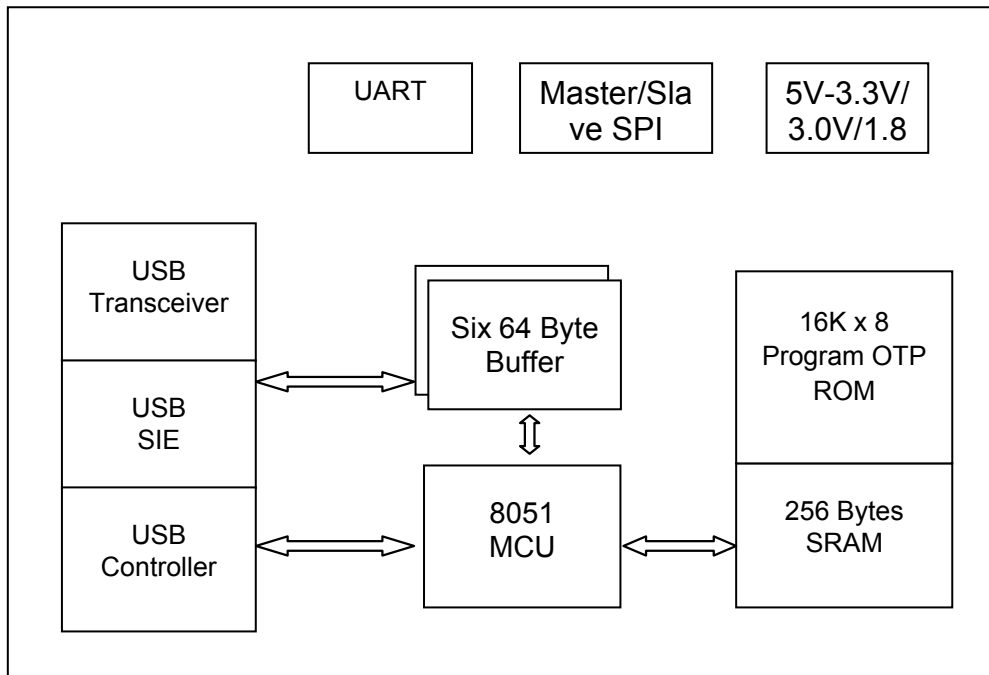
- Support Mode0, 1, 2, 3
- 1x Master/Slave (Tx FIFO 8\*8 bytes, Rx FIFO 8\*8 bytes) and 1x Master (Tx FIFO 8\*8 bytes, Rx FIFO 8\*8 bytes)
- Clock rate up to 6Mbps

**(9). Support 32768Hz Crystal pin for Accuracy timing in low power mode (optional)****(10). Keep SRAM data when USB un-plug (need battery)****(11). I/O Ports**

- 4 external Interrupts with wakeup function

**(12). LQFP48/Die Form**

### 3. Functional Block Diagram



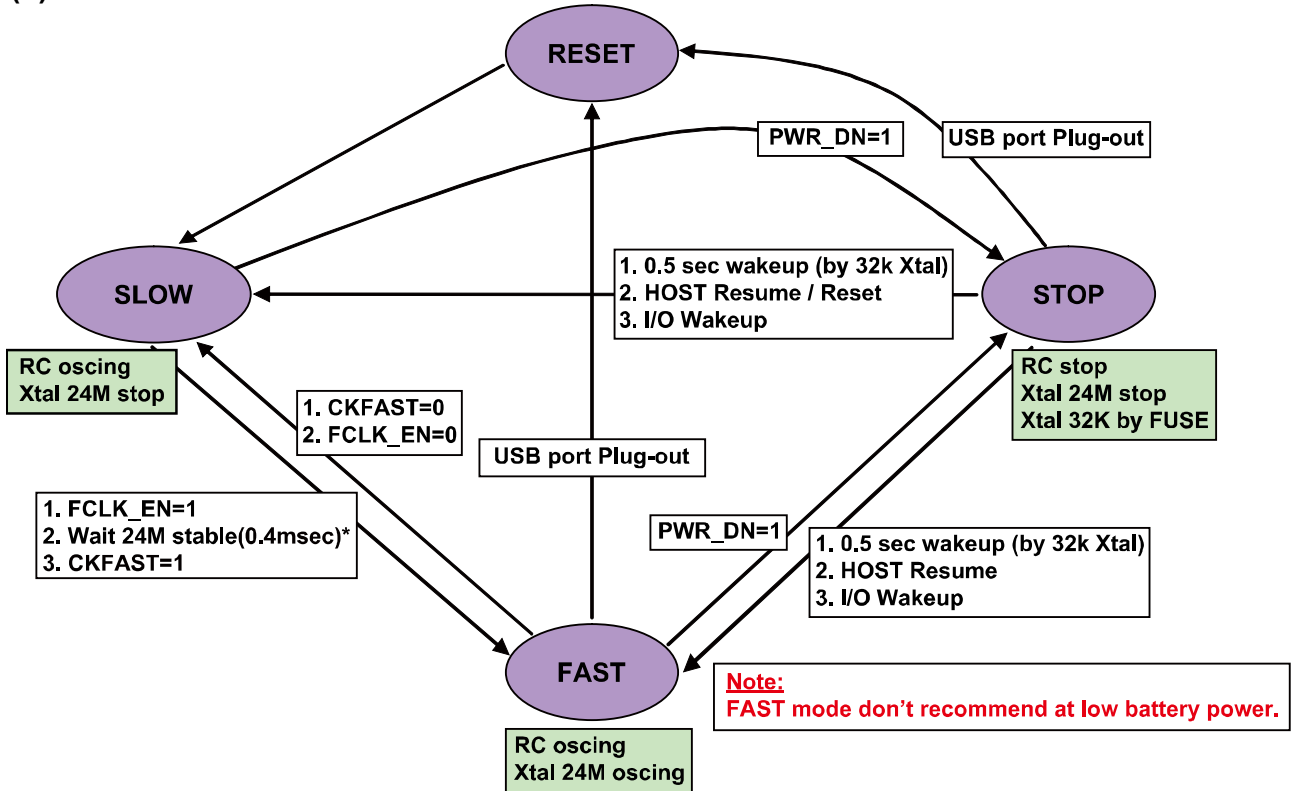
## 4. Pin Description

Name	I/O	Description
VDD	P	5V Power from USB cable
VSS	P	Ground
VBAT	P	Battery power
VIO	O	Chip I/O voltage, (1.8V/3.0V/3.3V/5V/VBAT by chip configuration)
FX1	I	Crystal in (24MHz)
FX2	O	Crystal out
LX1	I	Crystal in (32KHz)
LX2	O	Crystal out
OSCI	I	RC clock, external capacitor and resistor
VPP/RESETn	I	OTP programming power/Chip reset pin
TESTn[1:0]	I	Test Mode control
V33	O	3.3V regulator output
DP	I/O	USB positive data signal
DM	I/O	USB negative data signal
P1[7:0]	I/O	8051's Port1
P3[1:0]	I/O	8051's Port3[1:0]
P3.5/T0	I/O	8051's Port3.5 / Timer 0
P3.4/T1	I/O	8051's Port3.4 / Timer 1
PA[7:0]	I/O	GPIO
PB[0]	I/O	GPIO or SPIA serial clock out (I/O voltage = VIO/Vbat)
PB[1]	I/O	GPIO or SPIA serial data out (I/O voltage = VIO/Vbat)
PB[2]	I/O	GPIO or SPIA serial data input (I/O voltage = VIO/Vbat)
PB[3]	I/O	GPIO or SPIA slave input enable (I/O voltage = VIO/Vbat)
PB[4]	I/O	GPIO or SPIB serial clock out
PB[5]	I/O	GPIO or SPIB serial data out
PB[6]	I/O	GPIO or SPIB serial data input
PB[7]	I/O	GPIO or smart card clock out (I/O voltage = VIO/Vbat)
PC[0]	I/O	GPIO with Wake-up interrupt
PC[1]	I/O	GPIO with Wake-up interrupt
PC[2]	I/O	GPIO with Wake-up interrupt
PC[3]	I/O	GPIO with Wake-up interrupt
PC[4]	I/O	GPIO or PWMB output
PC[5]	I/O	GPIO or PWMA output
PC[6]	I/O	GPIO or UART data receive input
PC[7]	I/O	GPIO or UART data transmit output (I/O voltage = VIO/Vbat)

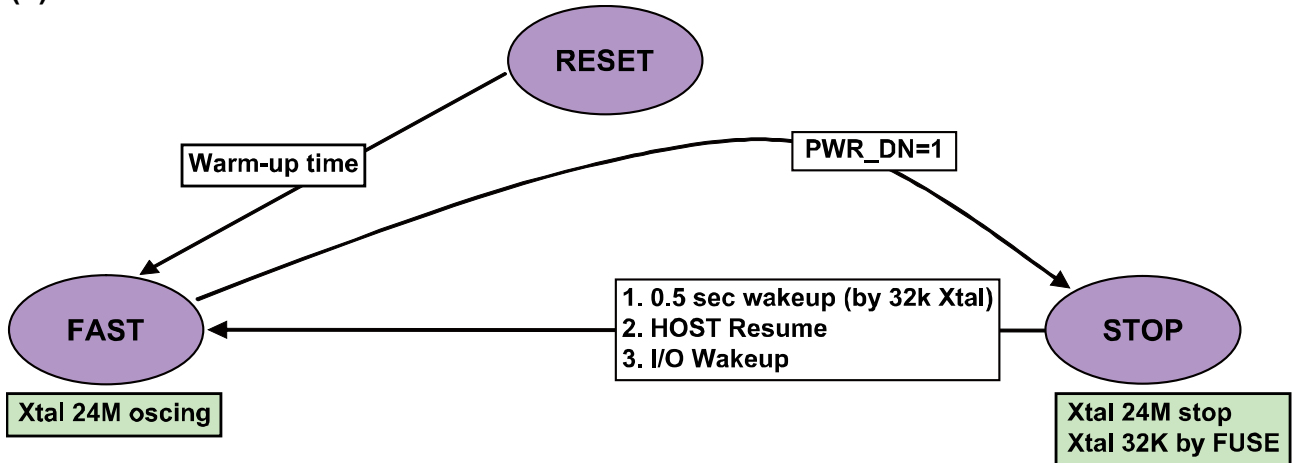
All I/O ports are pseudo-open drain type.

I/O voltage is fix 3.3V, unless otherwise specified.

(1). DUAL MODE



(2). SINGLE MODE



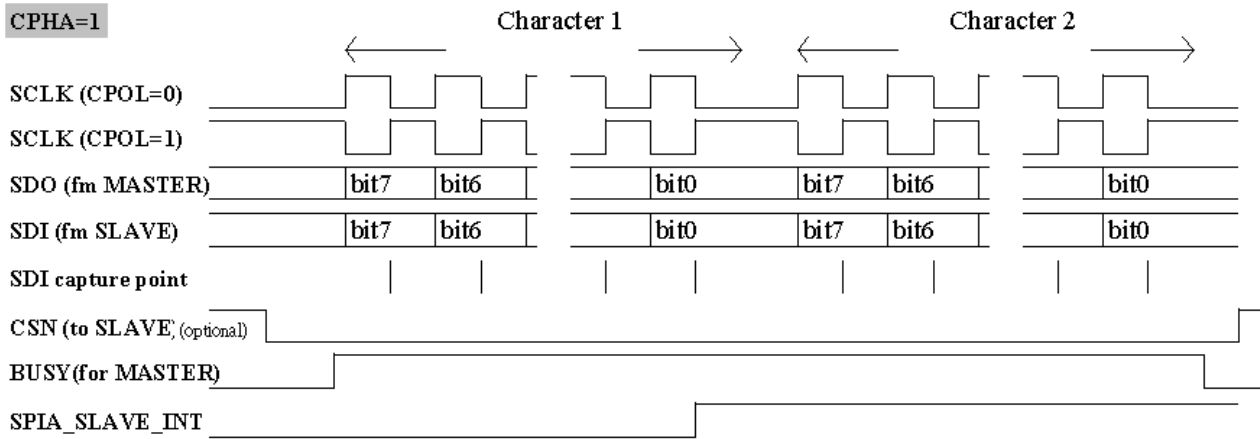
(3). CPU Operation Mode V.S. Peripheral Clock:

	DUAL MODE <sup>(Note-1)</sup>		SIGNLE MODE(1)	NOTE
	SLOW <sup>(Note-2)</sup>	FAST <sup>(Note-2)</sup>		
CPUCLK(CPU51)	RC osc	24MHz	24MHz	
USB function	N/A	48MHz	48MHz	
UART	N/A	48MHz	48MHz	
SPI	CPUCLK	CPUCLK	CPUCLK	
WDT	CPUCLK	CPUCLK	CPUCLK	
Smart Card	CPUCLK	CPUCLK	CPUCLK	
PWM	CPUCLK	CPUCLK	CPUCLK	
0.5sec timer wakeup Interrupt	0.5sec	0.5sec	0.5sec	If 32KHz Xtal <sup>(Note-3)</sup> is available

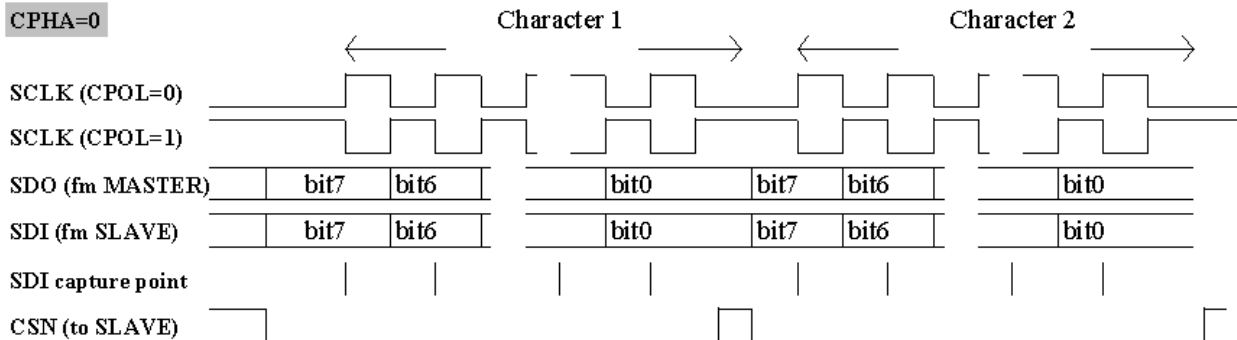
**Note:** 1. & 3. function enable/disable control by FUSE option.  
 2. CPU clock mode switching control by firmware.

(4). SPI Timing:

CPHA=1

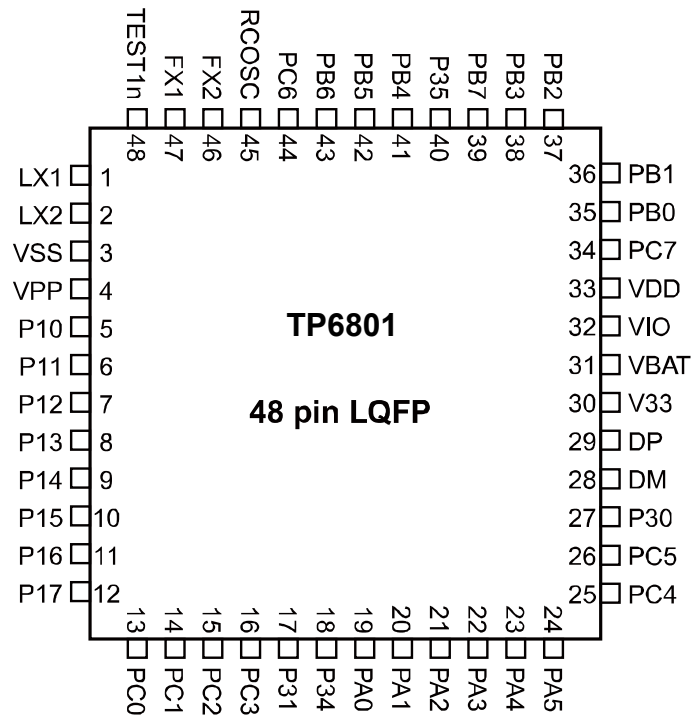


CPHA=0





5. Package

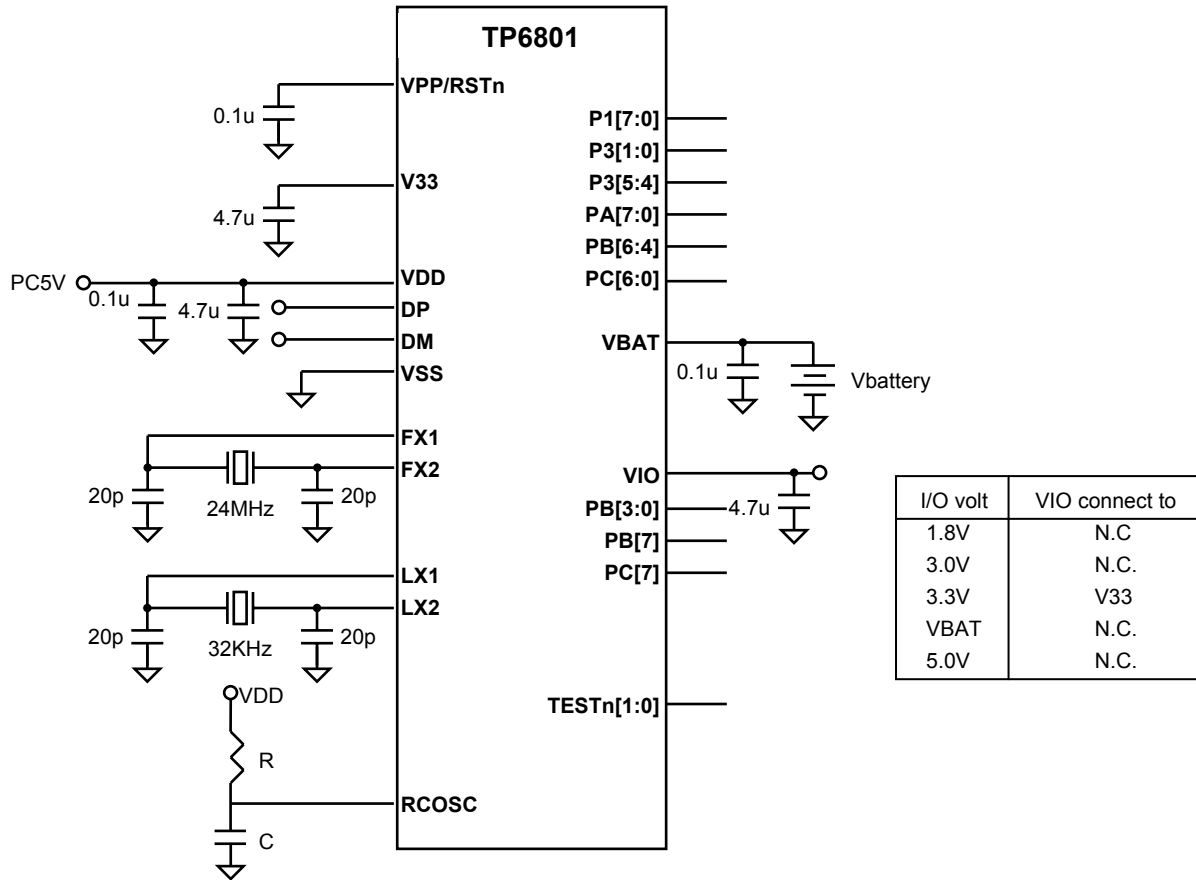


6. Pad List

(2880, 2950)

Probe Number	Pad Name	X Coordinate	Y Coordinate	Probe Number	Pad Name	X Coordinate	Y Coordinate
1	PADRC	747.50	2839.00	32	PADPA5	2033.50	111.00
2	PADTSTN0	620.50	2839.00	33	PADPA6	2151.50	111.00
3	PADFX2	499.50	2839.00	34	PADPA7	2269.50	111.00
4	PADFX1	377.50	2839.00	35	PADPC4	2387.50	111.00
5	PADTSTN1	111.00	2538.50	36	PADPC5	2505.50	111.00
6	PADLX1	111.00	2420.50	37	PADP30	2769.00	374.50
7	PADLX2	111.00	2258.50	38	PADPE2	2769.00	492.50
8	VSS	111.00	2140.50	39	PADPE3	2769.00	609.10
9	VSS	111.00	2022.50	40	PADDM	2769.00	846.50
10	PADVPP	111.00	1672.50	41	PADDP	2769.00	1138.50
11	PADP10	111.00	1554.50	42	PADV33	2769.00	1262.50
12	PADP11	111.00	1318.50	43	PADVBAT	2769.00	1495.45
13	PADP12	111.00	1200.50	44	PADVIO	2769.00	1726.70
14	PADP13	111.00	1082.50	45	VDD	2769.00	1968.70
15	PADP14	111.00	846.50	46	VDD	2769.00	2086.70
16	PADP15	111.00	728.50	47	PADPC7	2769.00	2322.70
17	PADP16	111.00	610.50	48	PADPB0	2769.00	2440.70
18	PADP17	111.00	492.50	49	PADPB1	2769.00	2558.70
19	PADPC0	111.00	374.50	50	PADPB2	2505.50	2839.00
20	PADPC1	381.50	111.00	51	PADPB3	2387.50	2839.00
21	PADPC2	499.50	111.00	52	PADPB7	2269.50	2839.00
22	PADPC3	617.50	111.00	53	PADPE4	2145.50	2839.00
23	PADP31	735.50	111.00	54	PADPE5	2027.50	2839.00
24	PADP34	853.50	111.00	55	PADP35	1791.50	2839.00
25	PADPE0	1089.50	111.00	56	PADPB4	1673.50	2839.00
26	PADPE1	1207.50	111.00	57	PADPB5	1555.50	2839.00
27	PADPA0	1325.50	111.00	58	PADPE6	1437.50	2839.00
28	PADPA1	1443.50	111.00	59	PADPE7	1319.50	2839.00
29	PADPA2	1561.50	111.00	60	PADPB6	1201.50	2839.00
30	PADPA3	1679.50	111.00	61	PADPC6	1083.50	2839.00
31	PADPA4	1797.50	111.00				

### 7. Application Circuit



## 8. Electrical Characteristics

### (1). ABSOLUTE MAXIMUM RATINGS (GND= 0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	-5 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

### (2). RECOMMEND OPERATING CONDITION (at Ta=-20°C to 70°C,GND= 0V)

Name	Symb.	Min.	Max.	Unit
Supply Voltage(USB mode)	VDD	4.5	5.5	V
Battery Voltage(battery mode)	Vbat	2.1	4.1	V
Chip I/O Voltage	Vio	1.8	5.5	V
Input "L" Voltage	Vil1	0	0.3xVio	V

### (3). DC CHARACTERISTICS (at Ta=25 °C,VDD=5.0V, VSS= 0V, Fosc=24MHz)

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
FAST clock	fclk		24		MHz		
SLOW clock	sclk	-30%	1	+30%	MHz	VBAT=3.0V, VDD=NC ExtC=750pF, ExtR=1K	
Threshold voltage of USB detection	Vdet		4.2		V		
Operating current	Icc1	-	16	-	mA	Fosc=24MHz	No load
	Icc2		1.4		mA	24MHz off, Fosc=1MHz VBAT=3.0V, VDD=N.C.	No load
Suspend current	I <sub>sus</sub>	-	340	500	uA	USB mode	No load
Power down current	I <sub>pd1</sub>			1	uA	RC mode, no 32KHz	No load
	I <sub>pd2</sub>		3	5	uA	RC mode with 0.5s wake up, disable Wakeup Int	No load
Port Output High Current	I <sub>oh1</sub>	6			mA	V <sub>oh</sub> =V <sub>io</sub> -0.4V, V <sub>io</sub> >=3.0V	One clk time
	I <sub>oh2</sub>	8			uA		
	I <sub>oh3</sub>	2.6			mA	V <sub>oh</sub> =V <sub>io</sub> -0.4V, V <sub>io</sub> =1.8V	One clk time
	I <sub>oh4</sub>	4			uA		
Port Output Low Current	I <sub>ol1</sub>	8			mA	V <sub>ol</sub> =V <sub>SS</sub> +0.2V, V <sub>io</sub> >=3.0V	
	I <sub>ol2</sub>	4			mA	V <sub>ol</sub> =V <sub>SS</sub> +0.06V, V <sub>io</sub> =1.8V	
VIO pin voltage	Vio1	1.7		1.9	V	I=40mA	Vio set 1.8V
	Vio2	2.9		3.1	V	I=80mA	Vio set 3V
	Vio3	3.2		3.4	V	I=120mA	Vio tie to V33
	Vio4	VDD-0.1		VDD	V		Vio set 5V
	Vio5	Vbat-0.1		Vbat	V	No PC5V, battery only	
Port Input High Voltage	Vih	0.55Vio			V	Schmitt trigger	

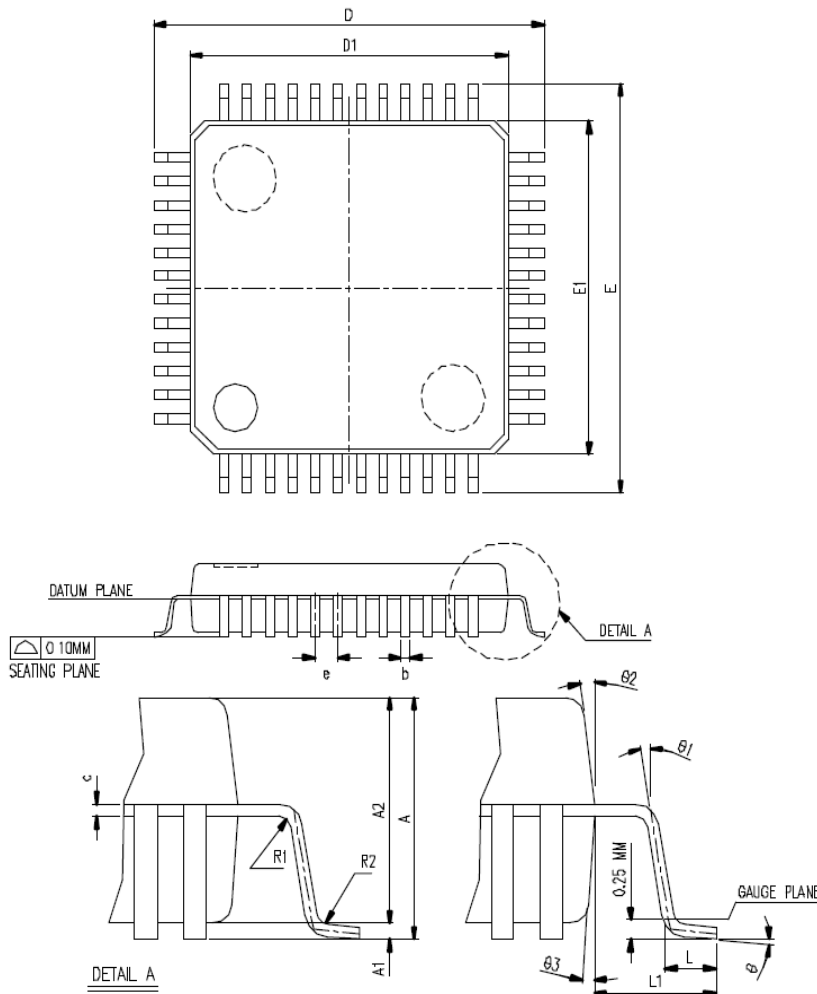
(4). AC CHARACTERISTICS (at Ta=25 °C, VDD5V=5.0V, VSS= 0V, Fosc=24MHz)

Name	Symb.	Min.	Typ.	Max.	Unit	Note
DP/DM rising time	Trise	4		20	ns	
DP/DM falling time	Tfall	4		20	ns	
DP,DM cross point	Vx	1.3		2.0	V	
V33 output voltage	Vreg	3.2	3.3	3.4	V	

**Note:** All USB transceiver characteristics can meet USB1.1 spec.

9. Package Information

(1). LQFP48:



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	D 22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
e	0.50 BASIC			0.020 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R2	0.08		0.20	0.003		0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BFC)					

\*NOTES · DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.