十速科技股份有限公司
tenx technology inc.

Advance Information

TP6823

USB Full Speed Game Pad Controller

Data Sheet

Tenx reserves the right to change or discontinue this product without notice.

Contain

1. GENERAL DESCRIPTION

The TP6823 is an 8051 embedded device tailored to the USB full speed Game Pad controller application. TP6823 was designed for connecting PC or operating at stand-alone (non-PC) mode. It also supports powerful functions and interfaces, such as USB Keyboard, USB Mouse, USB Joystick, USB HID, 10-bit A/D converter for data acquisition and 20 channels input analog or digital control all in one unit for Game Pad control, speech PWM output, PWM 2 channels of Pulse Width Modulation for Voice Vibration feedback, master/slave SPI and external parallel bus (NOR, NAND interface), RF 2.4G and Bluetooth control interface, G-sensor control interface.

2. FEATURES

(1). Dual Power System

- USB 5V and/or battery-in dual power systems

(2). Operation Frequency

- FAST mode
- 6MHz crystal oscillator for PLL clock source, PLL generate 48MHz for USB data transaction and 24MHz/6MHz for CPU clock
- SLOW mode
- External resistor, RC oscillator at 2.0V~3.6V for battery system (optional)
- 32KHz crystal oscillator for CPU clock and accuracy timing in low power mode (optional)
- STOP mode

(3). On-Chip Memory

- 32k x 8 internal program OTP-ROM
- Internal RAM 256 bytes and external XRAM up to 320 bytes

(4). USB interface

- Compliance with the Universal Serial Bus specification v2.0 Full Speed
- Built-in USB Transceiver, 3.3V regulator
- Software Control USB pull-up resister
- Support USB Suspend /Resume and Remote Wakeup function
- Endpoint 0: Control SETUP transfer (8 bytes)
- Endpoint 0: Control IN/OUT transfer (64 bytes)
- Endpoint 1: BULK-IN transfer with Pin-Pong feature (2*64 bytes)

- Endpoint 2: BULK-OUT transfer with Pin-Pong feature (2*64 bytes)
- Endpoint 3: INTERRUPT IN transfer (8 bytes)

(5). ADC (Analog to Digital Converter)

- 20 input channels analog or digital control all in one unit for Game Pad control
- 10-bit SAR A/D converter

(6). Speech PWM Out

- 8-bit unsigned PCM format
- 8KHz sampling rate for Audio Playback
- Class-D Amplify for Speaker Out

(7). NOR Interface

- Data transfer for all of External XRAMs
- H/W handle NOR command procedure
- Read DMA (up to 64 bytes per time)
- Write DMA (up to 64 bytes per time)

(8). NAND Interface

- Data transfer for all of External XRAMs
- Write DMA (up to 64 bytes per time)
- Read DMA (up to 64 bytes per time)
- Compatible with 8-bit parallel interface

(9). SPI Interface

- Mode0, 1, 2, 3
- Master or Slave mode
- Clock Rate up to 12Mbps
- Read DMA (up to 64 bytes per time)
- Write DMA (up to 64 bytes per time)

(11). PWM

- Support 2 channels of Pulse Width Modulation (PWM) function with 8-bit resolution
- Voice Vibration feedback for Game Pad

(12). Reset Controller

- Power On Reset
- Low Voltage Reset
- Watch-Dog Timer

- USB Plug-in Reset
- Plug-out Reset

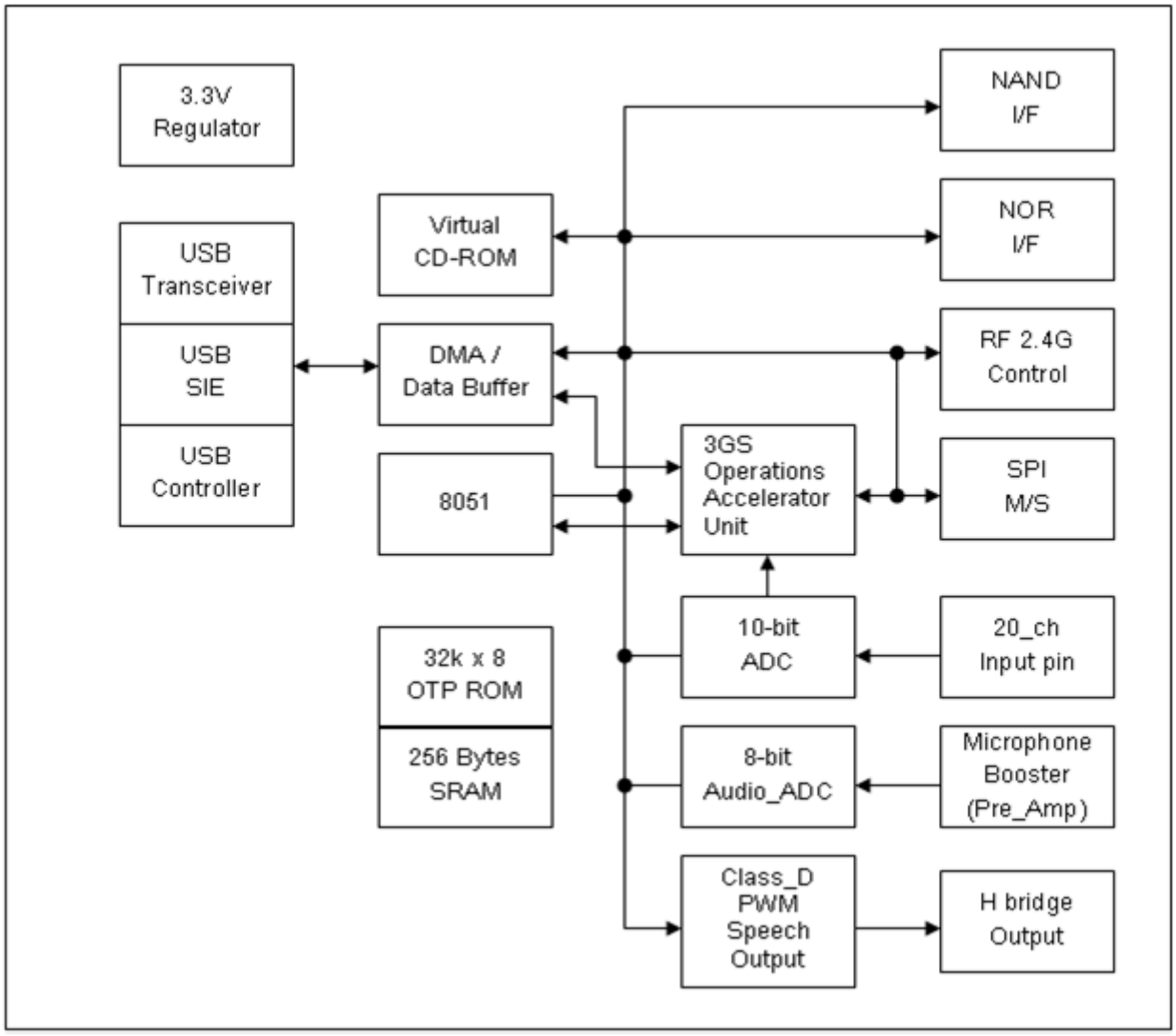
(13). Keep SRAM data when USB un-plug (need battery)

(14). LQFP80 / Die Form / Customer Request

(15). Application

- USB full speed Game Pad for PS3 peripheral application
- USB full speed Game Pad for G-sensor application
- USB full speed Game Pad for RF 2.4G wireless application
- USB full speed Game Pad for Bluetooth wireless application
- USB full speed Game Pad with Built-in Games application

3. Functional Block Diagram



4. Pin Description

Name	I/O	Description		
DVDD	P	5V Power from USB cable		
DGND	P	Ground		
PC5VDET	I	USB 5V detection pin, should connect to USB powe		
VBAT	P	Battery power in		
V33	O	3.3V regulator output		
DP	I/O	USB positive data signal		
DM	I/O	USB negative data signal		
VPP/RESETn	I	OTP programming power/Chip reset pin (internal pull-up)		
TESTn[1:0]	I	Test Mode control (internal pull-up)		
FX1	I	Crystal in (6MHz)		
FX2	O	Crystal out		
VDDX	P	PLL power		
FLTC	I	PLL filter		
VSSX	P	PLL ground		
LX1	I	Crystal in (32KHz)		
LX2	O	Crystal out		
VR	I	RCLK clock, external resistor		
RF_RST	O	RF Reset (Bluetooth, RF 2.4G)		
CSA	O	Serial flash Chip enable		
CSB	O	Chip enable pin		
CLE	O	NAND Flash Command Latch Enable		
CSM	O	NAND Flash Chip Enable		
CSR	O	RF Chip Enable		
ALE	O	NAND Flash Address Latch Enable		
RDY	I	NAND Flash ready output		
WP	I	NAND Flash Write Protect		
Key1	I/O	Function Key and 8051's UART (RXD)		
Key2	I/O	Function Key and 8051's UART (TXD)		
T0	I/O	8051's Timer 0 and USB Power enable		
T1	I/O	8051's Timer 1 and System Power enable		
ADC[4:0]	I/O	ADC_CH[4:0]	NOR_FA[4:0] (o)	wake-up interrupt
ADC5	I/O	G-Sensor AXOUT	ADC_CH[5]	NOR_FA[5] (o)
ADC6	I/O	G-Sensor AYOUT	ADC_CH[6]	NOR_FA[6] (o)
ADC7	I/O	G-Sensor AZOUT	ADC_CH[7]	NOR_FA[7] (o)
D[3:0]	I/O	NAND_DIO[3:0] (b)	NOR_FD[3:0] (b)	
D[7:4]	I/O	NAND_DIO[7:4] (b)	NOR_FD[7:4] (b)	ADC_CH[19:16]
WRN	I/O	NAND_WRN (o)	NOR_WRN (o)	wake-up interrupt
RDN	I/O	NAND_RDN (o)	NOR_RDN (o)	wake-up interrupt
Key0	I	Function Key with wake-up interrupt (b)		
RF_PKT	I	RF Packet flag		
LED	O	LED Output with PWM		
RF_FIFO	I	RF FIFO		

RF_CLK	O	RF SPI CLK Output
RF_DO	O	RF SPI Data Output
RF_DI	I	RF SPI Data Input
ADC[15:8]		ADC Channel[15:8]
CSG	O	G-Sensor Chip select
FS0	I	G-Sensor Function select 0
FS1	I	G-Sensor Function select 1
FS2	I	G-Sensor Function select 2
ADC:		
AVDD	P	Analog Power
AGND	P	Analog Ground
MICP	I	Micro-phone MIC IN+ input
MICN	I	Micro-phone MIC IN- input
VREF	I	External reference voltage
ANAI	I	AC couple in
ANAO	O	AC couple out
Speech PWM:		
VDDW	P	PWM Power
PWMP	O	Speech PWMP output
PWMN	O	Speech PWMN output
VSSW	P	PWM Ground

All I/O Pin are pseudo-open drain type, unless otherwise specified function.

5. CPU Operation Mode V.S. Peripheral Clock

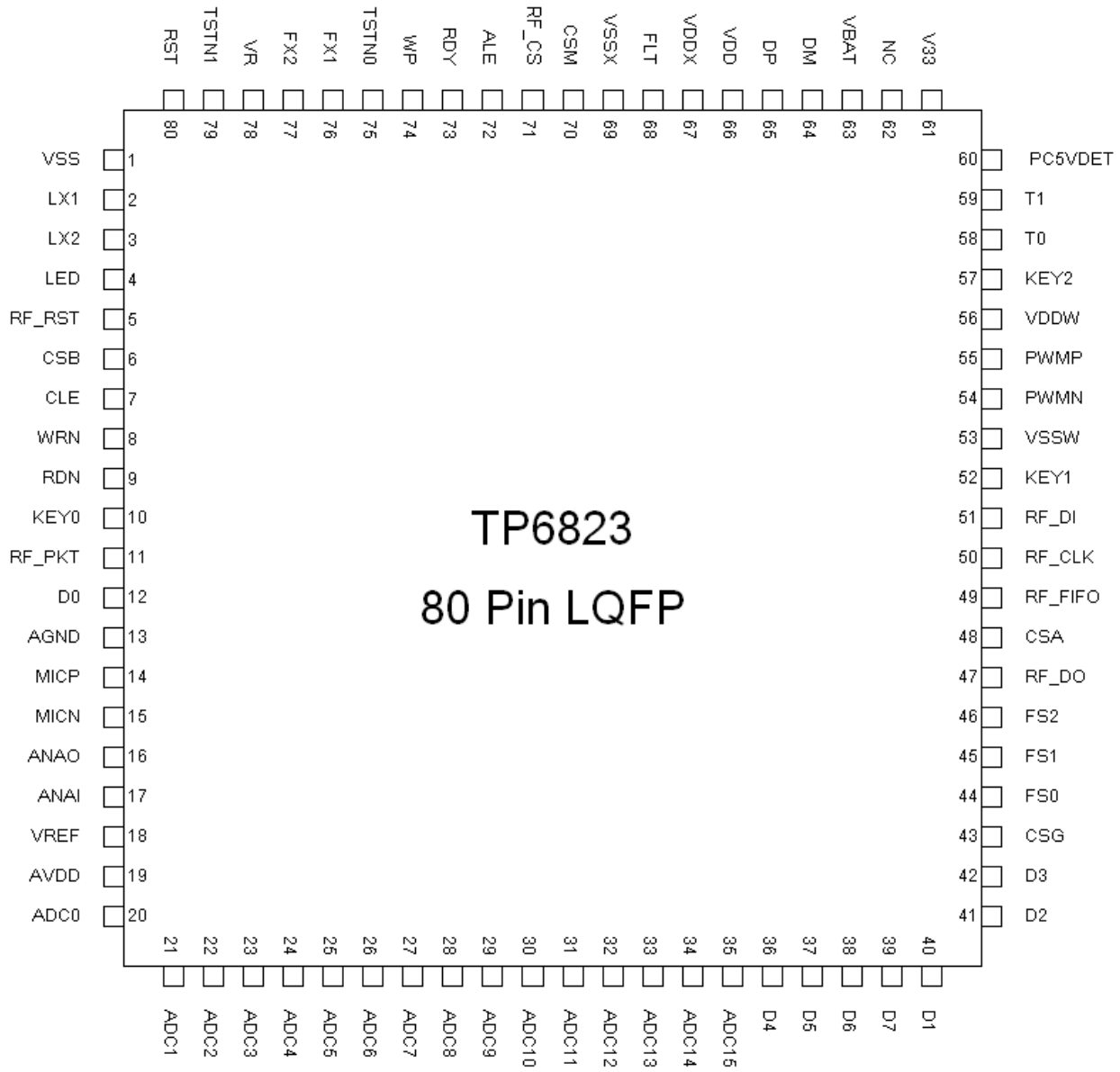
	DUAL MODE[1]		SIGNLE MODE[1]	NOTE
	SLOW [2]	FAST [2]		
CPUCLK(CPU51)	RCLK/32KHz	6M/24MHz	6M/24MHz	
USB function	N/A	48MHz	48MHz	
NAND DMA	N/A	6MHz	6MHz	XTAL_EN = 1
NOR DMA	N/A	6MHz	6MHz	
A/D converter	N/A	6MHz	6MHz	
Recording	N/A	6MHz	6MHz	
Speech PWM	N/A	6MHz	6MHz	
SPI	CPUCLK	CPUCLK	CPUCLK	
WDT	CPUCLK	CPUCLK	CPUCLK	
PWMA/B	CPUCLK	CPUCLK	CPUCLK	
0.5sec timer wakeup Interrupt	0.5sec	0.5sec	0.5sec	If 32KHz Xtal[3] is available

Notes:

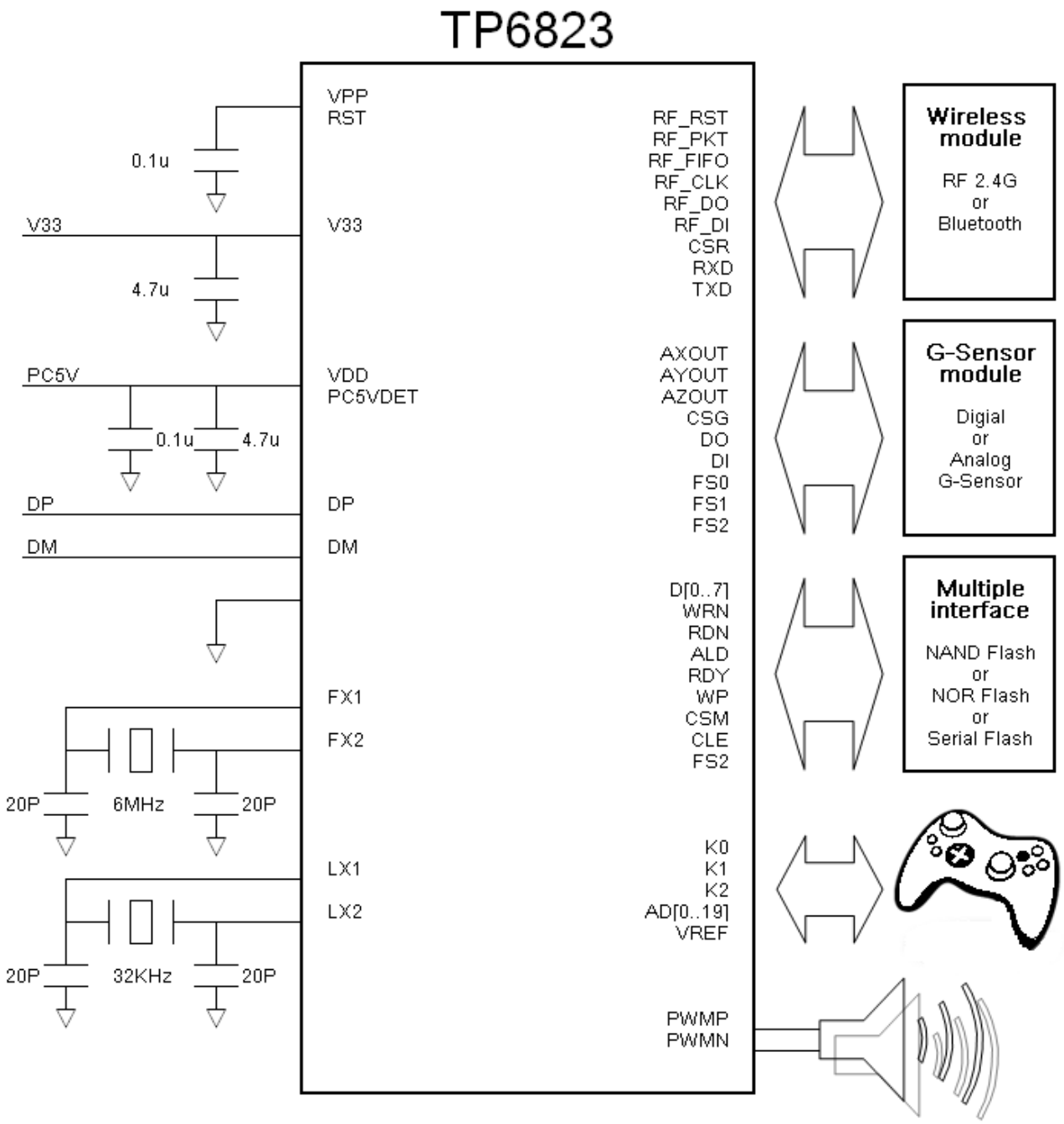
(1) & (3) Function enable/disable control by FUSE option.

(2) CPU clock mode switching control by firmware.

6. Package


TP6823
80 Pin LQFP
1 VSS
2 LX1
3 LX2
4 LED
5 RF_RST
6 CSB
7 CLE
8 WRN
9 RDN
10 KEY0
11 RF_PKT
12 D0
13 AGND
14 MICP
15 MICN
16 ANAO
17 ANAI
18 VREF
19 AVDD
20 ADC0
21 ADC1
22 ADC2
23 ADC3
24 ADC4
25 ADC5
26 ADC6
27 ADC7
28 ADC8
29 ADC9
30 ADC10
31 ADC11
32 ADC12
33 ADC13
34 ADC14
35 ADC15
36 D4
37 D5
38 D6
39 D7
40 D1
41 D2
42 D3
43 CSG
44 FS0
45 FS1
46 FS2
47 RF_DO
48 CSA
49 RF_FIFO
50 RF_CLK
51 RF_DI
52 KEY1
53 VSSW
54 PWMN
55 PWMP
56 VDDW
57 KEY2
58 T0
59 T1
60 PC5VDET
61 V33
62 NC
63 VBAT
64 DM
65 DP
66 VDD
67 VDDX
68 FLT
69 VSSX
70 CSM
71 RF_CS
72 ALE
73 RDY
74 WP
75 TSTN0
76 FX1
77 FX2
78 VR
79 TSTN1
80 RST

7. Application Circuit



8. Electrical Characteristics

(1). ABSOLOUTE MAXIMUM RATINGS (GND = 0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD +0.3	V
Maximum output Voltage	Vout	-0.3 to VDD +0.3	V
Maximum Operating Temperature	Topg	-10 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	℃

(2). RECOMMEND OPERATING CONDITION (at Ta = -10℃ to 70℃, GND = 0V)

Name	Symb.	Min.	Max.	Unit
Supply Voltage	VDD	2.2	5.5	V
Battery Voltage, if apply	Vbat	2.2	4.2	V
Input “H” Voltage	Vih	0.9 x VDD	VDD	V
Input “L” Voltage	Vil	0	0.1 x VDD	V

(3). DC CHARACTERISTICS

(at Ta = 25℃, VDD = 5.0V, VSS = 0V, unless otherwise specify)

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
FAST clock	fclk1		24		MHz	XT6MHz On, PLL enable	
	fclk2		6		MHz	XT6MHz On	
SLOW clock	sclk1	0.1		10	MHz	VBAT = 3.0V, VDD = N.C.	
	sclk2		32		KHz	XT32KHz On	
Operating current	Icc1		10		mA	fclk1 = 24MHz, XT6MHz On	No load
	Icc2		0.8		mA	XT6MHz Off, RCLK = 3MHz VBAT = 3.0V, VDD = N.C.	No load
Suspend current	Isus		360	500	uA	USB mode	No load
Power down current	Ipd1		3	5	uA	VDD = 3.0v, XT32KHz Off	No load
Output high current	Ioh1	2.5	3.8	-	mA	Voh = 3.0v, Vbat = 3.3v, VDD = N.C.	One clk time
	Ioh2	4	6	-	uA		
	Ioh3	2.5	3.8	-	mA		PWMA/B
	Ioh4	60	70	-	mA	VDD = 3.3V, Voh = VDD/2	Sph. PWM
Output low current	Iol1	10	15	-	mA	Vol = VSS + 0.4v,	GPIO
	Iol2	20	25	-	mA	Vol = VSS + 0.4v	PWMA/B
Input high voltage	Vih1	1.6		VDD	V	VDD = 3.2V, Vio = V33 = 3.2V PC5V = 0, Schmitt trigger	GPIO
	Vih2	1.7		VDD	V	VDD = 5.0V, Vio = V33 = 3.3V, PC5V > Vih3, Schmitt trigger	GPIO
	Vih3	2.8		VDD	V	Schmitt trigger	PC5V
Pull up resistance	Rup1	5	10	15	KΩ	VDD = 3.3 or 5V	VPP/RSTn
	Rup2	40	50	60	KΩ	VDD = 5V	TEST pin
Pull down resistance	Rdn1	50	100	150	KΩ	PC5V	
V33 pin voltage	V33	3.0	3.3	3.6	V	PC5V > Vih3	
V33 output current	IV33		130		mA	PC5V > Vih3	

(4). A/D conversion

(at Ta = 25℃, VDD = AVDD = 5.0V, VSS = AGND = 0V, unless otherwise specify)

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
Resolution		-	10	-	Bits		
Conversion time	Tadc		24		us	Fadc=1.5MHz	
Differential linearity	DL		±2.5	±4	LSB		
Linearity	IL		±3.2	±5	LSB		
Total error	ERR		±4	±6	LSB		

(5). USB AC CHARACTERISTICS

(at Ta = 25℃, VDD = AVDD = 5.0V, VSS = AGND = 0V)

Name	Symb.	Min.	Typ.	Max.	Unit	Note
DP/DM rising time	Trise	4		20	ns	
DP/DM falling time	Tfall	4		20	ns	
DP,DM cross point	Vx	1.3		2.0	V	
V33 output voltage	Vreg	3.2	3.3	3.4	V	

Note: All USB transceiver characteristics can meet USB1.1 spec.