

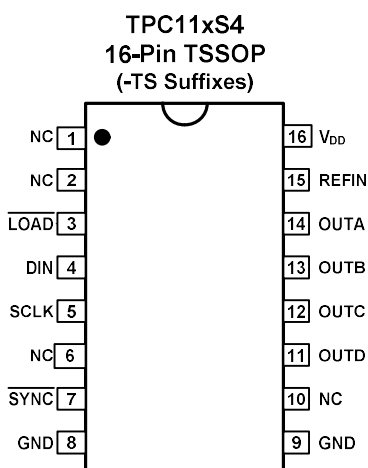
Features

- Quad, 16-/12-Bit Pin Compatible DACs
 TPC116S4: 16bit
 TPC112S4: 12bit
- Low Power Consumption (800µA typ)
- Differential Nonlinearity: $\pm 1\text{LSB}(\text{max})$
- Glitch Energy: 0.1nV-s
- Power-On Reset to Zero
- Supply Range: 2.7V to 5.5V
- Buffered Rail-to-Rail Output Operation
- Safe Power-On Reset (POR) to Zero DAC Output
- Fast 30MHz, 3-Wire, SPI/QSPI/MICROWIRE-Compatible Serial Interface
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- SYNC Interrupt Facility
- High Performance Drop-In Compatible With TLV5614
- Available in TSSOP-16 Package

Applications

- Gain and Offset Adjustment
- Process Control and Servo Loops
- Programmable voltage and current sources
- Programmable attenuators
- Automatic Test Equipment

Package Information (Top View)



Description

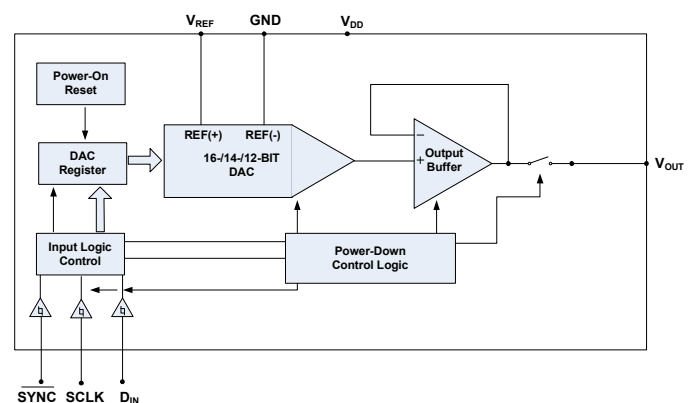
The TPC116S4/TPC112S4 are pin compatible 16-bit and 12-bit digital-to-analog converter, these series product are four channels, low power, buffered voltage-out DACs and are guaranteed monotonic by design. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption.

The TPC116S4/ TPC112S4 accepts a wide 2.7V to 5.5V supply voltage range. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place.

The TPC116S4/ TPC112S4 on-chip precision output amplifier allows rail-to-rail output swing to be achieved. For remote sensing applications, the output amplifier's inverting input is available to the user. The TPC116S4/ TPC112S4 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The TPC116S4/ TPC112S4 are available in a small size 16-pin TSSOP package, all package are specified over the -40°C to +125°C extended industrial temperature range.

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Block diagram of one DAC

Order Information

TPC116S4/ TPC112S4

Quad 16-/12-Bit, Low Power, High Performance DACs

| Model Name | Order Number | Package | Transport Media, Quantity | Marking Information |
|------------|--------------|--------------|---------------------------|---------------------|
| TPC112S4 | TPC112S4-TR | 16-Pin TSSOP | Tape and Reel, 3,000 | 112S4 |
| TPC116S4* | TPC116S4-TR | 16-Pin TSSOP | Tape and Reel, 3,000 | 116S4 |

* Sample is not ready, can be provided in 2 months.

Absolute Maximum Ratings Note 1

| | |
|--|--|
| Supply Voltage: $V^+ - V^-$ <small>Note 2</small>7.0V | Operating Temperature Range.....-40°C to 125°C |
| Input Voltage..... $V^- - 0.3$ to $V^+ + 0.3$ | Maximum Junction Temperature..... 150°C |
| Input Current: +IN, -IN <small>Note 3</small> ± 20 mA | Storage Temperature Range..... -65°C to 150°C |
| Output Short-Circuit Duration <small>Note 4</small> Indefinite | Lead Temperature (Soldering, 10 sec) 260°C |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|--------|--------------------------|----------------------------|---------------|------|
| HBM | Human Body Model ESD | MIL-STD-883H Method 3015.8 | 8 | kV |
| CDM | Charged Device Model ESD | JEDEC-EIA/JESD22-C101E | 2 | kV |

Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|--------------|---------------|---------------|------|
| 16-Pin TSSOP | 180 | 35 | °C/W |

Quad 16-/12-Bit, Low Power, High Performance DACs

Electrical Characteristics

($V_{DD} = 5V$, $V_{REF} = 5V$, $C_L = 100pF$, $R_L = 10k\Omega$, $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------------------|---------------------------------|------|------------|---------------|----------------------|
| STATIC ACCURACY (Note 5) | | | | | | |
| N | Resolution | TPC112S4 | 12 | | | Bits |
| | | TPC116S4 | 16 | | | |
| INL | Integral Nonlinearity | TPC112S4 (12-bit) (Note 6) | -2 | ± 0.25 | 2 | LSB |
| | | TPC116S4 (16-bit) (Note 6) | -16 | ± 8 | 16 | |
| DNL | Differential Nonlinearity | TPC112S4 (12-bit) (Note 6) | -1 | ± 0.05 | 1 | LSB |
| | | TPC116S4 (16-bit) (Note 6) | -1 | ± 0.5 | 1 | |
| OE | Zero Offset Error | | | 6.5 | 12 | mV |
| | Full-Scale Offset Error | | -10 | 0 | 10 | mV |
| | Offset-Error Drift | | | ± 1 | | $\mu V/^\circ C$ |
| GE | Gain Error | | -0.3 | ± 0.13 | 0.3 | %FS |
| | Gain Temperature Coefficient | | | ± 2 | | ppmFS/ $^\circ C$ |
| REFERENCE INPUT | | | | | | |
| V_{REF} | Reference-Input Voltage Range | | 0.5 | | V_{DD} | V |
| R_{REF} | Reference-Input Impedance | | | 333 | | k Ω |
| DAC OUTPUT | | | | | | |
| | Output Voltage Range | No load (typical) | | | V_{REF} | V |
| | | 10 k Ω load | 0.2 | | $V_{REF}-0.1$ | |
| | DC Output Impedance | | | 0.1 | | Ω |
| C_L | Capacitive Load (Note 8) | Series resistance = 0 Ω | | | 0.1 | nF |
| | | Series resistance = 1k Ω | | | 15 | μF |
| R_L | Resistive Load (Note 8) | | 5 | | | k Ω |
| | Short-Circuit Current | $V_{DD} = 5.5V$ | | 35 | | mA |
| | Power-Up Time | From power-down mode | | 25 | | μs |
| DIGITAL INPUTS (SCLK, DIN, SYNC) | | | | | | |
| V_{IH} | Input High Voltage | $V_{DD} = 5V$ | 2 | | | V |
| | | $V_{DD} = 3.3V$ | 1.5 | | | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 5V$ | | | 0.6 | V |
| | | $V_{DD} = 3.3V$ | | | 0.4 | V |
| I_{IN} | Input Leakage Current | $V_{IN} = 0V$ or V_{DD} | | ± 5 | ± 10 | μA |
| C_{IN} | Input Capacitance | | | 1 | | pF |

Electrical Characteristics(continued)

($V_{DD} = 5V$, $V_{REF} = 5V$, $C_L = 100pF$, $R_L = 10k\Omega$, $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

Dual/Quad 36V Ultra Low Distortion OPAMP

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------------------|---|-----|------|-----|------------------------|
| V_{HYS} | Hysteresis Voltage | | | 0.15 | | V |
| DYNAMIC PERFORMANCE (Note 8) | | | | | | |
| SR | Voltage-Output Slew Rate | Positive and negative | | 1 | | V/ μ s |
| BW | Voltage-Output Settling Time | 1/4 scale to 3/4 scale, to ≤ 0.5 LSB, 12-bit | | 14 | | μ s |
| | Reference -3dB Bandwidth | Hex code = 800 (TPC112S4), Hex code = 8000 (TPC116S4) | | 100 | | kHz |
| | Digital Feedthrough | Code = 0, all digital inputs from 0V to VDD, SCLK < 50MHz | | 0.5 | | nV \cdot s |
| | DAC Glitch Impulse | Major code transition | | 2 | | nV \cdot s |
| | Output Noise | 10kHz | | 90 | | nV/ \sqrt Hz |
| | Integrated Output Noise | 0.1Hz to 10Hz | | 25 | | μ V _{P-P} |
| POWER REQUIREMENTS | | | | | | |
| V_{DD} | Supply Voltage | | 2.7 | | 5.5 | V |
| I_{DD} | Supply Current | $V_{DD} = 5V$, No load; all digital inputs at 0V or V_{DD} , supply current only; excludes reference input current, midscale | | 0.8 | 1.5 | mA |
| I_{DD} | Supply Current | $V_{DD} = 3.3V$, No load; all digital inputs at 0V or V_{DD} , supply current only; excludes reference input current, midscale | | 0.5 | 1 | mA |
| | Power-Down Supply Current | No load, all digital inputs at 0V or V_{DD} | | | 500 | μ A |

Note 5: Linearity is tested within 20mV of GND and V_{DD} .

Note 6: Gain and offset is tested within 100mV of GND and V_{DD} .

Note 7: Guaranteed by design; not production tested.

Note 8: All timing specifications measured with $V_{IL} = V_{GND}$, $V_{IH} = V_{DD}$.

Quad 16-/12-Bit, Low Power, High Performance DACs

Serial Write Operation

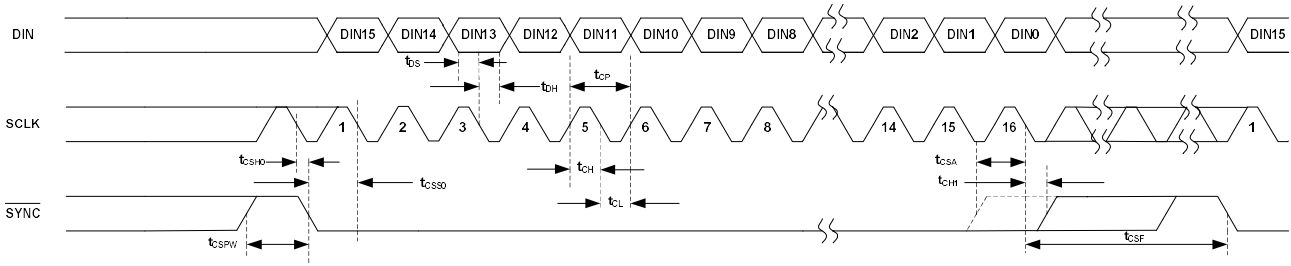


Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S4)

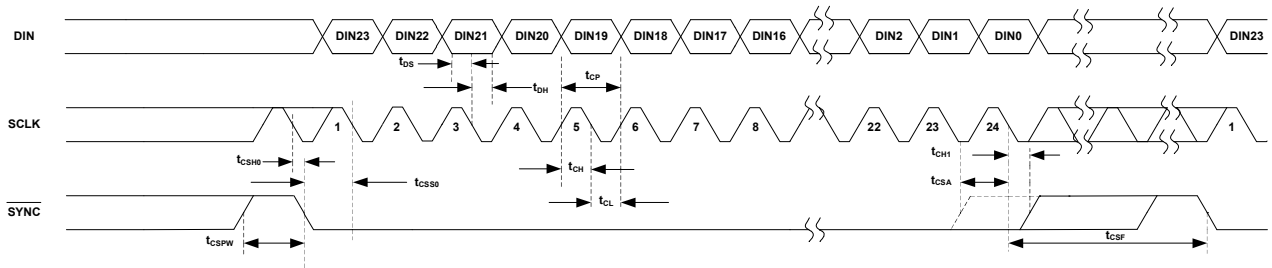


Figure 2. 24-Bit Serial-Interface Timing Diagram (TPC116S4)

| TIMING CHARACTERISTICS (Figures 1,2 and 3) | | | | | | |
|--|-----------------------------------|------------|-----|-----|-----|-------|
| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| f_{SCLK} | Serial Clock Frequency | | 0 | | 30 | MHz |
| t_{CH} | SCLK Pulse-Width High | | 8 | | | ns |
| t_{CL} | SCLK Pulse-Width Low | | 8 | | | ns |
| t_{CSS0} | SYNC Fall to SCLK Fall Setup Time | | 8 | | | ns |
| t_{SSH0} | SYNC Fall to SCLK Fall Hold Time | | 0 | | | ns |
| t_{SSH1} | SYNC Rise to SCLK Fall Hold Time | | 0 | | | ns |
| t_{CSA} | SYNC Rise to SCLK Fall | | | | 12 | ns |
| t_{CSF} | SCLK Fall to SYNC Fall | | 100 | | | ns |
| t_{DS} | DIN to SCLK Fall Setup Time | | 5 | | | ns |
| t_{DH} | DIN to SCLK Fall Hold Time | | 4.5 | | | ns |
| t_{CSPW} | SYNC Pulse-Width High | | 20 | | | ns |
| t_{CLPW} | SYNC Pulse-Width Low | | 20 | | | ns |
| t_{CSC} | SYNC Rise to SYNC Fall | | 20 | | | ns |

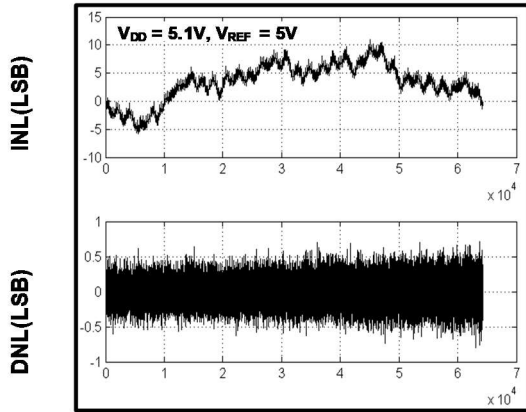
TPC116S4/ TPC116S4

Quad 16-/12-Bit, Low Power, High Performance DACs

Typical Performance Characteristics

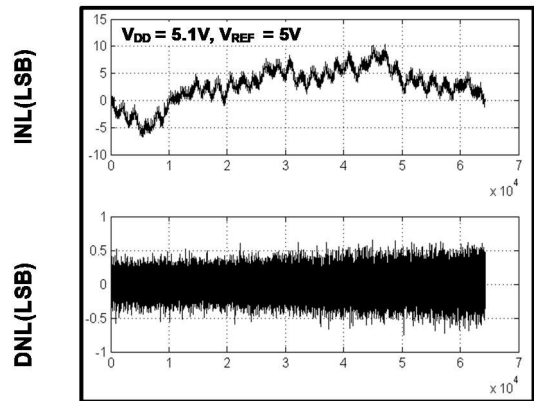
$V_S = 5V$, At $T_A = +25^\circ C$, unless otherwise specified

INL and DNL vs. Digital Input Code(+25°C TPC116S4)



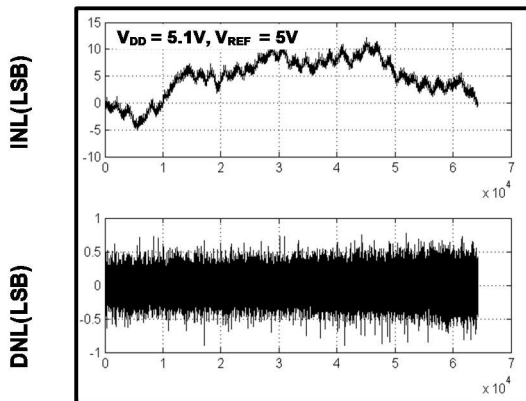
Digital Input Code

INL and DNL vs. Digital Input Code(-40°C TPC116S4)



Digital Input Code

INL and DNL vs. Digital Input Code(+105°C TPC116S4)



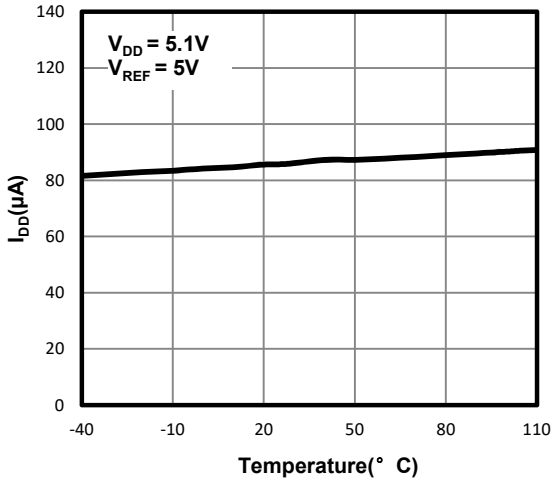
Digital Input Code

Quad 16-/12-Bit, Low Power, High Performance DACs

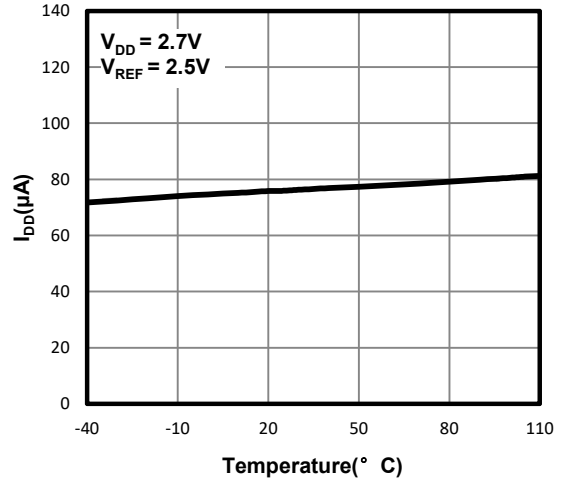
Typical Performance Characteristics

$V_S = 5V$, At $T_A = +25^\circ C$, unless otherwise specified

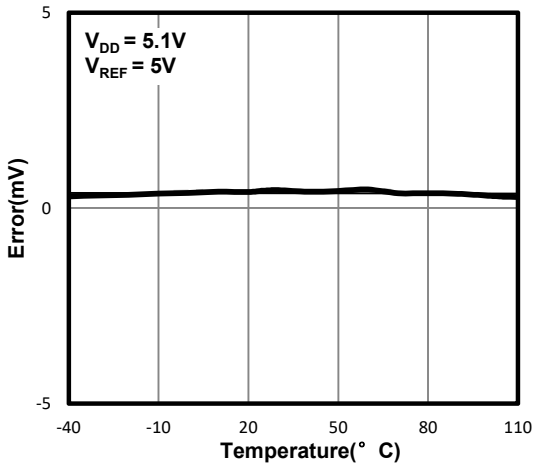
Power-Supply Current vs. Temperature(TPC116S4)



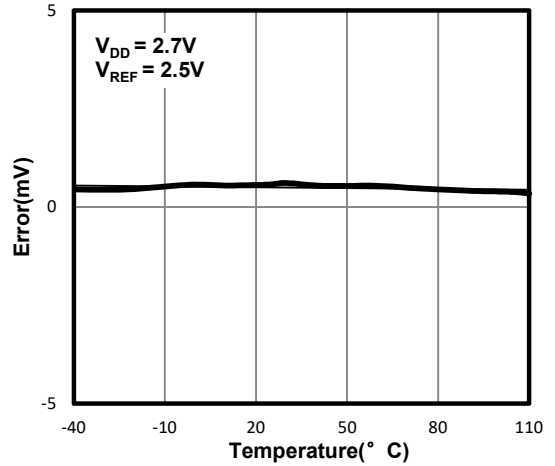
Power-Supply Current vs. Temperature(TPC116S4)



Zero-Scale Error vs. Temperature(TPC116S4)



Zero-Scale Error vs. Temperature(TPC116S4)

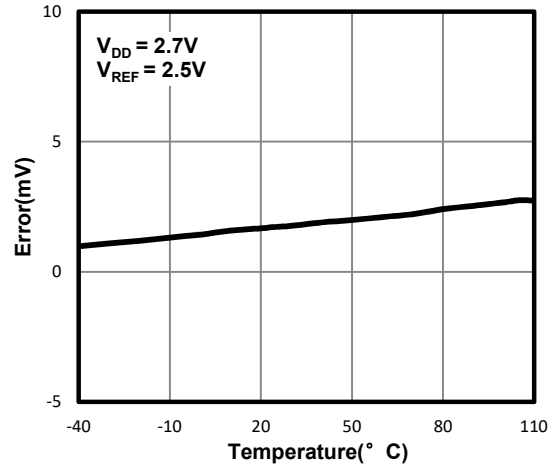
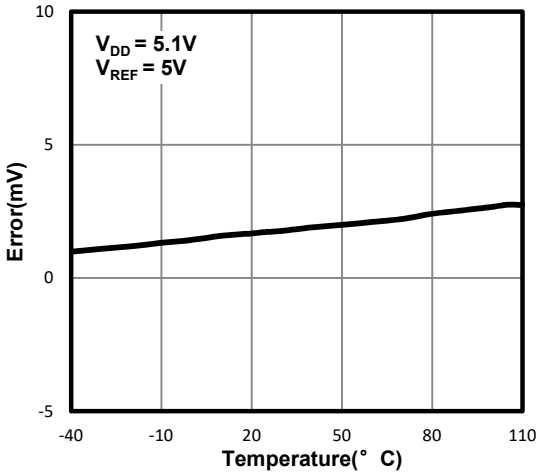


Full-Scale Error vs. Temperature(TPC116S4)

Full-Scale Error vs. Temperature(TPC116S4)

TPC116S4/ TPC116S4

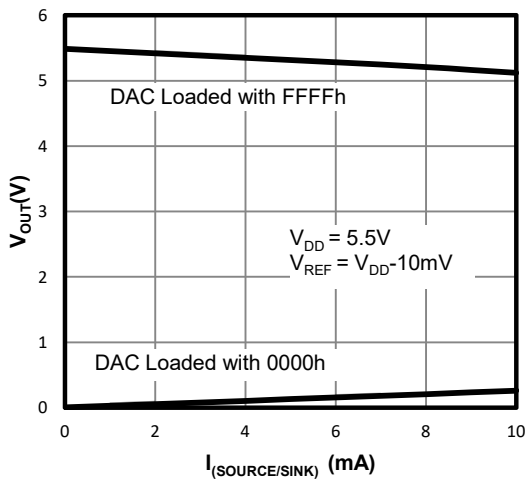
Quad 16-/12-Bit, Low Power, High Performance DACs



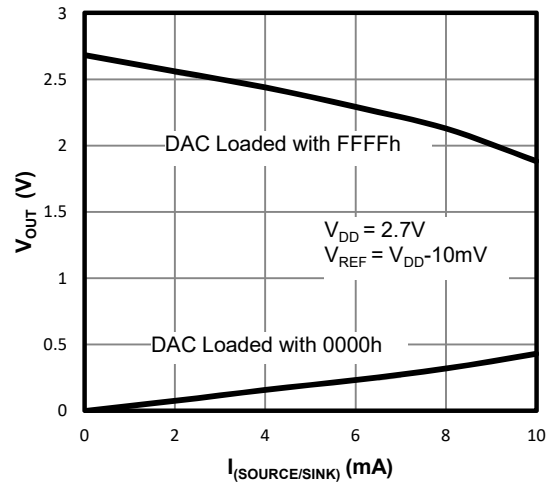
Typical Performance Characteristics

$V_S = 5V$, At $T_A = +25^\circ C$, unless otherwise specified

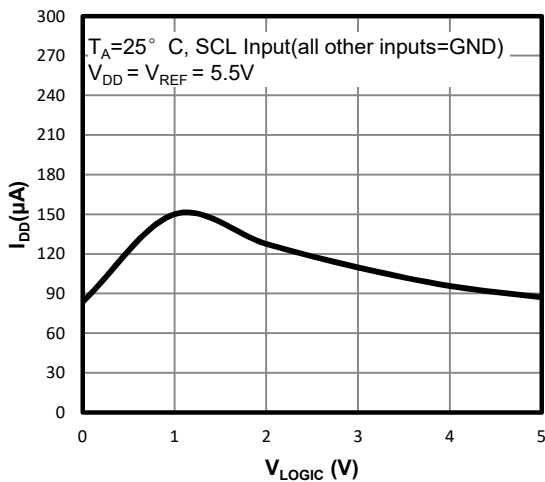
Source and Sink Current Capability(TPC116S4)



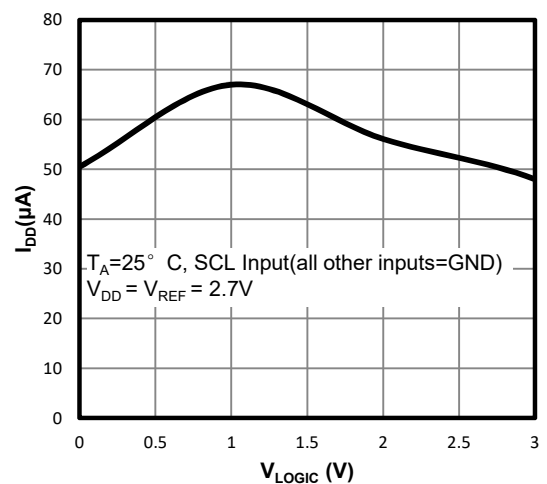
Source and Sink Current Capability(TPC116S4)



Supply Current vs. Logic Input Voltage(TPC116S4)

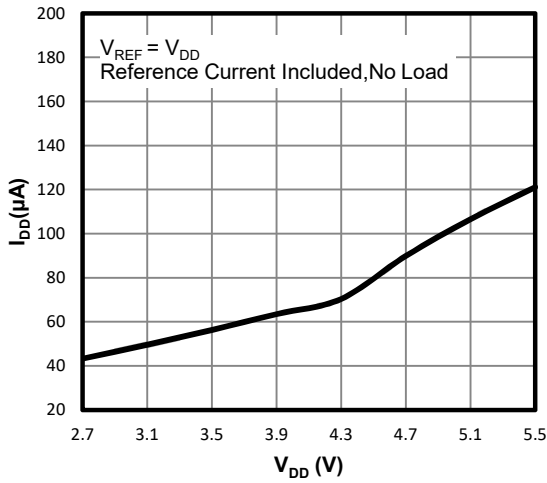


Supply Current vs. Logic Input Voltage(TPC116S4)

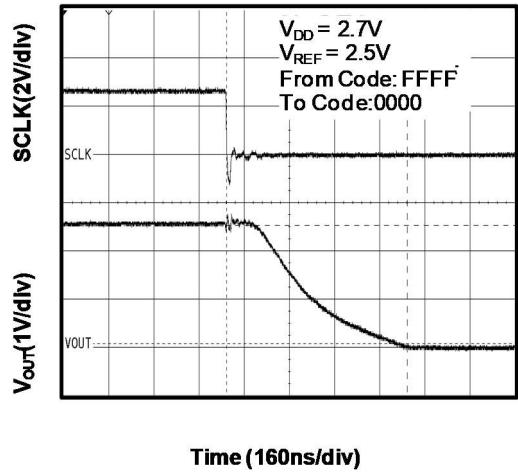


Quad 16-/12-Bit, Low Power, High Performance DACs

Supply Current vs. Supply Voltage(TPC116S4)



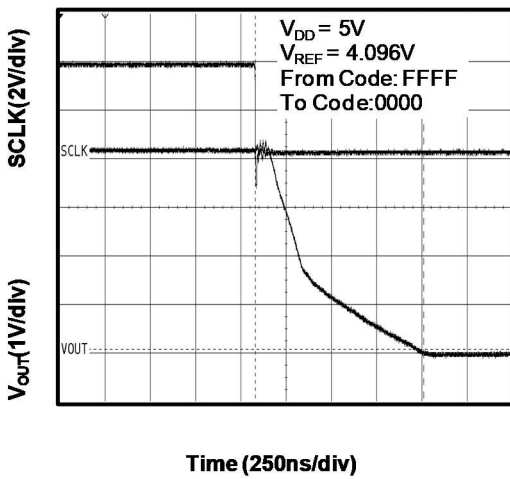
Full-Scale Settling Time(2.7V Falling Edge)



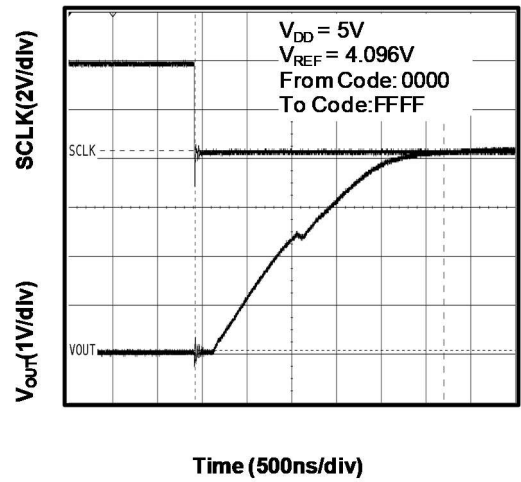
Typical Performance Characteristics

V_S = 5V, At T_A = +25°C, unless otherwise specified

Full-Scale Settling Time(5V Falling Edge)



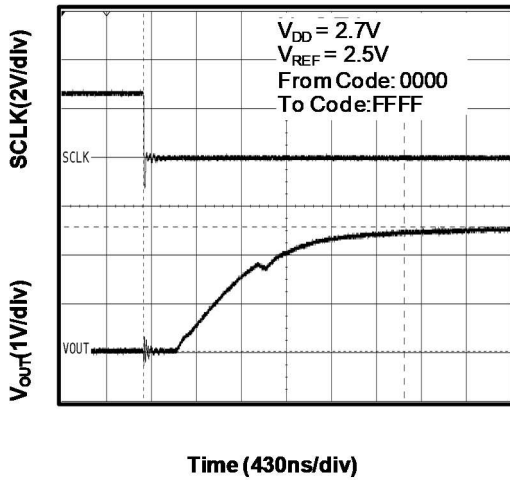
Full-Scale Settling Time(5V Rising Edge)



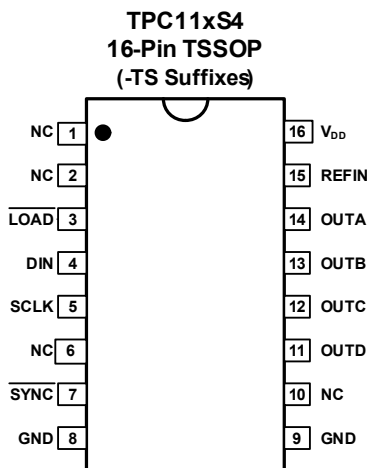
Full-Scale Settling Time(2.7V Rising Edge)

TPC116S4/ TPC116S4

Quad 16-/12-Bit, Low Power, High Performance DACs



Pin Functions



| PIN number | PIN name | Function |
|------------|----------|--|
| 1 | NC | Not connect |
| 2 | NC | Not connect |
| 3 | LOAD | Load DAC. When the LOAD signal is high, no DAC output updates occur when the input |

Quad 16-/12-Bit, Low Power, High Performance DACs

| | | |
|----|--------------------------|---|
| | | digital data is read into the serial interface. The DAC outputs are only updated when LDAC is low. |
| 4 | DIN | Serial data input. Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input. |
| 5 | SCLK | Serial clock input. Data can be transferred at rates up to 30MHz. Schmitt-Trigger logic input. |
| 6 | NC | Not connect |
| 7 | $\overline{\text{SYNC}}$ | Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. |
| 8 | GND | Ground reference point for all circuitry on the part. |
| 9 | GND | Ground reference point for all circuitry on the part. |
| 10 | NC | Not connect |
| 11 | OUTD | DACD output |
| 12 | OUTC | DACC output |
| 13 | OUTB | DACB output |
| 14 | OUTA | DACA output |
| 15 | REFIN | Reference voltage input |
| 16 | VDD | Power supply input, 2.7V to 5.5V |

TPC116S4/ TPC112S4

Quad 16-/12-Bit, Low Power, High Performance DACs

Detailed Description

The TPC116S4/TPC112S4 are pin-compatible and software-compatible 12-bit and 16-bit DACs. The TPC116S4/TPC112S4 are 4-channels, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S4/TPC112S4 minimize the digital noise feed through from their inputs to their outputs by powering down the SCLK and DIN input buffers after completion of each data frame. The data frames are 16-bit for the TPC112S4 and 24-bit for the TPC116S4. On power-up, the TPC116S4/TPC112S4 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The TPC116S4/TPC112S4 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

Applications Information

DAC Reference (REF)

The external reference input features a typical input impedance of 333kΩ and accepts an input voltage from +2V to VDD. Connect an external voltage supply between REF and GND to apply an external reference.

Serial Interface

The TPC116S4/TPC112S4 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, SYNC, and DIN. The chip-select input (SYNC) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16-bit for the TPC112S4 and 24-bit for the TPC116S4. The first 3 bits are the control bits followed by 1 power-down bit as well as 12 data bits (MSB first) for the TPC112S4 and 22 data bits (MSB first) for the TPC116S4 as shown in Tables 1 and 2. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, drive SYNC high and keep SYNC high for a minimum of 20ns before the next write sequence. The SCLK can be either high or low between SYNC write pulses. Figures 1 and 2 show the timing diagram for the complete 3-wire serial interface transmission. The TPC116S4 DAC code is unipolar binary with $V_{OUT} = (\text{code}/65,536) \times V_{REF}$. The TPC112S4 DAC code is unipolar binary with $V_{OUT} = (\text{code}/4096) \times V_{REF}$.

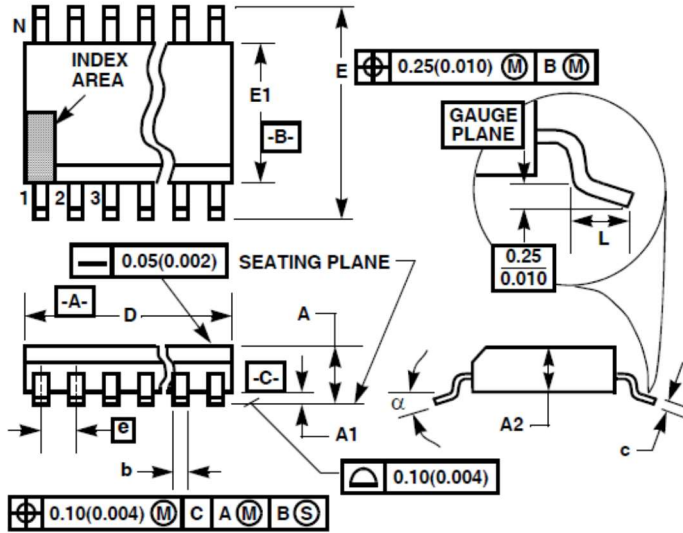
| 16-BIT WORD | | | | | | | | | | | | | | | | Function |
|-------------|-----|-----|-----|--------------|-----|----|----|----|----|----|----|----|----|----|----|-------------------|
| A2 | A1 | A0 | PD | DAC Data Bit | | | | | | | | | | | | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | Update DAC A Data |
| 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | Update DAC B Data |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | Update DAC C Data |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | Update DAC D Data |
| X | X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | Power down |

Table 1. Operating Mode Truth Table (TPC112S4)

Package Outline Dimensions

Quad 16-/12-Bit, Low Power, High Performance DACs

TSSOP-16



| Symbol | Dimensions In Millimeters | | |
|----------|------------------------------|------|------|
| | MIN | NOM | MAX |
| A | - | 0.55 | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.90 | 0.95 |
| b | 0.19 | 0.25 | 0.30 |
| c | 0.09 | 0.15 | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.25 | 6.38 | 6.5 |
| L | 0.50 | 0.60 | 0.70 |
| N | 16 | | |
| e | 0.65 BSC | | |
| α | 0° | 4° | 8° |