24-Bit, 32-kSPS, 4-Channel Sigma-Delta ADC with Internal Reference and Temperature Sensor

Features

- 24-Bit, 32 kSPS, 4-Channel ADC
- Wide Supply Range: 2.7 V to 5.5 V
- Programmable Data Rate:
  - 64 SPS to 32 kSPS
- Single-Cycle Settling
- Supporting Four Single-Ended or Two Differential Inputs
- Internal PGA
- Optional Global Chop Mode
- Internal Low-Drift Voltage Reference
- Internal Temperature Sensor
- SPI Compatible Interface
- Package: MSOP10 3 mm x 3 mm
- Wide Operating Temperature Range: −40°C to +125°C

Applications

- Current-shunt Measurements
- Voltage Measurements
- Industrial Automation
- Temperature Measurements

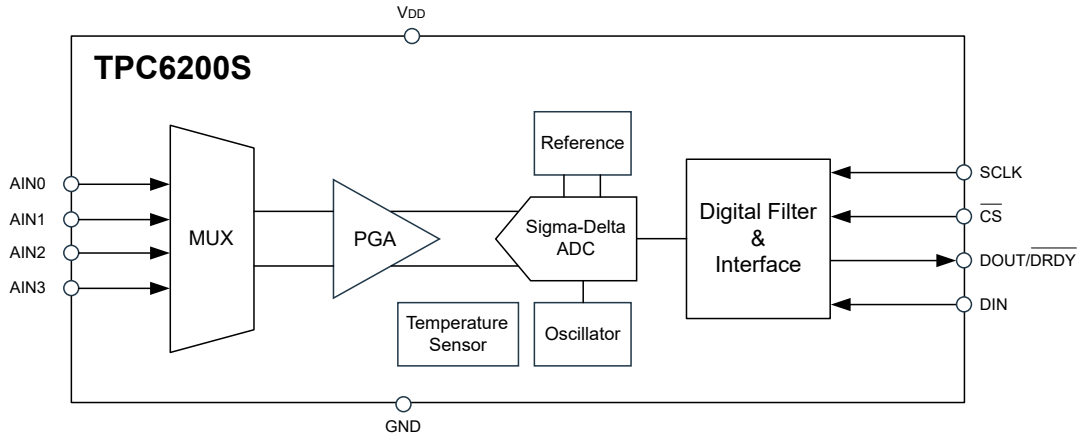
Description

The TPC6200S is a 24-bit Sigma-Delta ADC for high precision and low power measurement. The TPC6200S features an internal programmable gain amplifier(PGA), voltage reference, oscillator, digital filter, and temperature sensor. The device supports a wide range of supply voltage from 2.7 V to 5.5 V.

The data rate of TPC6200S is configurable from 64 SPS to 32 kSPS. The PGA provides input ranges spanning from ±256 mV to ±6.144 V, with the analog input negative voltage down to −128 mV, which allows both high precision positive and negative signal measurement. The integrated input mux supports two differential pairs or four independent single-ended inputs. The internal temperature sensor can be used for general temperature monitoring or thermal couple cold-junction compensation.

The TPC6200S can be set in single-shot conversion mode or continuous conversion mode. The single-shot mode features power down after a conversion, which is suitable for low-power applcaitions. The digital interface supports communication with various host controllers with SPI-compatible serial interface. The TPC6200S is available in an MSOP10 package and operating from −40°C to +125°C.

Functional Block Diagram



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Product Family Table

Order Number	Channels	Resolution	Throughput	Package	Interface
TPC6200S-VS2R	4	24 Bits	32 kSPS	MSOP10	SPI

Revision History

Date	Revision	Notes
2025-02-28	Rev.A.0	Initial release.

Pin Configuration and Functions

TPC6200S
MSOP10 Package
Top View

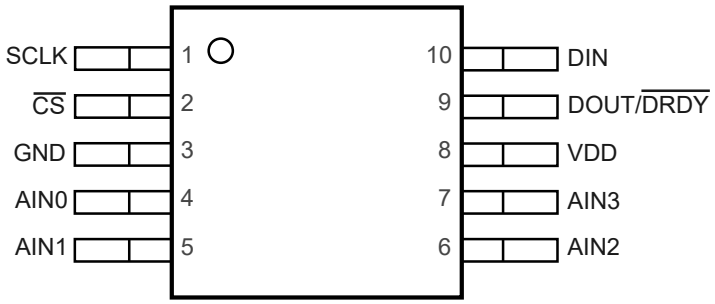


Table 1. Pin Functions: TPC6200S

Pin		Type (1)	Description
No.	Name		
1	SCLK	DI	Serial clock input. This pin acts as the serial clock input for data transfers.
2	$\overline{CS}$	DI	Chip Select. This active low-logic input frames the data transfer. If not used, connect this pin to GND.
3	GND	P	Ground.
4	AIN0	AI	Analog Input for Channel 0. If not used, float this pin or tie to VDD.
5	AIN1	AI	Analog Input for Channel 1. If not used, float this pin or tie to VDD.
6	AIN2	AI	Analog Input for Channel 2. If not used, float this pin or tie to VDD.
7	AIN3	AI	Analog Input for Channel 3. If not used, float this pin or tie to VDD.
8	VDD	P	Power supply. Connect a 0.1 μF power supply decoupling capacitor to GND.
9	DOUT/$\overline{DRDY}$	DO	Serial data output combined with data ready; active low.
10	DIN	DI	Serial data input.

(1) AI is an analog input, GND is ground, P is power supply, DI is digital input, and DO is digital output.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage to GND	GND − 0.3	VDD + 0.3	V
Digital Voltage	Digital Input Voltage to AGND	GND − 0.3	VDD + 0.3	V
	Digital Output Voltage to AGND	GND − 0.3	VDD + 0.3	V
Supply Voltage	VDD to GND	−0.3	5.5	V
Input current (continuous)	Any Pin except Power Supply Pins	−10	10	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Typ	Max	Unit
VDD	Power Supply	VDD to GND	2.7		5.5	V
FSR	Full-scale Input Voltage (1)	VIN = $V_{(AINP)}$ - $V_{(AINN)}$	±0.256		±6.144	V
$V_{(AINx)}$	Absolute Input Voltage		−0.128		VDD	V
Digital input Voltage	Absolute Input Voltage		GND		VDD	V
T_A	Operating Ambient Temperature		−40		125	℃

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	125	48	°C/W

Electrical Characteristics

All test conditions: VDD = 3.3 V, data rate = 1.024 kSPS, and FSR = ±2.048 V. T_A = −40 °C to 125 °C, unless otherwise noted.

Parameter	Test Conditions		Min	Typ	Max	Unit
Analog Inputs						
Common-mode Input Impedance	FSR = ±6.144 V (1)			1.7		MΩ
	FSR = ±4.096 V (1)			0.87		MΩ
	FSR = ±2.048 V			0.51		MΩ
	FSR = ±1.024 V			0.54		MΩ
	FSR = ±0.512 V			0.26		MΩ
	FSR = ±0.256 V			0.26		MΩ
Differential Input Impedance	FSR = ±6.144 V (1)			0.74		MΩ
	FSR = ±4.096 V (1)			0.37		MΩ
	FSR = ±2.048 V			0.19		MΩ
	FSR = ±1.024 V			0.11		MΩ
	FSR = ±0.512 V			0.068		MΩ
	FSR = ±0.256 V			0.068		MΩ
System Performance						
Resolution	No missing code		24			Bits
DR	Data rate		64, 128, 256, 512, 1024, 2000, 4000, 8000, 16000, 32000			SPS
	Data rate variation	All data rates	− 10%		10%	
INL	Integral nonlinearity	DR = 64 SPS, FSR = ±2.048 V	−35	±8	35	ppm
Offset Error	FSR = ±2.048 V, differential inputs		−0.2	0.056	0.2	mV
Offset Drift	FSR = ±2.048 V			0.6		μV/℃
Offset Power-supply Rejection	FSR = ±2.048 V, DC supply variation			1500		LSB/V
Offset Channel Match	Match between any two inputs			232		LSB
Gain Error	FSR = ±2.048 V, T_A = 25 °C			0.05%	0.15%	
Gain Drift (2)	FSR = ±0.256 V			3.7		ppm/℃
	FSR = ±2.048 V			3.7	10	ppm/℃
	FSR = ±6.144 V (1)			3.7		ppm/℃
Gain Match	Match between any two gains			0.05%	0.1%	
Gain Channel Match	Match between any two inputs			0.01%	0.1%	
CMRR	Common-mode rejection ration	At DC, FSR = ±0.256 V		126		dB
		At DC, FSR = ±2.048 V		115		dB

Parameter	Test Conditions		Min	Typ	Max	Unit
		At DC, FSR = ±6.144 V (1)		108		dB
		f_{CM} = 50 Hz, DR = 32 kSPS		114		dB
		f_{CM} = 60 Hz, DR = 32 kSPS		113		dB
Temperature Sensor						
Temperature Range			−40		+125	℃
Temperature Resolution	14-bit			0.03125		℃/LSB
Accuracy	T_A = −40℃ to 125℃			±3		℃
	vs supply			±1		℃/V
Digital Input/Outputs						
V_{IH}	High-level input voltage		0.7 x VDD		VDD	V
V_{IL}	Low-level input voltage		GND		0.2 x VDD	V
V_{OH}	I_{SOURCE} = 1 mA		0.8 x VDD			V
V_{OL}	I_{SINK} = 1 mA		GND		0.2 x VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	−10		10	μA
I_L	Input leakage, low	V_{IL} = GND	−10		10	μA
Power Supply						
I_{VDD}	Supply current	Power-down, VDD = 5 V T_A = 25°C		4.6	10	μA
		Power-down, VDD = 3.3 V T_A = 25°C		4.6	7	μA
		Operating		4	5.5	mA
P_D	Power dissipation	VDD = 5 V		20		mW
Temperature Range	Specified performance		−40		+125	℃

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

(2) Maximum value specified by characterization.

Timing Specifications (1)

All test conditions: VDD = 2.7 V to 5.5 V and T_A = −40 °C to 125 °C, unless otherwise noted.

Table 2. Serial Interface

Parameter	Description	Min	Typ	Max	Unit
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge (2)	100			ns
t_{SCCS}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	100			ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200			ns
t_{SCLK}	SCLK period	80			ns
t_{SPWH}	Pulse duration, SCLK high	100			ns
t_{SPWL}	Pulse duration, SCLK low (3)	100			ns
				30.8	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	20			ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge		700	800	ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	200			ns

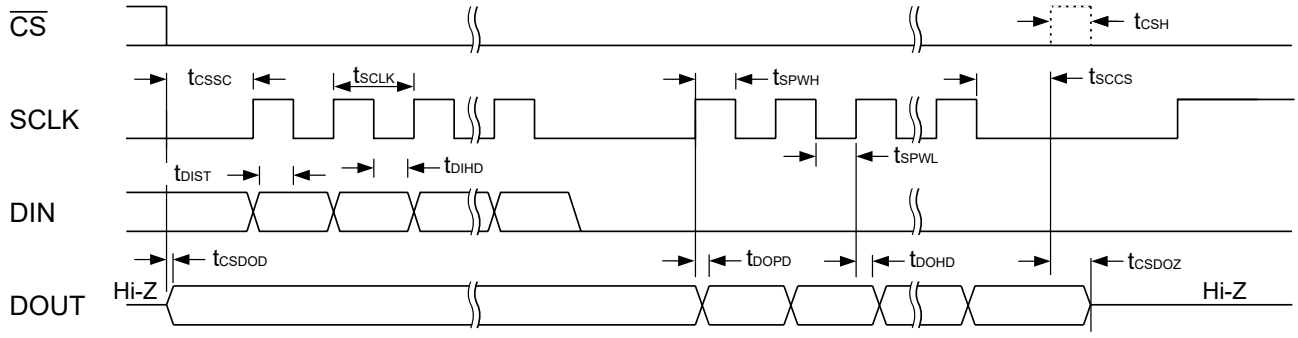


Figure 1. Serial Interface Timing

Table 3. Switching Characteristics: Serial Interface

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 100 kΩ to GND			100	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to GND	0		50	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 100 kΩ to GND			100	ns

(1) Parameters are provided by design simulation.
(2) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(3) Holding SCLK low longer than 30.8 ms resets the SPI interface. If $\overline{CS}$ is holding low meanwhile SCLK holding low longer than 30.8ms, the output code is also reset to 0.

Typical Performance Characteristics

All test conditions: T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V, DR = 64 SPS, unless otherwise noted.

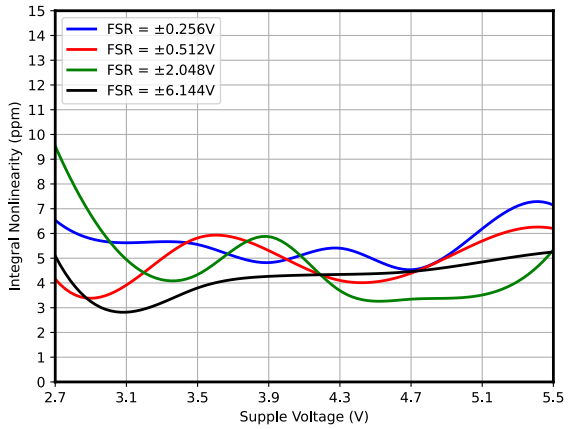
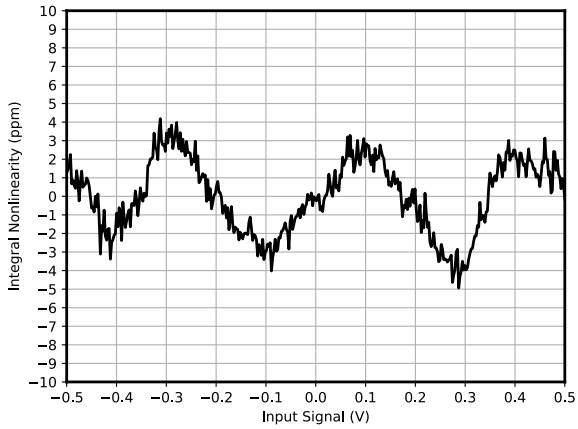
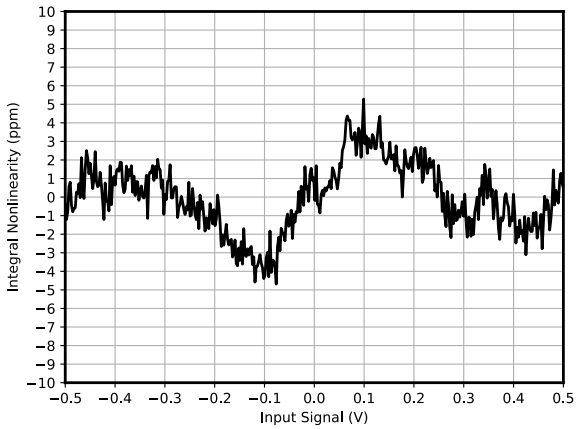


Figure 2. INL vs. Supply Voltage



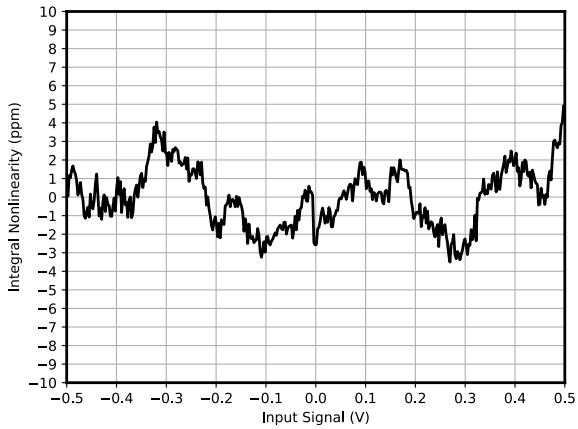
VDD = 3.3 V, FSR = ±0.512 V, DR = 64 SPS, best fit

Figure 3. INL vs. Input Signal



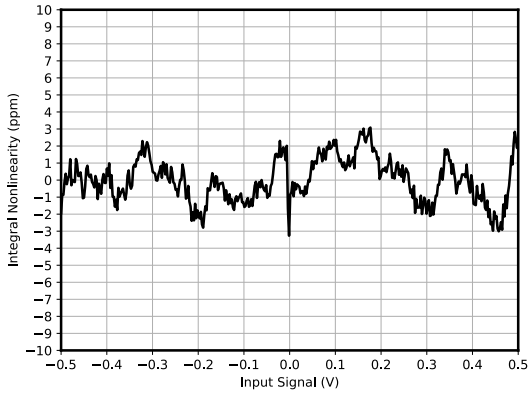
VDD = 5.0 V, FSR = ±0.512 V, DR = 64 SPS, best fit

Figure 4. INL vs. Input Signal



VDD = 3.3 V, FSR = ±2.048 V, DR = 64 SPS, best fit

Figure 5. INL vs. Input Signal



VDD = 5.0 V, FSR = ±2.048 V, DR = 64 SPS, best fit

Figure 6. INL vs. Input Signal

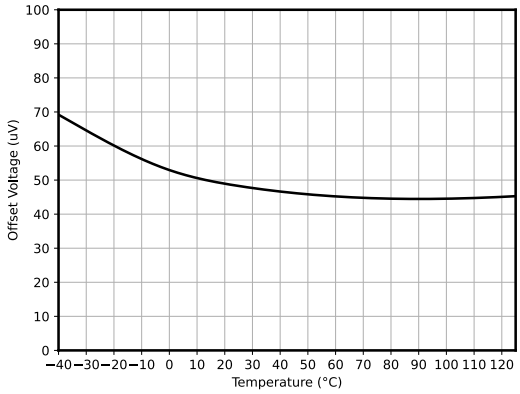


Figure 7. Differential Offset Voltage vs. Temperature

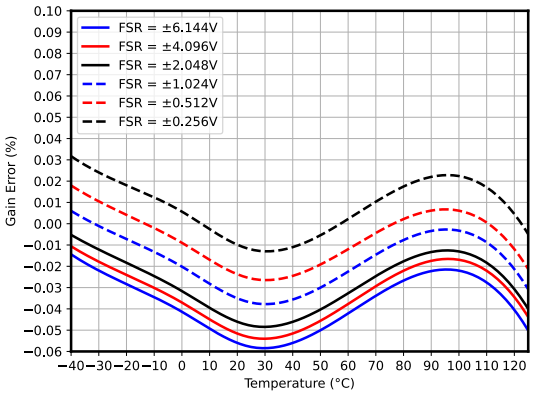
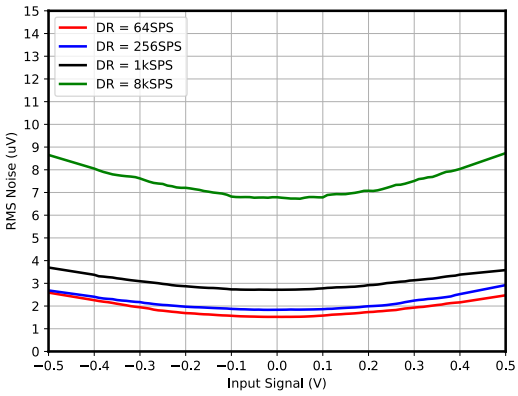
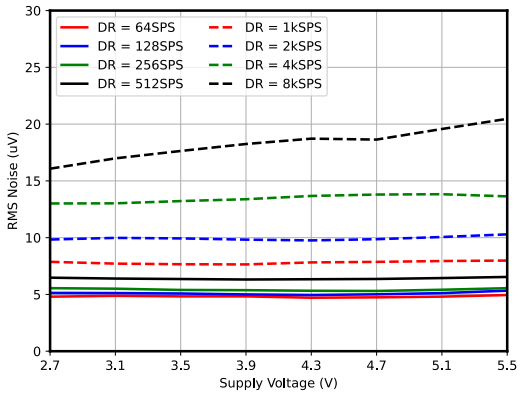


Figure 8. Gain Error vs. Temperature



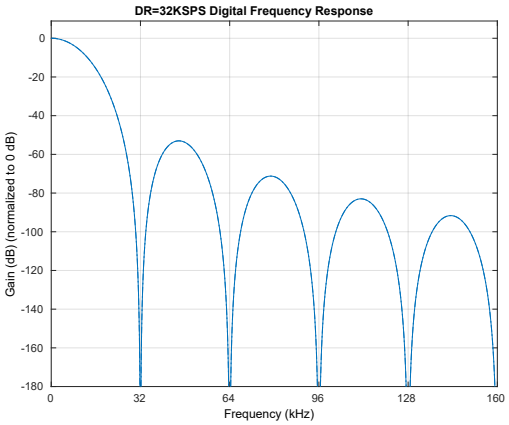
FSR = ±0.512 V

Figure 9. Noise vs. Input Signal



FSR = ±0.512 V

Figure 10. Noise vs. Supply Voltage



Provided by simulation results

Figure 11. Digital Filter Frequency Response

Noise Performance

The Sigma-Delta (ΣΔ) ADC architecture operates based on oversampling principles. In this approach, the input signal is sampled at a high frequency, known as the modulator frequency. The sampled signal is then processed through filtering and decimation in the digital domain, resulting in the final conversion output at a specified data rate. The oversampling ratio (OSR), which is the ratio between the modulator frequency and the output data rate, plays a crucial role. By increasing the OSR, and consequently lowering the output data rate, the noise performance of the ADC can be optimized. This is achieved by averaging more samples of the internal modulator, thereby reducing input-referred noise. Additionally, increasing the gain proves beneficial for measuring low-level signals as it further contributes to the reduction of input-referred noise.

The following tables provide an overview of the noise performance of the device, with data representative of typical noise characteristics at a temperature of 25°C and the inputs externally shorted together. Table 4 and Table 5 display the input-referred noise in units of microvolts root mean square (μVRMS), with microvolts peak-to-peak (μVPP) values shown in parentheses. Table 6 and Table 7 present the corresponding data in terms of effective number of bits (ENOB), calculated from μVRMS values using Equation 1. The noise-free bits, determined from peak-to-peak noise values using Equation 2, are enclosed in parentheses.

$$ENOB = \ln(FSR/V_{RMS-Noise})/\ln(2) \quad (1)$$

$$Noise-Free\ Bits = \ln(FSR/V_{PP-Noise})/\ln(2) \quad (2)$$

Table 4. Noise in μVRMS at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	13.02	8.83	4.52	2.31	1.36	1.04
128	13.98	9.5	4.75	2.49	1.5	1.11
256	16.38	10.57	5.34	2.94	1.71	1.3
512	18.94	12.03	6.48	3.42	2.07	1.51
1024	22.93	14.79	7.44	4.13	2.43	1.92
2k	29.28	18.25	9.57	5	3.14	2.33
4k	37.7	24.38	12.62	6.74	4.11	3.16
8k	49.34	34.42	16.72	8.76	5.65	4.46
16k	30.38	19.55	9.82	5.6	3.37	2.61
32k	48.29	26.57	15.77	6.87	4.49	3.39

Table 5. Noise in μVPP at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	78.11	52.97	27.13	13.85	8.13	6.22
128	83.9	56.98	28.5	14.92	9.03	6.63
256	98.25	63.43	32.01	17.65	10.28	7.8
512	113.65	72.21	38.86	20.5	12.42	9.08
1024	137.6	88.72	44.66	24.75	14.61	11.52
2k	175.68	109.48	57.41	29.97	18.85	13.95

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
4k	226.19	146.29	75.74	40.42	24.64	18.98
8k	296.03	206.5	100.34	52.58	33.91	26.77
16k	182.29	117.3	58.92	33.63	20.21	15.65
32k	289.72	159.45	94.61	41.21	26.93	20.35

Table 6. ENOB from RMS Noise at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	19.85	19.82	19.79	19.76	19.53	18.91
128	19.75	19.72	19.72	19.65	19.38	18.82
256	19.52	19.56	19.55	19.41	19.19	18.59
512	19.31	19.38	19.27	19.19	18.92	18.37
1024	19.03	19.08	19.07	18.92	18.68	18.02
2k	18.68	18.78	18.71	18.65	18.31	17.75
4k	18.31	18.36	18.31	18.21	17.93	17.3
8k	17.93	17.86	17.9	17.83	17.47	16.81
16k	18.63	18.68	18.67	18.48	18.21	17.58
32k	17.96	18.23	17.99	18.19	17.8	17.2

Table 7. Noise-Free Bits from Peak-to-Peak Noise at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	17.26	17.24	17.2	17.17	16.94	16.33
128	17.16	17.13	17.13	17.07	16.79	16.24
256	16.93	16.98	16.97	16.82	16.6	16
512	16.72	16.79	16.69	16.61	16.33	15.78
1024	16.45	16.49	16.48	16.34	16.1	15.44
2k	16.09	16.19	16.12	16.06	15.73	15.16
4k	15.73	15.77	15.72	15.63	15.34	14.72
8k	15.34	15.28	15.32	15.25	14.88	14.22
16k	16.04	16.09	16.09	15.89	15.63	15
32k	15.37	15.65	15.4	15.6	15.21	14.62

Table 8. Noise in μVRMS at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	5.02	3.28	1.64	0.9	0.59	0.45
128	7.35	4.75	2.56	1.28	0.77	0.57
256	10.8	6.96	3.67	1.83	1.03	0.79
512	16.26	10.1	5.11	2.62	1.45	1.12
1024	22.83	13.92	7.44	3.82	2.08	1.66
2k	30.32	18.21	10.68	5.02	2.97	2.33
4k	38.96	22.82	13.64	6.76	3.83	3.16
8k	56.97	31.11	19.29	8.9	4.48	4.32
16k	55.33	34.1	18.39	8.97	5.65	3.65
32k	79.44	53.3	26.56	13.75	7.65	5.21

Table 9. Noise in μVPP at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	30.1	19.66	9.87	5.41	3.52	2.67
128	44.13	28.49	15.35	7.66	4.62	3.42
256	64.81	41.77	22	10.98	6.2	4.72
512	97.56	60.63	30.68	15.72	8.68	6.73
1024	136.99	83.51	44.63	22.9	12.49	9.99
2k	181.9	109.24	64.06	30.12	17.8	13.96
4k	233.78	136.9	81.85	40.59	23	18.94
8k	341.8	186.65	115.75	53.37	26.86	25.93
16k	331.98	204.62	110.33	53.81	33.91	21.9
32k	476.65	319.8	159.34	82.48	45.93	31.28

Table 10. ENOB from RMS Noise at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	21.22	21.25	21.25	21.11	20.73	20.13
128	20.67	20.72	20.61	20.61	20.34	19.78
256	20.12	20.17	20.09	20.09	19.92	19.31
512	19.53	19.63	19.61	19.58	19.43	18.8
1024	19.04	19.17	19.07	19.03	18.91	18.23
2k	18.63	18.78	18.55	18.64	18.4	17.75
4k	18.27	18.45	18.2	18.21	18.03	17.31

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8k	17.72	18.01	17.7	17.81	17.8	16.85
16k	17.76	17.87	17.77	17.8	17.47	17.1
32k	17.24	17.23	17.23	17.18	17.03	16.58

Table 11. Noise-Free Bits from Peak-to-Peak Noise at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	18.64	18.67	18.66	18.53	18.15	17.55
128	18.09	18.13	18.03	18.03	17.76	17.19
256	17.53	17.58	17.51	17.51	17.33	16.73
512	16.94	17.04	17.03	16.99	16.85	16.21
1024	16.45	16.58	16.49	16.45	16.32	15.65
2k	16.04	16.19	15.96	16.05	15.81	15.16
4k	15.68	15.87	15.61	15.62	15.44	14.72
8k	15.13	15.42	15.11	15.23	15.22	14.27
16k	15.18	15.29	15.18	15.22	14.88	14.51
32k	14.65	14.64	14.65	14.6	14.44	14

Detailed Description

Overview

The TPC6200S is a compact, low-power, 24-bit sigma-delta analog-to-digital converter (ADC) designed to minimize external circuitry and enhance performance. It incorporates a ΣΔ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI interface. Additionally, it integrates a precise temperature sensor. The ADC core measures a differential signal, VIN, representing the difference between V(AINP) and V(AINN). The core features a differential, switched-capacitor ΣΔ modulator followed by a digital filter, providing strong common-mode signal attenuation.

The device operates in single-shot or continuous-conversion modes, with single-shot mode saving power by performing one conversion upon request and entering a power-down state. In continuous-conversion mode, the ADC automatically initiates conversions, and data can be read at any time, reflecting the most recent completed conversion.

Functional Block Diagram

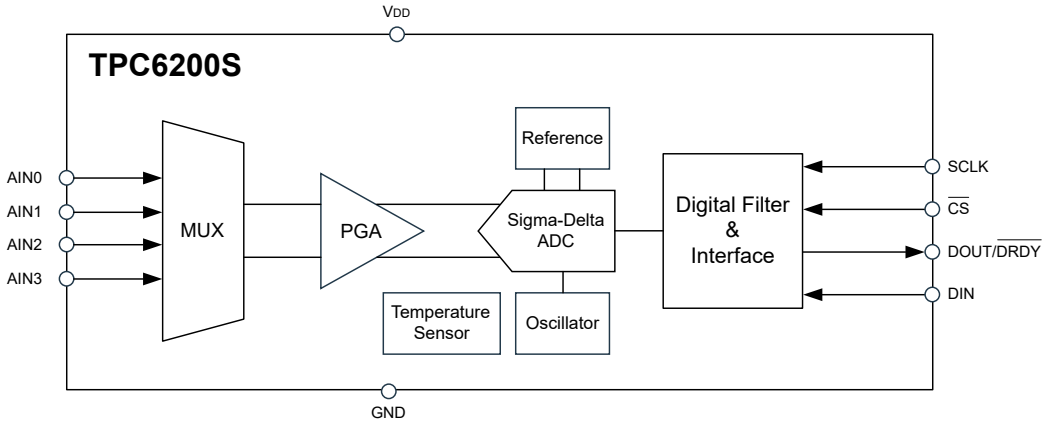


Figure 12. TPC6200S Block Diagram

Feature Description

Multiplexer

The TPC6200S is integrated with an input multiplexer (mux). It allows the measurement of either four single-ended signals or two differential signals. Also, the AIN0, AIN1, and AIN2 inputs can be differentially measured against AIN3. The configuration of the multiplexer is controlled by the MUX[2:0] bits in the Config register. In cases where single-ended signals are being measured, the negative input of the ADC is internally connected to GND through a switch within the multiplexer.

When single-ended inputs are being measured, the TPC6200S does not produce negative codes. Negative codes are indicative of negative differential signals, where $(V_{(AINP)} - V_{(AINN))} < 0$. Electrostatic discharge (ESD) diodes to VDD and GND serve to protect the ADC inputs. The TPC6200S is allowed to measure absolute negative input voltage down to −128mV and still needs to prevent the ESD diodes from turning on, it is essential to maintain the absolute voltage on any input within the range specified in the following equation:

$$GND - 0.3\ V < V_{(AINx)} < VDD + 0.3\ V \quad (3)$$

If there is a possibility that the voltages on the input pins may violate these conditions, it is advisable to employ external Schottky diodes and series resistors. This helps to limit the input current to safe values. Additionally, overdriving one unused input on the TPC6200S may impact conversions occurring on other input pins at that time. In cases where overdriving unused inputs is a possibility, it is recommended to clamp the signal using external Schottky diodes.

Analog Inputs

The TPC6200S employs a switched-capacitor input stage, where capacitors undergo a continuous charging and discharging process to measure the voltage between AIN_P and AIN_N. The equivalent resistance is determined by the values of the capacitors and the frequency at which they are switched.

The common-mode input impedance is determined by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance may vary depending on the selected full-scale range. The common-mode input impedance is denoted as Z_{CM}.

The differential input impedance is measured by applying a differential signal to the AIN_P and AIN_N inputs. The average current flowing through the input pins represents the differential current and scales with the selected full-scale range. The symbol Z_{DIFF} represents the differential input impedance.

Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause DC gain errors, depending on the output impedance of the source that is driving the ADC input. The table below shows the allowable external resistance/capacitance values such that no gain error at the 20-bit level is introduced when data rate is within 2 kSPS.

Table 12. External R-C Combination for No 20-Bit Gain Error

R (Ω)	C (pF)
16	1000
50	300
100	150

Full-Scale Range (FSR) and LSB Size

The gain setting of PGA inside TPC6200S ΣΔ ADC determines the input full-scale range (FSR). The full-scale range is configured by bits PGA[2:0] in the Config register, and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V.

The table below presents the Full-Scale Range (FSR) alongside the corresponding Least Significant Bit (LSB) size. The LSB size is calculated from the full-scale voltage using the formula in Equation 4. It is essential to ensure that the analog input voltage never exceeds the specified analog input voltage range limit provided in the Electrical Characteristics. If a VDD greater than 4 V is utilized, the ±6.144-V full-scale range allows input voltages to extend up to the supply voltage. It is important to note that in such cases or whenever the supply voltage is less than the full-scale range (e.g., VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be achieved, resulting in a loss of dynamic range.

Equation (4): $LSB = FSR/2^{24}$

Table 13. Full-Scale Range and Corresponding LSB Size

FSR	LSB Size
±6.144 V (1)	732 nV
±4.096 V (1)	488 nV
±2.048 V	244 nV
±1.024 V	122 nV
±0.512 V	61 nV
±0.256 V	30.5 nV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

Voltage Reference

The TPC6200S integrates an internal voltage reference, and the use of an external reference is not supported with this device. Any errors associated with the initial voltage reference accuracy and its drift with temperature are accounted for in the gain error and gain drift specifications provided in the specifications.

Oscillator

The TPC6200S features an integrated oscillator, eliminating the need for an external clock to drive the device. It's important to note that the internal oscillator may exhibit drift over temperature and time. Additionally, the output data rate scales proportionally with the oscillator frequency.

Temperature Sensor

The TPC6200S includes a precision temperature sensor, activated by setting TS_MODE = 1 in the Config Register, which outputs a 14-bit left-justified result within a 16-bit conversion, with each LSB representing 0.03125°C and negative values in twos complement format.

Temperature (°C)	Digital Output (Binary)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001

Temperature (°C)	Digital Output (Binary)	HEX
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–40	11 1011 0000 0000	3B00

Converting from Temperature to Digital Codes

For positive temperatures:

For positive temperature values, twos complement is not applied; instead, the number is directly converted to a 14-bit binary format, left-justified within the 16-bit result, with the MSB set to 0 to indicate a positive sign.

For negative temperatures:

To generate the two's complement of a negative number, first, take the binary representation of its absolute value, complement all bits, add 1 to the result, and set the MSB to 1 to indicate the negative sign.

For positive temperature values, twos complement is not applied; instead, the number is directly converted to a 14-bit binary format, left-justified within the 16-bit result, with the MSB set to 0 to indicate a positive sign.

Converting from Digital Codes to Temperature

For positive temperatures:

For positive temperature values, twos complement is not applied; instead, the number is directly converted to a 14-bit binary format, left-justified within the 16-bit result, with the MSB set to 0 to indicate a positive sign.

For negative temperatures:

To generate the two's complement of a negative number, first, take the binary representation of its absolute value, complement all bits, add 1 to the result, and set the MSB to 1 to indicate the negative sign.

For positive temperature values, twos complement is not applied; instead, the number is directly converted to a 14-bit binary format, left-justified within the 16-bit result, with the MSB set to 0 to indicate a positive sign.

Global Chop Mode

Although the device has a low-drift PGA and modulator to achieve very low input voltage offset drift, a small amount of offset voltage drift sometimes is left in normal measurement. The device has a global chop option to reduce the offset voltage and its drift to very low levels.

The global chop mode can be enabled using the G_CHOP bit. When the global chop is enabled, the ADC performs two internal conversions to cancel the input offset voltage. The first conversion is taken with normal input polarity. And then the ADC reverses the internal input polarity and does a second conversion. Finally, the average of the two conversions is given out as the final result, removing the offset voltage.

In global chop mode, sequences are similar to taking consecutive single-shot conversions and swapping the input on each conversion. In continuous conversion mode with the global chop mode enabled, the first conversion result is available after the ADC takes two separate conversions with settled data, and subsequent conversions complete in half the time as the first conversion completes.

The global chop mode also reduces the ADC noise by a factor of $\sqrt{2}$ because two conversions are averaged.

Digital Interface

Device Functional Modes

Reset and Power-Up

When the TPC6200S powers up, the device undergoes a reset procedure that results in the configuration register (Config register) having all its bits set to their default values. In its default state, the device enters a power-down mode upon startup. During this mode, the device's interface and digital blocks remain active, but no data conversions take place. This initial power-down state is designed to prevent systems with stringent power-supply requirements from experiencing a surge during the power-up phase.

Operating Modes

The TPC6200S operates in one of two modes: continuous-conversion or single-shot. The operating mode is determined by the state of the MODE bit in the Config register.

Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, indicating single-shot mode, the TPC6200S enters a power-down state. This power-down state is the default state when power is first applied. While in this state, the device remains responsive to commands. The device will stay in the power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is set, the device powers up, resets the SS bit to 0, and initiates a single conversion. Once the conversion is completed, and the conversion data are ready, the device returns to the power-down state. Attempting to write a 1 to the SS bit while a conversion is already in progress will have no effect. To switch to continuous-conversion mode, it is necessary to write a 0 to the MODE bit in the Config register.

Continuous-Conversion Mode

In continuous-conversion mode, where the MODE bit is set to 0, the TPC6200S consistently conducts conversions. Once a conversion is finished, the result is stored in the Conversion register, and the device promptly initiates another conversion. To transition to single-shot mode, one can write a 1 to the MODE bit in the Config register or perform a device reset.

Duty Cycling for Low Power

The noise performance of a ΣΔ ADC typically improves at lower output data rates, as more samples of the internal modulator are averaged to produce a single conversion result. In scenarios where power consumption is critical consideration and the enhanced noise performance at low data rates is not essential, the TPC6200S provides support for duty cycling. This feature enables significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

Programming

Serial Interface

The SPI-compatible serial interface of the TPC6200S includes either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$) or three signals (SCLK, DIN, and DOUT/$\overline{DRDY}$ with $\overline{CS}$ tied low). This interface facilitates tasks such as reading conversion data, accessing registers for reading and writing, and controlling the operation of the device.

Chip Select

The chip select pin ($\overline{CS}$) is utilized to select the TPC6200S for SPI communication, particularly beneficial in scenarios where multiple devices share the same serial bus. It is essential to keep $\overline{CS}$ low throughout the serial communication process. When $\overline{CS}$ is raised to a high state, the serial interface undergoes a reset, SCLK signals are disregarded, and DOUT/$\overline{DRDY}$ enters a high-impedance state, rendering it unable to provide data-ready indication. For situations involving multiple devices where DOUT/$\overline{DRDY}$ monitoring is necessary, periodically lowering $\overline{CS}$ enables either an immediate high signal, indicating no new data, or an immediate low signal, indicating the availability of new data in the Conversion register. Data transfer can occur at any time without risking data corruption, as the current result is locked into the output shift register during transmission and remains unchanged until the communication concludes.

Serial Clock

The serial clock pin (SCLK) incorporates a Schmitt-triggered input and serves the purpose of clocking data into and out of the TPC6200S through the DIN and DOUT/$\overline{DRDY}$ pins. It is important to maintain a clean SCLK signal, despite the hysteresis present, to prevent glitches that could inadvertently shift the data. To initiate a reset of the serial interface, SCLK should be held low for 30.8 ms, and the subsequent SCLK pulse will commence a new communication cycle. This time-out feature can be utilized to recover communication in cases where a serial interface transmission is interrupted. During idle periods of the serial interface, SCLK should be held low.

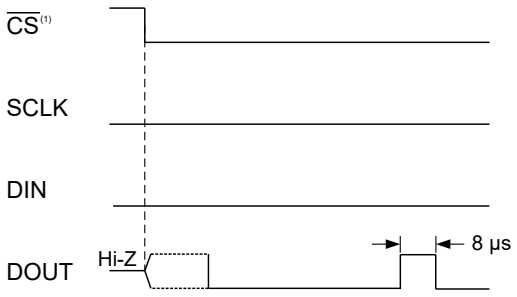
Data Input

The data input pin (DIN) collaborates with SCLK to transmit data to the TPC6200S. Data is latched on the DIN pin at the falling edge of the SCLK signal. It's important to note that the device does not actively drive the DIN pin.

Data Output and Data Ready

The data output and data ready pin (DOUT/$\overline{DRDY}$) are employed, along with SCLK, for reading conversion and register data from the TPC6200S. Data present on DOUT/$\overline{DRDY}$ are shifted out on the rising edge of the SCLK signal. Additionally, DOUT/$\overline{DRDY}$ serves as an indicator of the completion of a conversion, signaling that new data are ready for retrieval. The pin transitions low when new data are available. DOUT/DRDY can also be utilized to trigger a microcontroller to initiate the reading of data from the TPC6200S. In continuous-conversion mode, DOUT/$\overline{DRDY}$ returns high again 8 µs before the subsequent data ready signal (DOUT/$\overline{DRDY}$ low) if no data are retrieved from the device. It is essential to complete the data transfer before DOUT/$\overline{DRDY}$ returns high.

In single-shot mode, once the $\overline{DRDY}$ is low for signaling data ready, the new SPI command should be sent 8 µs after the $\overline{DRDY}$ low.



(1) $\overline{CS}$ can be held low if the TPC6200S does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data is available.

Figure 13. DOUT/$\overline{DRDY}$ Behavior without Data Retrieval in Continuous-Conversion Mode

When the chip select ($\overline{CS}$) pin is in a high state, the data output and data ready pin (DOUT/$\overline{DRDY}$) are automatically configured with a weak internal pullup resistor as a default setting. This configuration minimizes the chance of DOUT/$\overline{DRDY}$ floating near the mid-supply voltage and causing a leakage current in the master device. To deactivate this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config register.

Data Format

The TPC6200S outputs data in a 24-bit binary two's complement format. For a positive full-scale (+FS) input, the output code is 7FFFFFh, while a negative full-scale (−FS) input results in an output code of 800000h. The output codes clip at these values for signals that exceed the full-scale range. The table below provides a summary of the ideal output codes corresponding to different input signals.

Table 14. Input Signal versus Ideal Output Code

INPUT SIGNAL, VIN (AIN_P – AIN_N)	IDEAL OUTPUT CODE (1)
≥ FS (2^{23} – 1) / 2^{23}	7FFFFFh
FS / 2^{23}	000001h
0	000000h
−FS / 2^{23}	FFFFFFh
≤ −FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

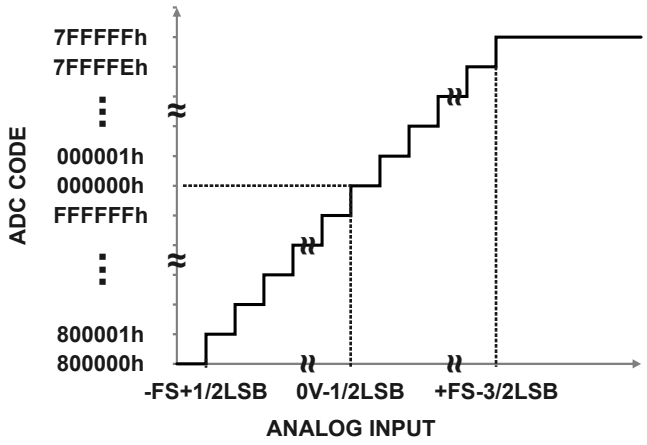


Figure 14. Code Transition Diagram

Data Retrieval

Data is written to and read from the TPC6200S in the same manner for both single-shot and continuous-conversion modes, without the need to issue specific commands. The operating mode for the device is determined by the MODE bit in the Config register.

To set the device in continuous-conversion mode, set the MODE bit to 0. In this mode, the device consistently initiates new conversions, even when the $\overline{CS}$ is high.

To activate the single-shot mode, set the MODE bit to 1. In this mode, a new conversion begins only when the SS bit is written with a value of 1.

The conversion data is continuously buffered and remains unchanged until new conversion data replaces it. Reading the data can be done at any time without the risk of corruption. When DOUT/$\overline{DRDY}$ goes low, indicating the availability of new

conversion data, the data can be read by shifting it out on DOUT/$\overline{DRDY}$. The most significant bit (MSB), bit 23, is clocked out on the first rising edge of SCLK. Simultaneously, new data for the Config register is latched on DIN during the falling edge of SCLK.

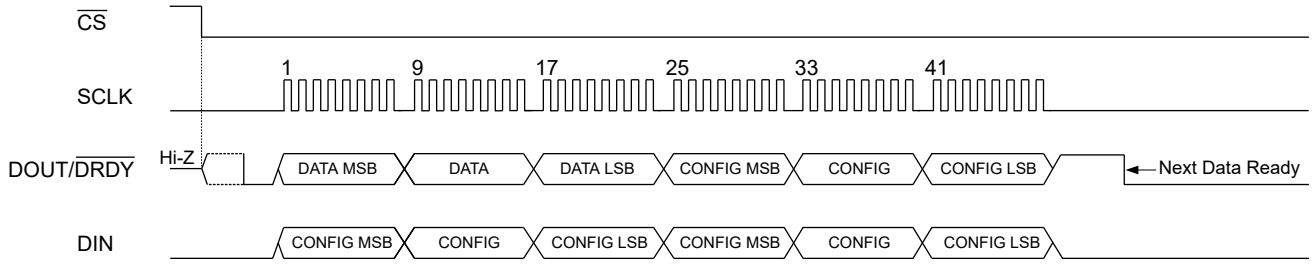
The TPC6200S provides an option for direct readback of the Config register settings within the same data transmission cycle. A complete data transmission cycle is either 48 bits (when Config register readback is employed) or 24 bits (used only when the $\overline{CS}$ line is controllable and not permanently tied low).

48-Bit Data Transmission Cycle

The data in a 48-bit data transmission cycle consists of six bytes: three bytes for the conversion result, and an additional three bytes for the Config register readback. The device always reads the MSB first.

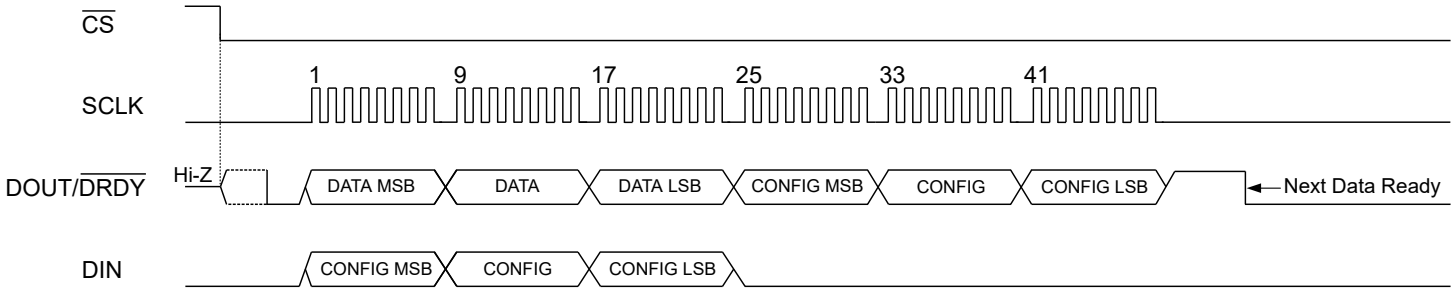
During a single transmission cycle, write the same Config register setting twice, as illustrated in figure below. For convenience, user can write the Config register setting once during the first half of the transmission cycle. Subsequently, maintain the DIN pin either low or high during the second half of the cycle. If there is no need to update the Config register, keep the DIN pin either low or high throughout the entire transmission cycle in continuous-conversion mode, while keeping the DIN pin high only in single-shot mode. The Config register setting written in the first three bytes of a 48-bit transmission cycle is read back in the last three bytes of the same cycle.

When utilizing a continuous SCLK for the entire 48-bit data transfer, ensure that the SCLK frequency remains below 1 MHz. In case an SCLK frequency exceeding 1 MHz is employed, introduce a delay between the transmission of the first 24 bits and the second 24 bits. This delay is necessary to allow for the complete decoding of the Config register write before initiating the readback of the Config register. Select a delay that ensures the time between the SCLK rising edge of the first bit and the SCLK rising edge of the 25th bit exceeds 16 µs.



(1) $\overline{CS}$ can be held low if the TPC6200S does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data is available.

Figure 15. 48-Bit Data Transmission Cycle with Config Register Readback



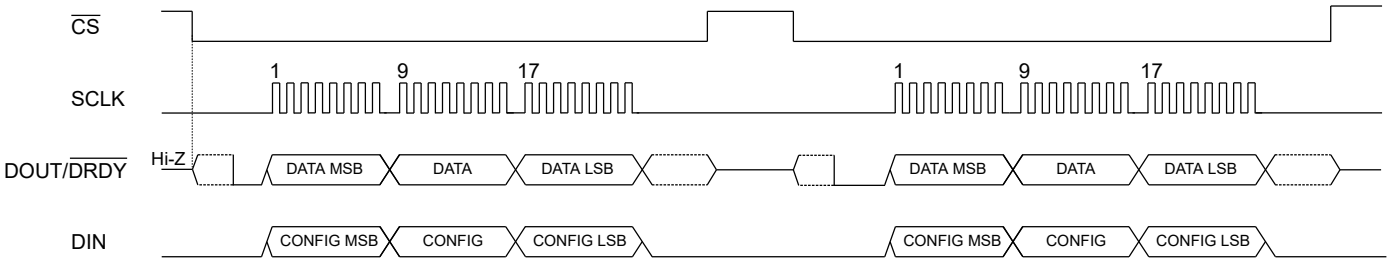
(1) $\overline{CS}$ can be held low if the TPC6200S does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 16. 48-Bit Data Transmission Cycle: DIN Held Low

24-Bit Data Transmission Cycle

If there is no need to read back Config register data, the conversion data from the TPC6200S can be clocked out in a concise 24-bit data transmission cycle, as depicted in figure below. After the 24th SCLK cycle, set $\overline{CS}$ high to reset the SPI interface. Upon the subsequent lowering of $\overline{CS}$, data transmission initiates, starting with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low at the beginning of data retrieval, the conversion buffer is already updated with a new result. Conversely, if DOUT/$\overline{DRDY}$ is high, the same result from the preceding data transmission cycle is read.

If there is no need to update the Config register, keep the DIN pin either low or high throughout the entire transmission cycle in continuous-conversion mode, while keeping the DIN pin high only in single-shot mode



(1) $\overline{CS}$ can be held low if the TPC6200S does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data is available.

Figure 17. 24-Bit Data Transmission Cycle

Register Summary

The TPC6200S features two accessible registers via SPI. The Conversion register is the result of the most recent conversion, while the Config register sets operating modes and inquires about the device status.

Conversion Register [reset = 000000h]

The 24-bit Conversion register stores the results of the latest conversion in binary twos complement format. After power-up, the register is reset to 0 and retains this value until the initial conversion is finished. Refer to the table below for the register format.

Table 15. Conversion Register

23	22	21	20	19	18	17	16
D23	D22	D21	D20	D19	D18	D17	D16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
23:0	D[23:0]	R	000000h	24-bit conversion result

Config Register [reset = 058B20h]

The 24-bit Config register can be configured to set the TPC6200S operating mode, input selection, data rate, full-scale range, temperature sensor mode and global chop mode. The register format is shown in table below.

Table 17. Config Register

23	22	21	20	19	18	17	16
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DR[2:0]			TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR_Boost[1:0]		Global Chop	Reserved				
R/W-0h		R/W-1h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

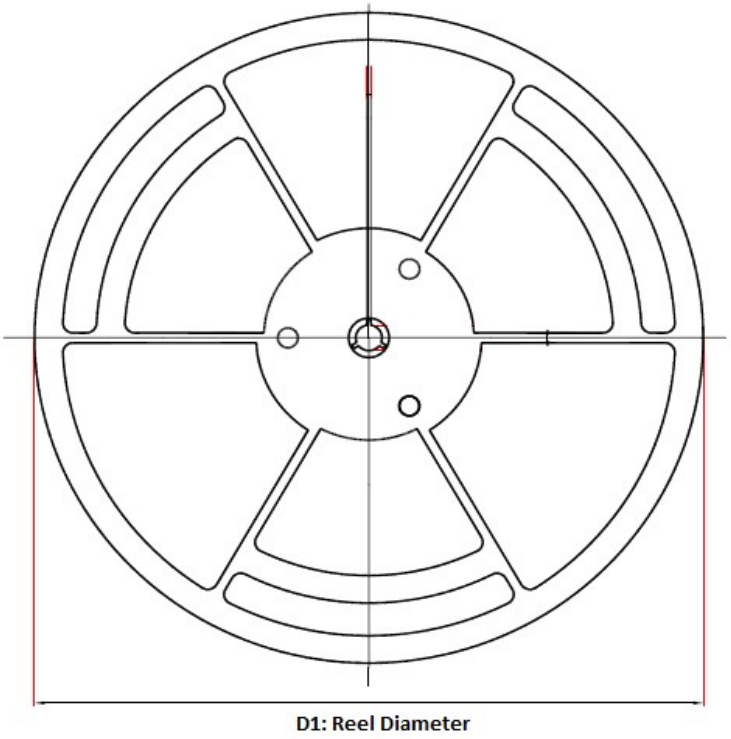
Table 18. Config Register Field Descriptions

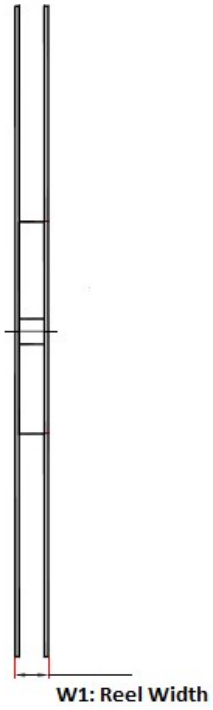
Bit	Field	Type	Reset	Description
23	SS	R/W	0h	**Single-shot conversion start** This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back as 0 (default).
22:20	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND
19:17	PGA[2:0]	R/W	2h	**Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 = FSR is ±6.144 V (1) 001 = FSR is ±4.096 V (1) 010 = FSR is ±2.048 V (default) 011 = FSR is ±1.024 V 100 = FSR is ±0.512 V 101 = FSR is ±0.256 V 110 = FSR is ±0.256 V 111 = FSR is ±0.256 V
16	MODE	R/W	1h	**Device operating mode** This bit controls the TPC6200S operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
15:13	DR[2:0]	R/W	4h	**Data rate** These bits control the data-rate setting. 000 = 64 SPS 001 = 128 SPS 010 = 256 SPS 011 = 512 SPS 100 = 1024 SPS (default) 101 = 2 kSPS 110 = 4 kSPS 111 = 8 kSPS

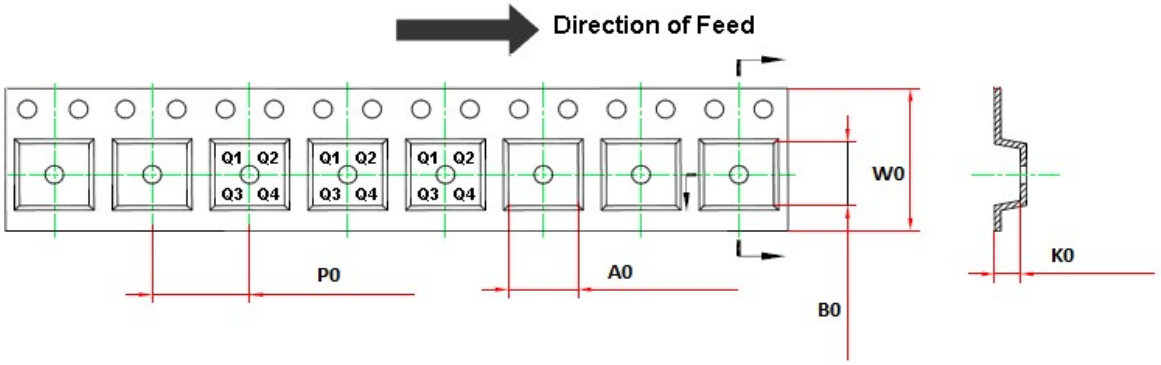
Bit	Field	Type	Reset	Description
12	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default 1 = Temperature sensor mod
11	PULL_UP_EN	R/W	1h	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{\text{DRDY}}$ pin only when $\overline{\text{CS}}$ is high. When enabled, an internal resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats. 0 = Pullup resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin 1 = Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin
10:9	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data; do not update the contents of the Config register 01 = Valid data; update the Config register (default) 10 = Invalid data; do not update the contents of the Config register 11 = Invalid data; do not update the contents of the Config register
8	Reserved	R	1h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 1.
7:6	DR_Boost[1:0]	R/W	0h	**Data rate boost** These bits control the data-rate boost setting. 00 Data rate is set by DR[2:0] register 01 = 16 kSPS 10 = 32 kSPS 11 = 32 kSPS
5	Global Chop Mode	R/W	1h	**Global chop mode** These bits set the global chop mode. 1 = Enable global chop (default) 0 = Disable global chop
4:0	Reserved	R/W	0h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 0.

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

Tape and Reel Information





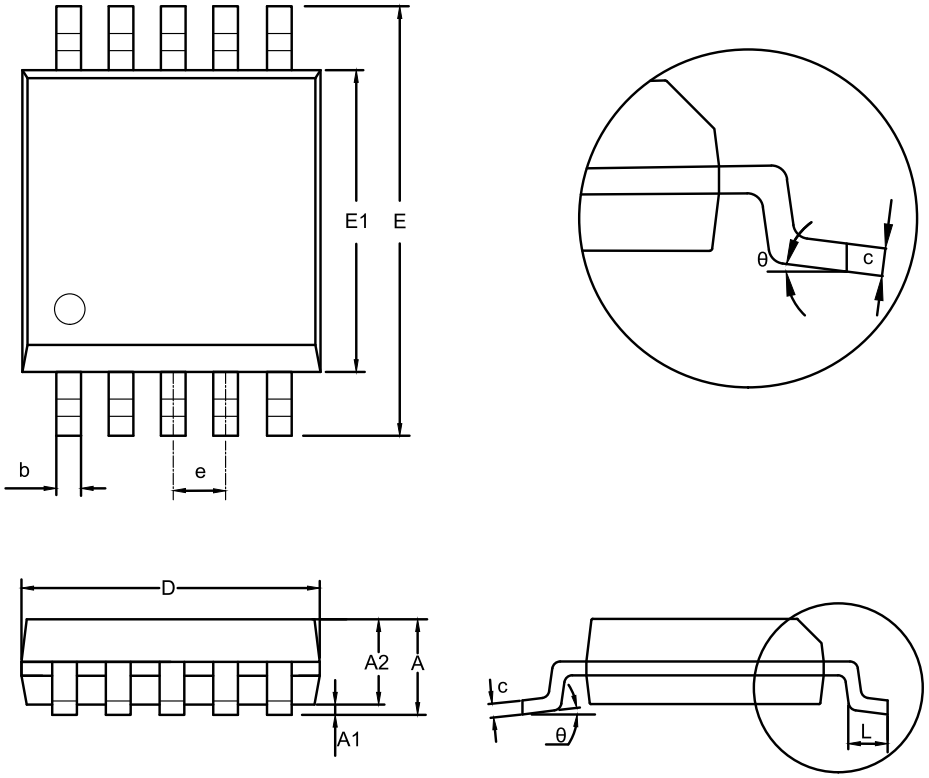


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC6200S-VS2R	MSOP10	330	17.6	5.3	3.4	1.4	8	12	Q1

Package Outline Dimensions

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC6200S-VS2R	−40 to 125°C	MSOP-10	6200S	2	T&R, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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