TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSVI)

TPC8001

Lithium Ion Battery Applications
Portable Equipment Applications
Notebook PC Applications

- Small footprint due to small and thin package
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 15 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 11 S (typ.)
- Low leakage current : I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement−mode : V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

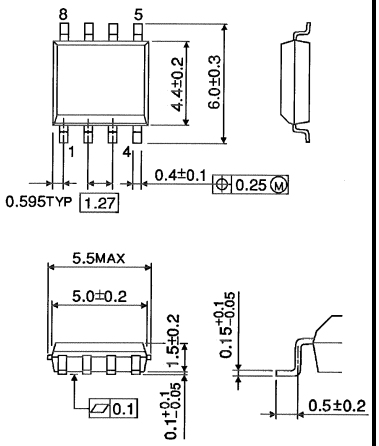
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	7	A
	Pulse (Note 1)	I_{DP}	28	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	2.4	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.0	W
Single pulse avalanche energy (Note 3)		E_{AS}	64	mJ
Avalanche current		I_{AR}	7	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.24	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For (Note 1), (Note 2), (Note 3) and (Note 4), please refer to the next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

Unit: mm

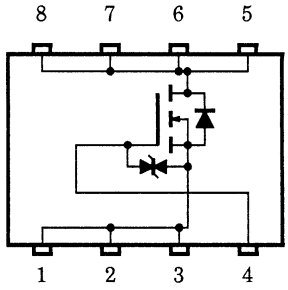


1, 2, 3 SOURCE
4 GATE
5, 6, 7, 8 DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-6J1B

Weight: 0.080 g (typ.)

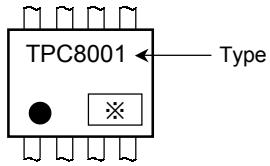
Circuit Configuration



Thermal Characteristics

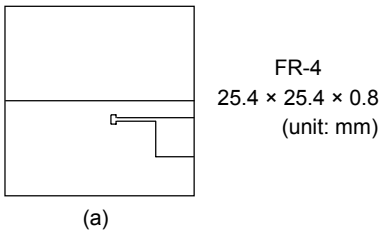
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	52.1	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	125	°C/W

Marking (Note 5)

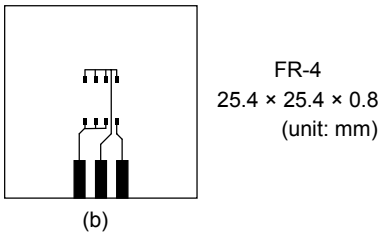


Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)



(b)

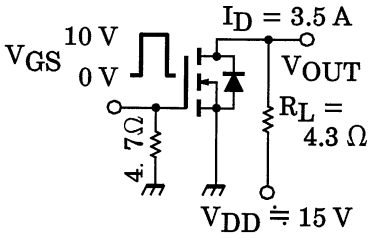
Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 7 A

Note 4: Reptitve rating; pulse width limited by maximum channel temperature

Note 5: ● on lower left of the marking indicates Pin 1.

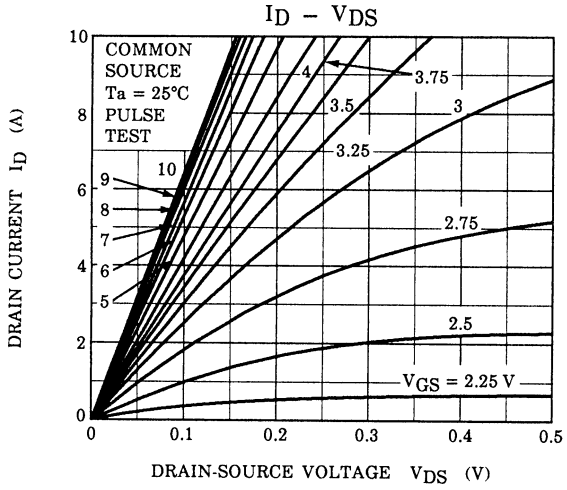
※ shows lot number. (year of manufacture: last decimal digit of the year of manufacture, month of manufacture: January to December are denoted by letters A to L respectively.)

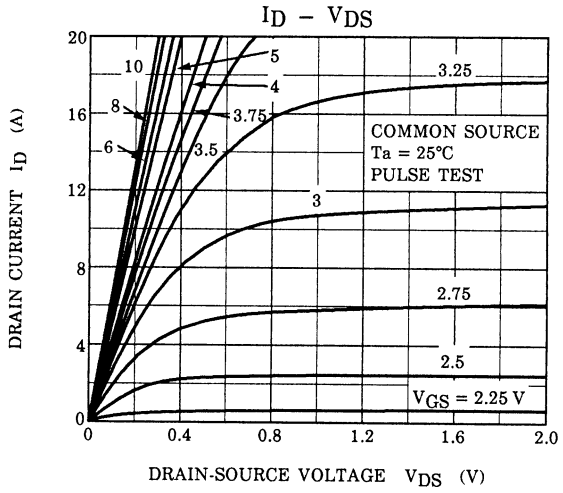
Electrical Characteristics (Ta = 25°C)

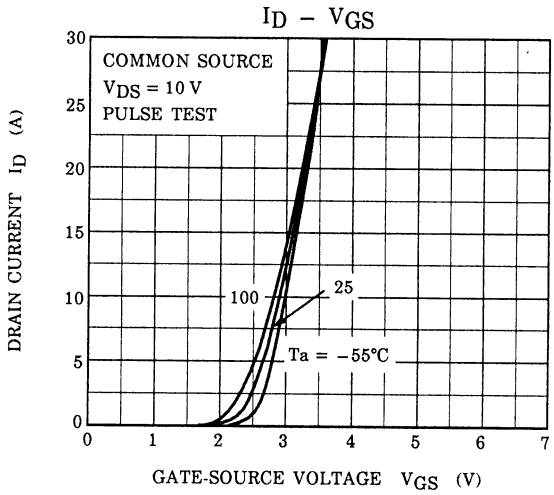
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 3.5 A	—	25	30	mΩ
		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 3.5 A	—	16	20	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3.5 A	5.5	11	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1250	—	pF
Reverse transfer capacitance		C_{rss}		—	190	—	
Output capacitance		C_{oss}		—	760	—	
Switching time	Rise time	tr		—	9	—	ns
	Turn−on time	t_{on}		—	17	—	
	Fall time	t_f		—	24	—	
	Turn−off time	t_{off}		—	100	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 7 A	—	40	—	nC
Gate−source charge		Q_{gs}		—	27	—	
Gate−drain (“miller”) charge		Q_{gd}		—	13	—	

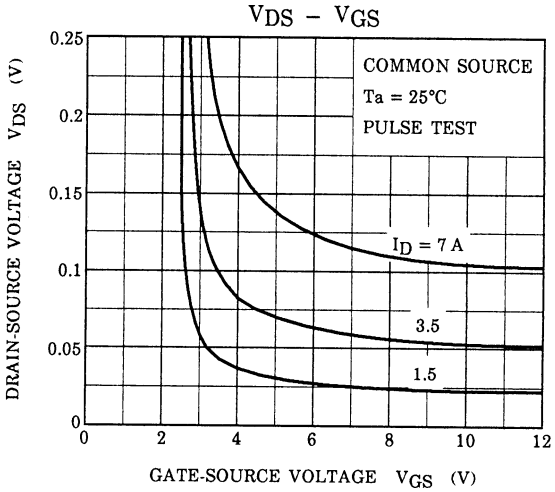
Source−Drain Ratings and Characteristics (Ta = 25°C)

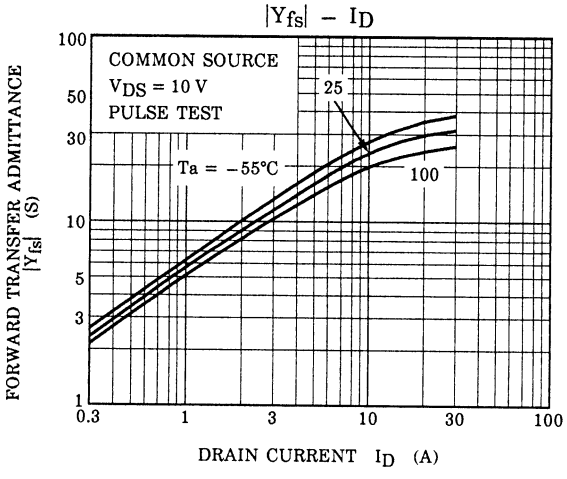
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	28	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 7 A, V_{GS} = 0 V	—	—	−1.2	V

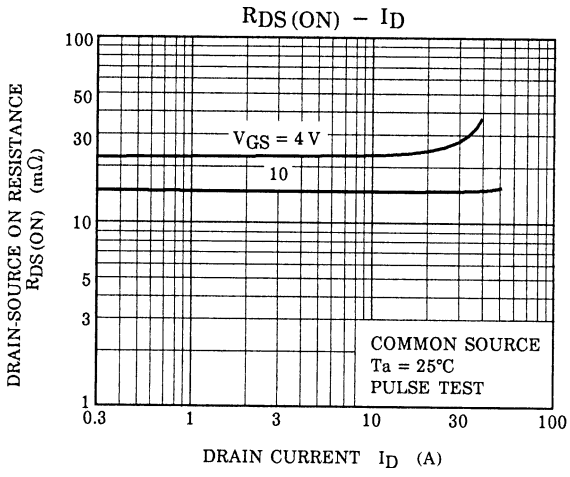

I_D – V_{DS}
COMMON SOURCE
Ta = 25°C
PULSE TEST
10
9
8
7
6
5
4
3.75
3.5
3
3.25
2.75
2.5
V_{GS} = 2.25 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
10
8
6
5
4
3.75
3.5
3.25
3
2.75
2.5
V_{GS} = 2.25 V
COMMON SOURCE
Ta = 25°C
PULSE TEST
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)

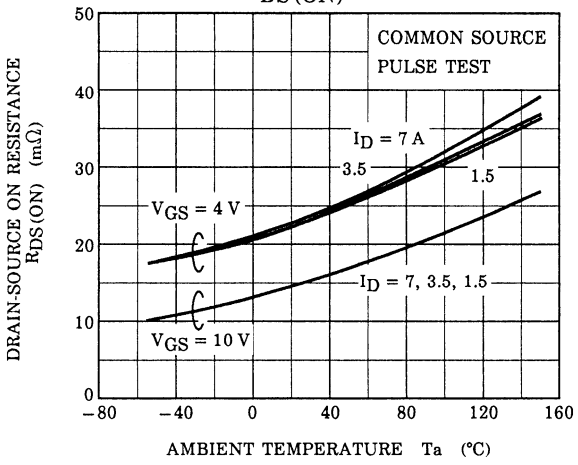

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
100
25
Ta = −55°C
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)


V_{DS} – V_{GS}
COMMON SOURCE
Ta = 25°C
PULSE TEST
I_D = 7 A
3.5
1.5
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)

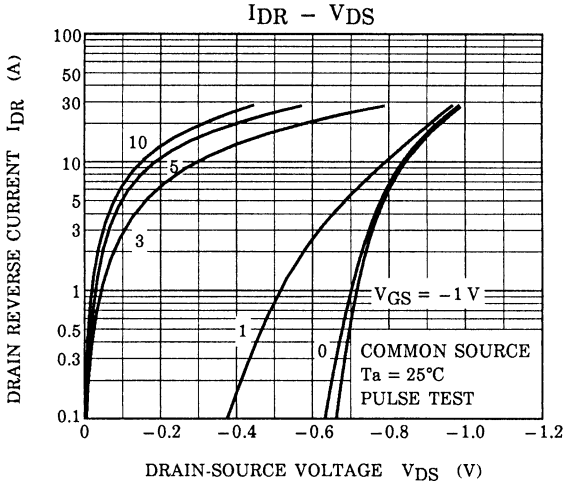

$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
25
Ta = −55°C
100
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS\,(ON)}$ – I_D
V_{GS} = 4 V
10
COMMON SOURCE
Ta = 25°C
PULSE TEST
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (mΩ)
DRAIN CURRENT I_D (A)

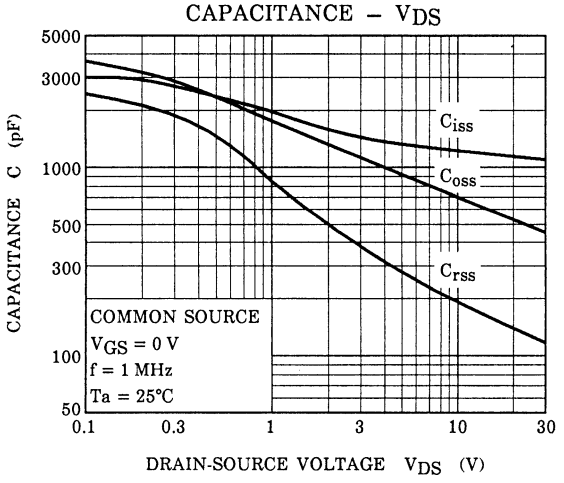
$R_{DS\,(ON)}$ – Ta



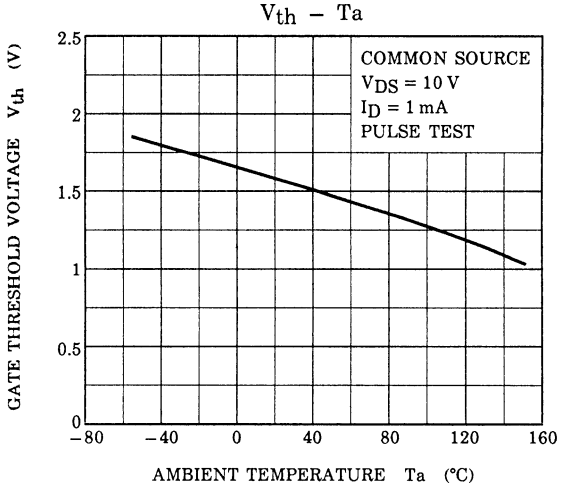
I_{DR} – V_{DS}



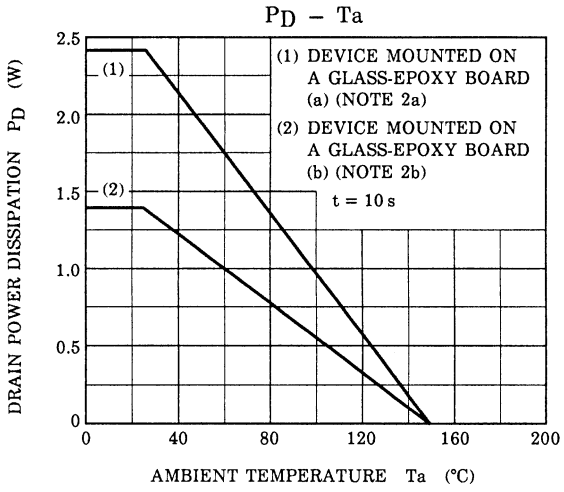
CAPACITANCE – V_{DS}



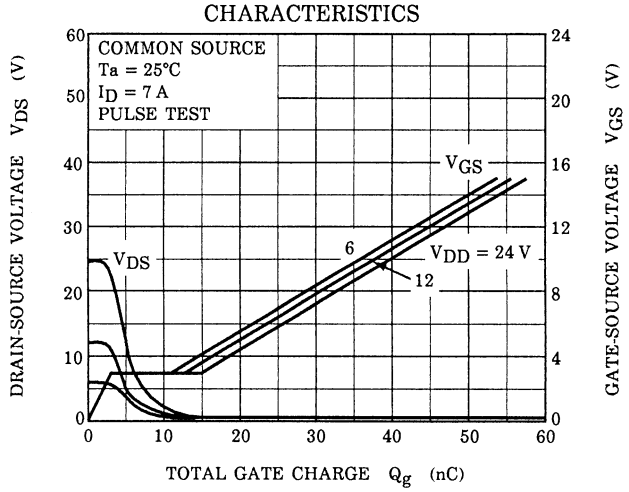
V_{th} – Ta



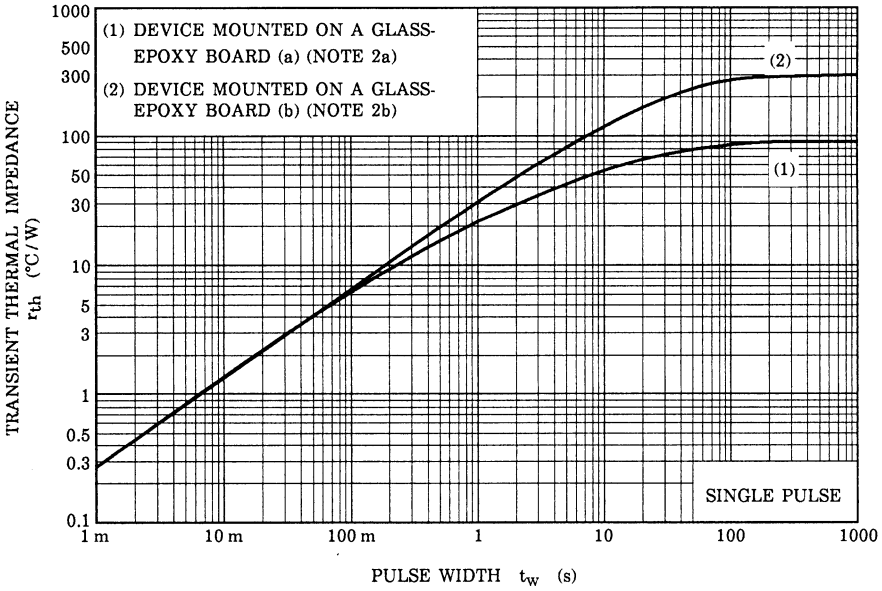
P_D – Ta



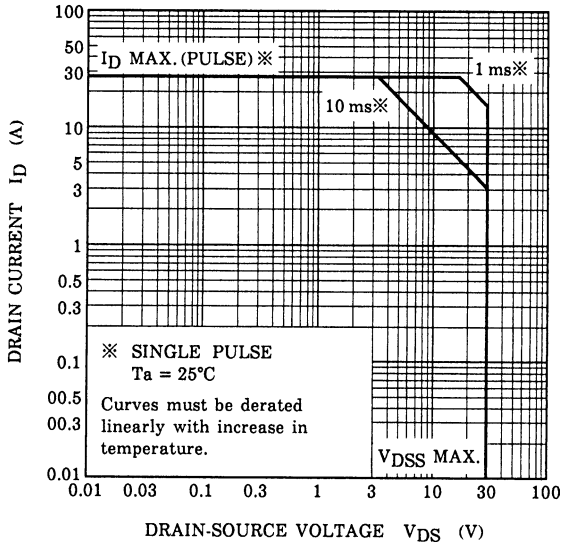
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



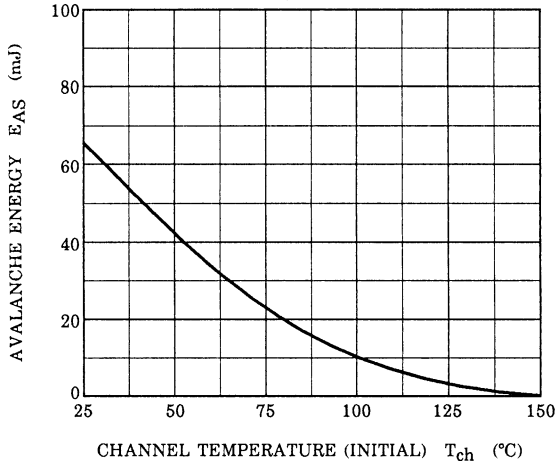
r_{th} – t_w

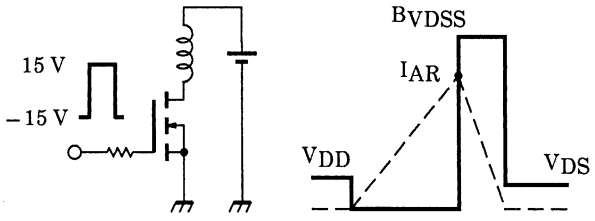


SAFE OPERATING AREA



E_{AS} – T_{ch}





TEST CIRCUIT WAVE FORM

T_{ch} = 25°C (Initial)
Peak I_{AR} = 7 A, R_G = 25 Ω
V_{DD} = 24 V, L = 1.0 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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000707EAA

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