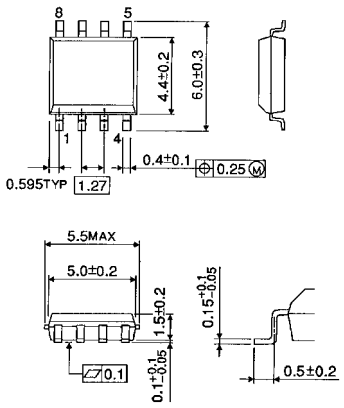
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra High speed U-MOSIII)

# TPC8017-H

High Speed and High Efficiency DC-DC Converters
Notebook PC Applications
Portable Equipment Applications

- Small footprint due to small and thin package
- High speed switching
- Small gate charge: $Q_g$ = 25 nC (typ.)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 5.1 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ =38 S (typ.)
- Low leakage current: $I_{DSS}$ = 10 μA (max) ($V_{DS}$ = 30 V)
- Enhancement mode: $V_{th}$ = 1.1 to 2.3 V ($V_{DS}$ = 10 V, $I_D$ = 1 mA)

Unit: mm




1, 2, 3 SOURCE
4 GATE
5, 6, 7, 8 DRAIN

| | |
|---|---|
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-6J1B |

Weight: 0.080 g (typ.)

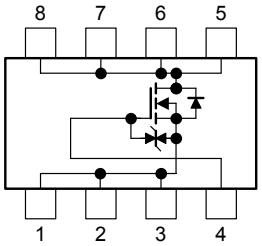
## Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 30 | V |
| Drain-gate voltage ($R_{GS}$ = 20 kΩ) | | $V_{DGR}$ | 30 | V |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC (Note 1) | $I_D$ | 15 | A |
| | Pulsed (Note 1) | $I_{DP}$ | 60 | |
| Drain power dissipation (t = 10 s) (Note 2a) | | $P_D$ | 1.9 | W |
| Drain power dissipation (t = 10 s) (Note 2b) | | $P_D$ | 1.0 | W |
| Single pulse avalanche energy (Note 3) | | $E_{AS}$ | 146 | mJ |
| Avalanche current | | $I_{AR}$ | 15 | A |
| Repetitive avalanche energy (Note 2a) (Note 4) | | $E_{AR}$ | 0.19 | mJ |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

Note: For (Note 1), (Note 2), (Note 3), (Note 4), please refer to the next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

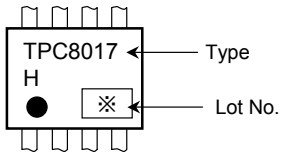
## Circuit Configuration



## Thermal Characteristics

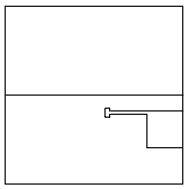
| Characteristics | Symbol | Max | Unit |
|---|---|---|---|
| Thermal resistance, channel to ambient (t = 10 s) (Note 2a) | $R_{th\ (ch\text{-}a)}$ | 65.8 | °C/W |
| Thermal resistance, channel to ambient (t = 10 s) (Note 2b) | $R_{th\ (ch\text{-}a)}$ | 125 | °C/W |

## Marking (Note 5)

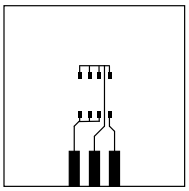



Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)




(a)



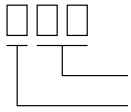

(b)

Note 3: $V_{DD}$ = 24 V, $T_{ch}$ = 25°C (initial), L = 0.5 mH, $R_G$ = 25 Ω, $I_{AR}$ = 15 A

Note 4: Repetitive rating: pulse width limited by max channel temperature

Note 5: • on lower left of the marking indicates Pin 1.

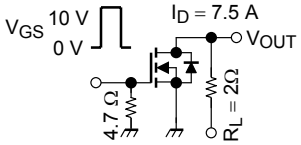
* Weekly code: (Three digits)



Week of manufacture
(01 for first week of year, continues up to 52 or 53)

Year of manufacture
(One low-order digits of calendar year)

## Electrical Characteristics (Ta = 25°C)

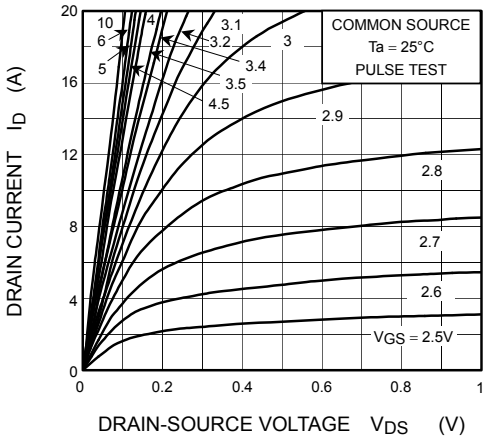
| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 V | — | — | ±10 | μA |
| Drain cut-OFF current | | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | — | — | 10 | μA |
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 30 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 10 mA, $V_{GS}$ = −20 V | 15 | — | — | |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.1 | — | 2.3 | V |
| Drain-source ON resistance | | $R_{DS\ (ON)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 7.5 A | — | 7.3 | 9.5 | mΩ |
| | | | $V_{GS}$ = 10 V, $I_D$ = 7.5 A | — | 5.1 | 6.6 | |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 7.5 A | 19 | 38 | — | S |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 1465 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 175 | — | |
| Output capacitance | | $C_{oss}$ | | — | 610 | — | |
| Switching time | Rise time | $t_r$ |   Duty ≦ 1%, $t_w$ = 10 μs | — | 4 | — | ns |
| | Turn-ON time | $t_{on}$ | | — | 11 | — | |
| | Fall time | $t_f$ | | — | 10 | — | |
| | Turn-OFF time | $t_{off}$ | | — | 38 | — | |
| Total gate charge (gate-source plus gate-drain) | | $Q_g$ | $V_{DD}$ ≃ 24 V, $V_{GS}$ = 10 V, $I_D$ = 15 A | — | 25 | — | nC |
| | | | $V_{DD}$ ≃ 24 V, $V_{GS}$ = 5 V, $I_D$ = 15 A | — | 14 | — | |
| Gate-source charge 1 | | $Q_{gs1}$ | $V_{DD}$ ≃ 24 V, $V_{GS}$ = 10 V, $I_D$ = 15 A | — | 4.7 | — | |
| Gate-drain (“miller”) charge | | $Q_{gd}$ | | — | 5.7 | — | |
| Gate switch charge | | $Q_{SW}$ | | — | 7.8 | — | |

## Source-Drain Ratings and Characteristics (Ta = 25°C)

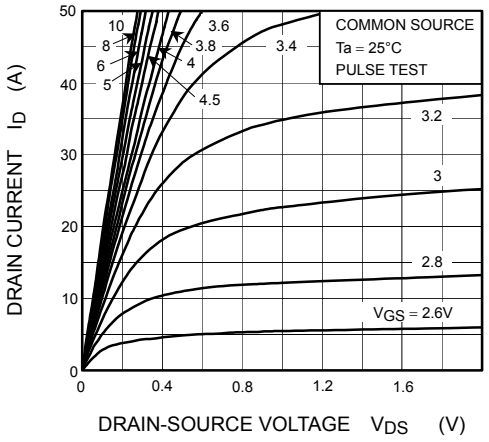


| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain reverse current | Pulse (Note 1) | $I_{DRP}$ | — | — | — | 60 | A |
| Forward voltage (diode) | | $V_{DSF}$ | $I_{DR}$ = 15 A, $V_{GS}$ = 0 V | — | — | −1.2 | V |

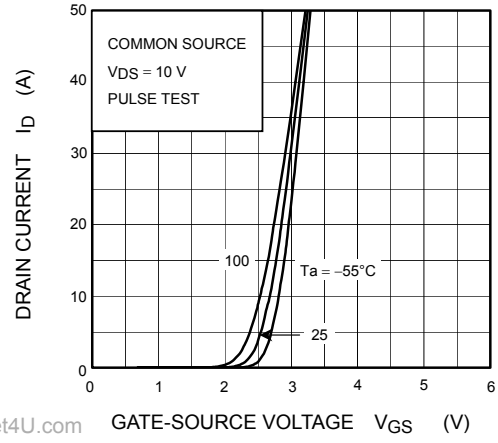
$I_D - V_{DS}$




$I_D - V_{DS}$

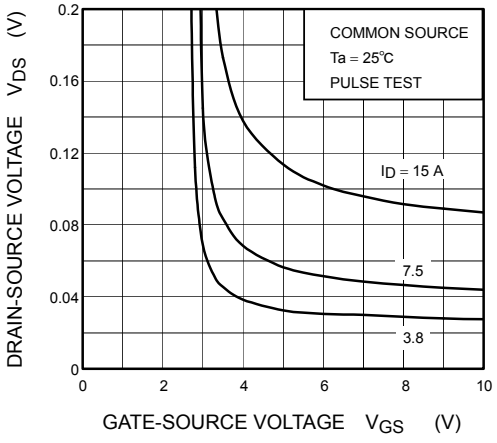



$I_D - V_{GS}$

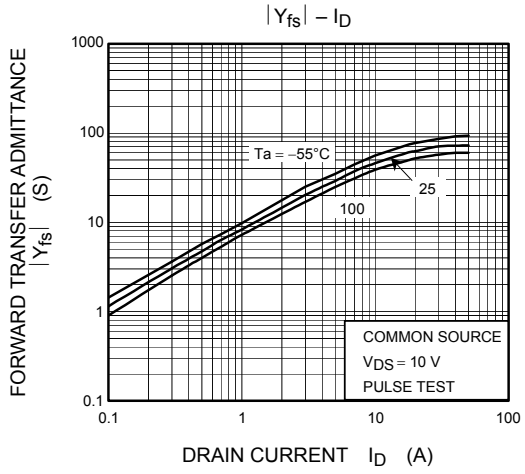




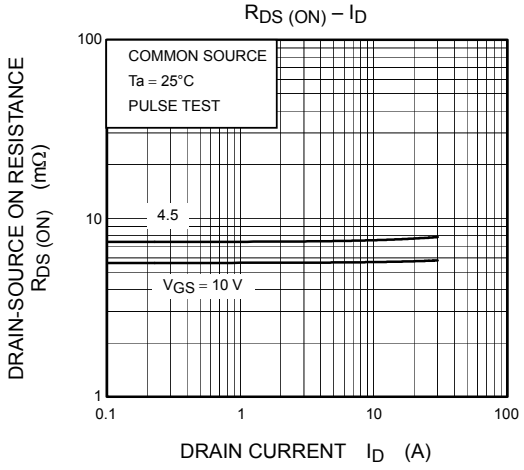

$V_{DS} - V_{GS}$



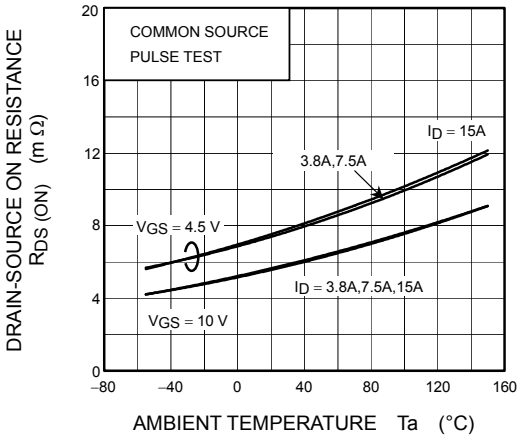

$|Y_{fs}| - I_D$



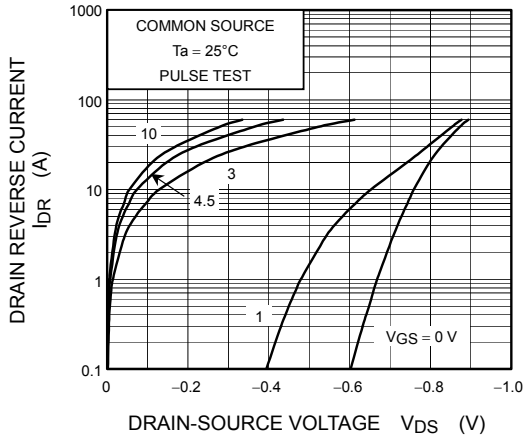

$R_{DS\ (ON)} - I_D$



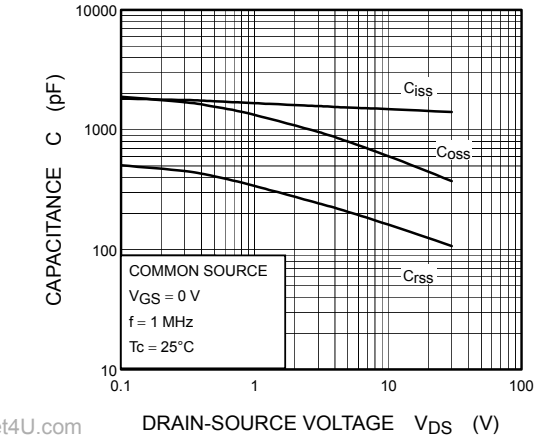
$R_{DS\ (ON)}$ – Ta



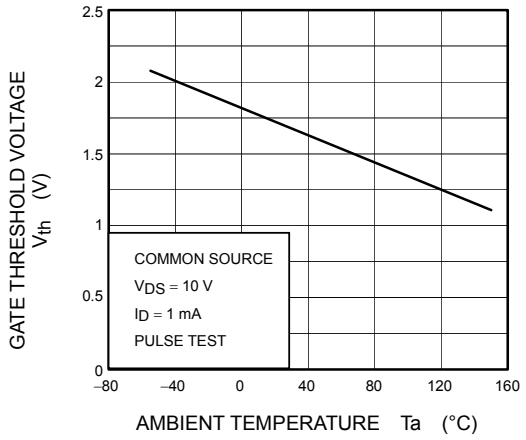

$I_{DR}$ – $V_{DS}$




CAPACITANCE – $V_{DS}$

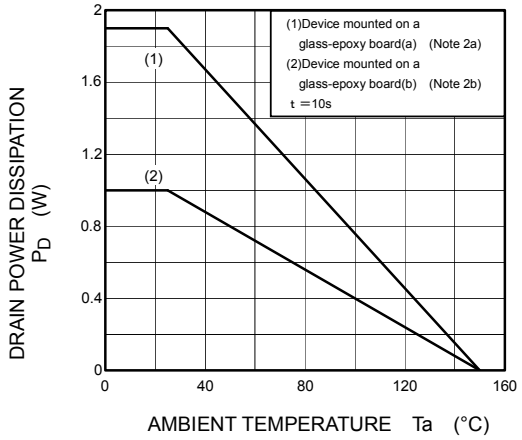



$V_{th}$ – Ta

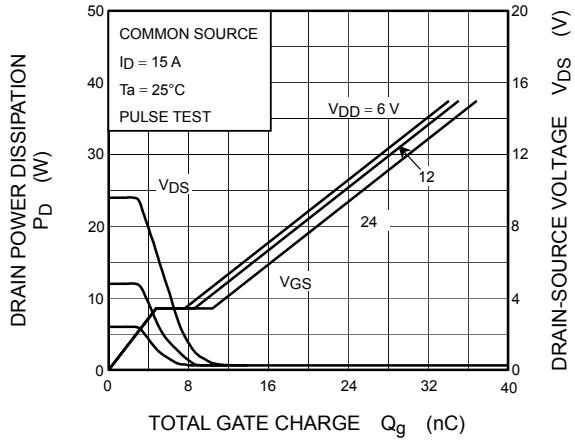




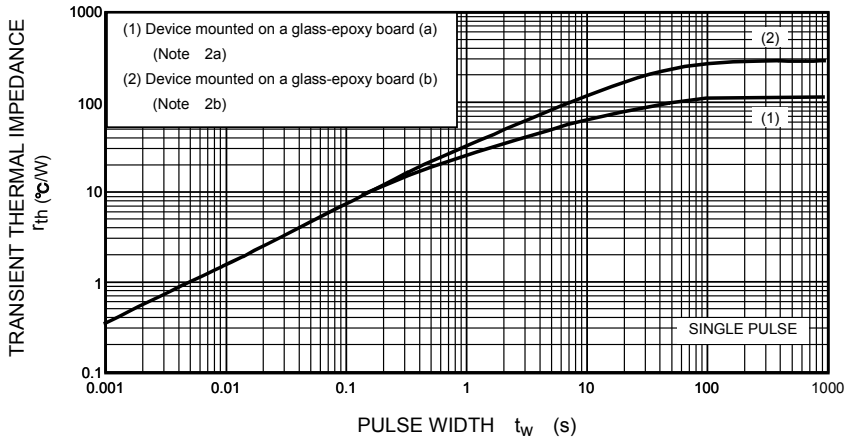

$P_D$ – Ta



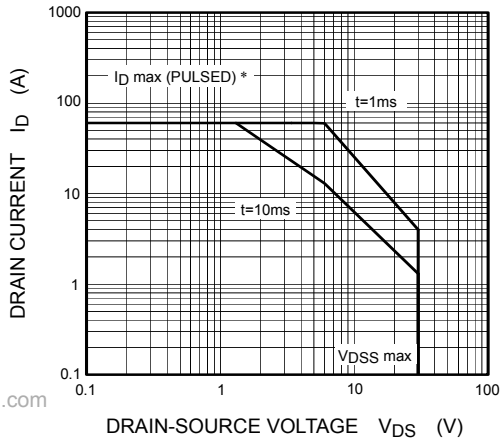

DYNAMIC INPUT / OUTPUT CHARACTERISTICS



$r_{th} - t_w$




SAFE OPERATING AREA



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