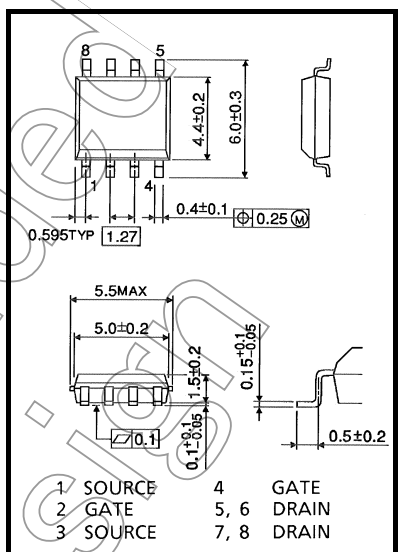
TOSHIBA Field Effect Transistor Silicon P, N Channel MOS Type
(P Channel π-MOSV/N Channel π-MOSV)

TPC8404

Motor Dreive
Switching Regulator Applications

- Low drain-source ON resistance: P Channel $R_{DS\ (ON)}$ = 1.85 Ω (typ.)
  N Channel $R_{DS\ (ON)}$ = 1.2 Ω (typ.)
- High forward transfer admittance: P Channel $|Y_{fs}|$ = 1.1 S (typ.)
  N Channel $|Y_{fs}|$ = 1.3 S (typ.)
- Low leakage current: P Channel I_{DSS} = −100 μA (V_{DS} = −250V)
  N Channel I_{DSS} = 100 μA (V_{DS} = 250V)
- Enhancement-mode
  : P Channel V_{th} = −1.5~−3.5 V (V_{DS} = −10 V, I_D = −1 mA)
  : N Channel V_{th} = 1.5~3.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



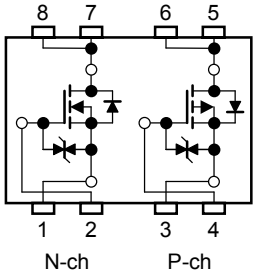
JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.080 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating		Unit
			P Channel	N Channel	
Drain-source voltage		V_{DSS}	−250	250	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−250	250	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	DC (Note 1)	I_D	−0.9	1.1	A
	Pulse (Note 1)	I_{DP}	−3.9	4.4	
Drain power dissipation (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$P_{D(1)}$	1.5	1.5	W
	Single-device value at dual operation (Note 3b)	$P_{D(2)}$	1.1	1.1	
Drain power dissipation (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$P_{D(1)}$	0.75	0.75	
	Single-device value at dual operation (Note 3b)	$P_{D(2)}$	0.45	0.45	
Single pulse avalanche energy		E_{AS}	0.49 (Note 4a)	0.49 (Note 4b)	mJ
Avalanche current		I_{AR}	−0.9	1.1	A
Repetitive avalanche energy Single-device value at operation (Note 2a, 3b, 5)		E_{AR}	0.11		mJ
Channel temperature		T_{ch}	150		°C
Storage temperature range		T_{stg}	−55~150		°C

Circuit Configuration



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

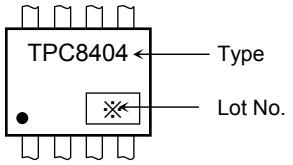
Note: (Note 1), (Note 2ab), (Note 3ab), (Note 4), (Note 5) Please see next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	114	
Thermal resistance, channel to ambient (t = 10s) (Note 2b)	Single-device operation (Note 2a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 2b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

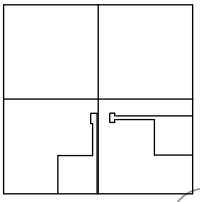
Marking



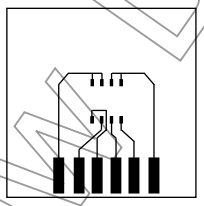
Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2:

a) Device mounted on a glass-epoxy board (a) b) Device mounted on a glass-epoxy board (b)



(a)



(b)

Note 3:

a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.).

b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.).

Note 4:

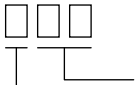
a) V_{DD} = −50 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = −0.9 A

b) V_{DD} = 50 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 1.1 A

Note 5: Repetitive rating; pulse width limited by max channel temperature.

Note 6: • on lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)

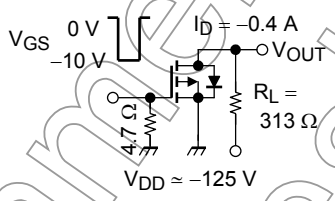


Week of manufacture
(01 for first week of year, continues up to 52 or 53)

Year of manufacture
(One low-order digits of calendar year)

P-ch

Electrical Characteristics (Ta = 25°C)

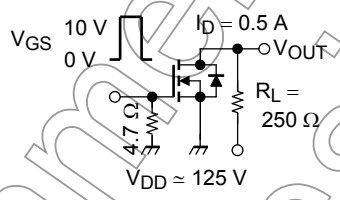
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = −250 V, V_{GS} = 0 V	—	—	−100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−250	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−1.5	—	−3.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −10 V, I_D = −0.9 A	—	1.85	2.55	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −0.4 A	0.4	1.1	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	381	—	pF
Reverse transfer capacitance		C_{rss}		—	52	—	
Output capacitance		C_{oss}		—	157	—	
Switching time	Rise time	t_r		—	8	—	ns
	Turn-ON time	t_{on}		—	20	—	
	Fall time	t_f		—	17	—	
	Turn-OFF time	t_{off}		—	60	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −200 V, V_{GS} = −10 V, I_D = −0.9 A	—	12	—	nC
Gate-source charge 1		Q_{gs}		—	7	—	
Gate-drain (“miller”) charge		Q_{gd}		—	5	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−3.6	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −0.9 A, V_{GS} = 0 V	—	—	2.0	V
Reverse recovery time		t_{rr}	I_{DR} = −0.9 A, V_{GS} = 0 V	—	110	—	V
Reverse recovery charge		Q_{rr}	dI_{DR}/dt = -100A/μsV	—	550	—	V

N-ch

Electrical Characteristics (Ta = 25°C)

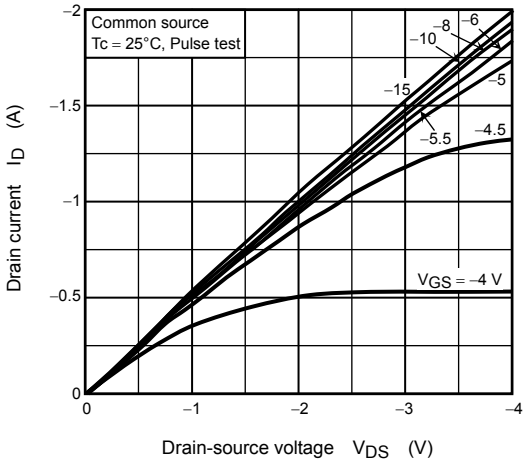
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	250	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 1.1 A	—	1.2	1.7	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 0.5 A	0.5	1.3	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	267	—	pF
Reverse transfer capacitance		C_{rss}		—	32	—	
Output capacitance		C_{oss}		—	98	—	
Switching time	Rise time	t_r		—	6	—	ns
	Turn-ON time	t_{on}		—	15	—	
	Fall time	t_f		—	10	—	
	Turn-OFF time	t_{off}		—	35	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 200 V, V_{GS} = 10 V, I_D = 1.1 A	—	10	—	nC
Gate-source charge 1		Q_{gs}		—	6	—	
Gate-drain (“miller”) charge		Q_{gd}		—	4	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

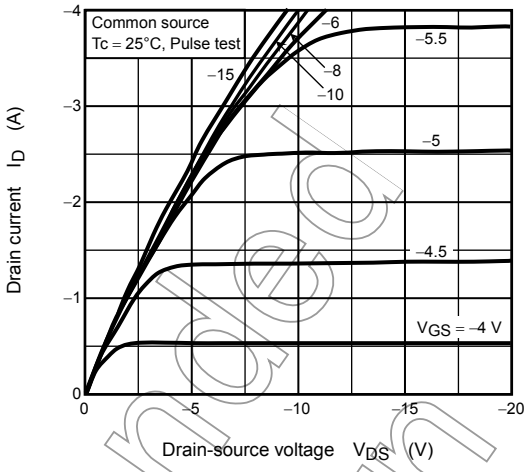
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	4.4	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 1.1 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time		t_{rr}	I_{DR} = 1.1 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	100	—	ns
Reverse recovery charge		Q_{rr}		—	320	—	nC

P-ch

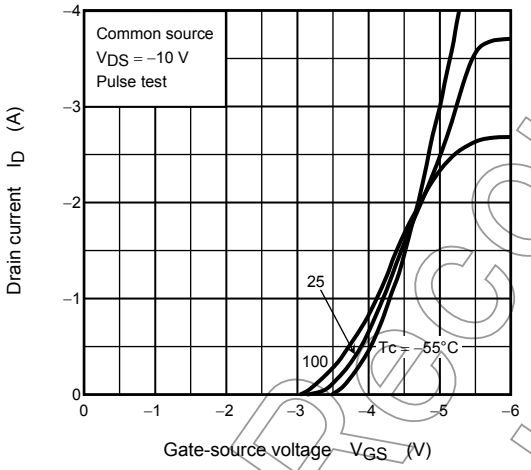
$I_D - V_{DS}$



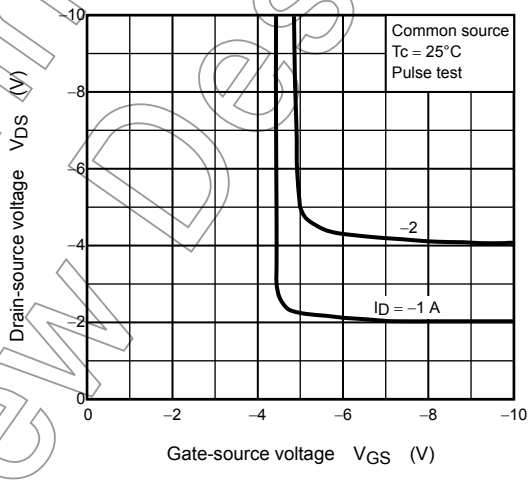
$I_D - V_{DS}$



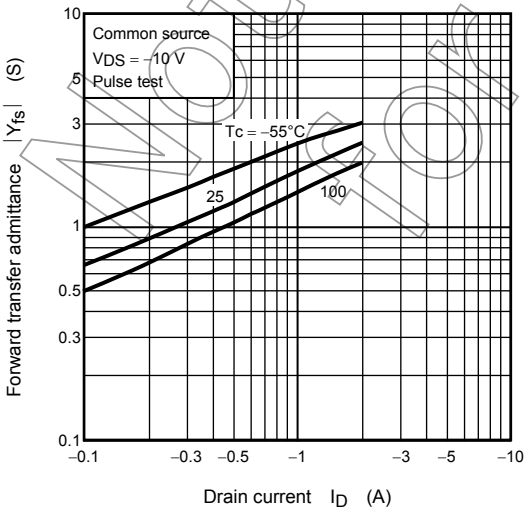
$I_D - V_{GS}$



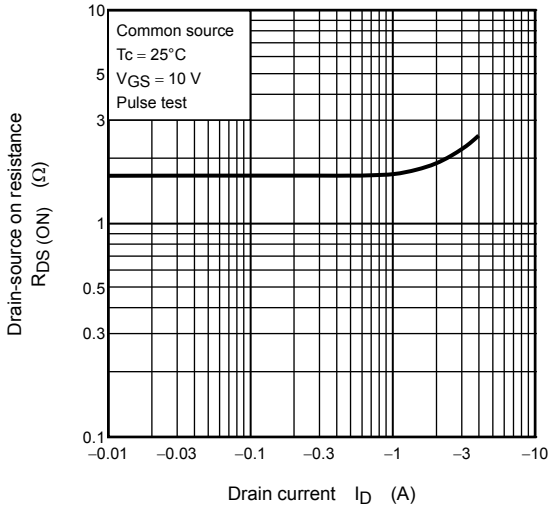
$V_{DS} - V_{GS}$



$|Y_{fs}| - I_D$

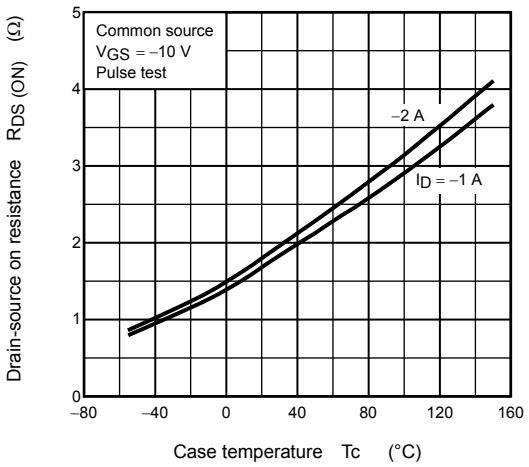


$R_{DS\ (ON)} - I_D$

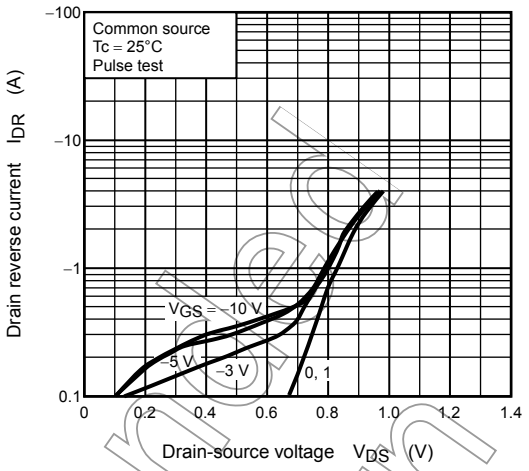


P-ch

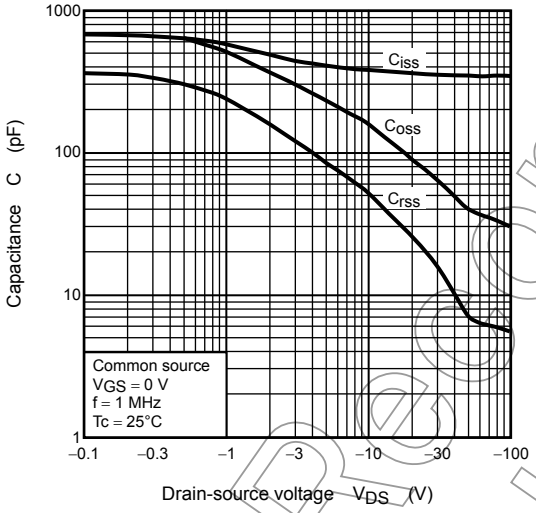
$R_{DS\ (ON)}$ – Tc



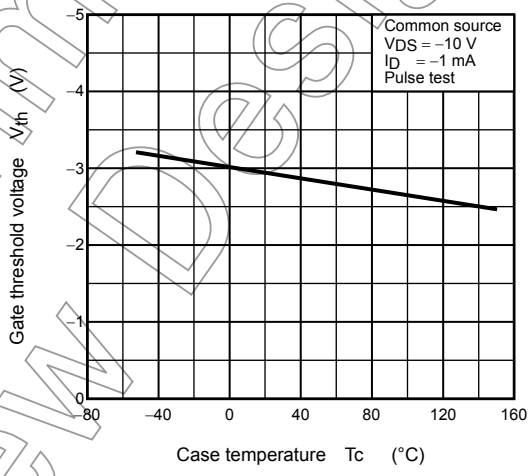
I_{DR} – V_{DS}



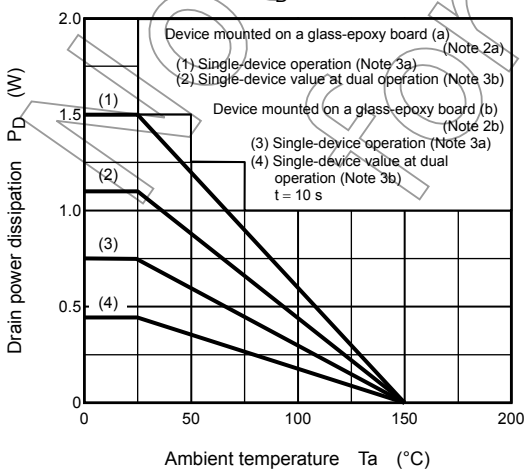
Capacitance – V_{DS}



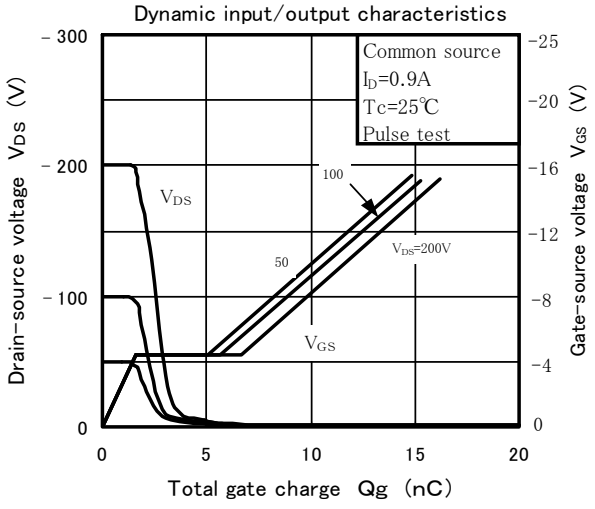
V_{th} – Tc



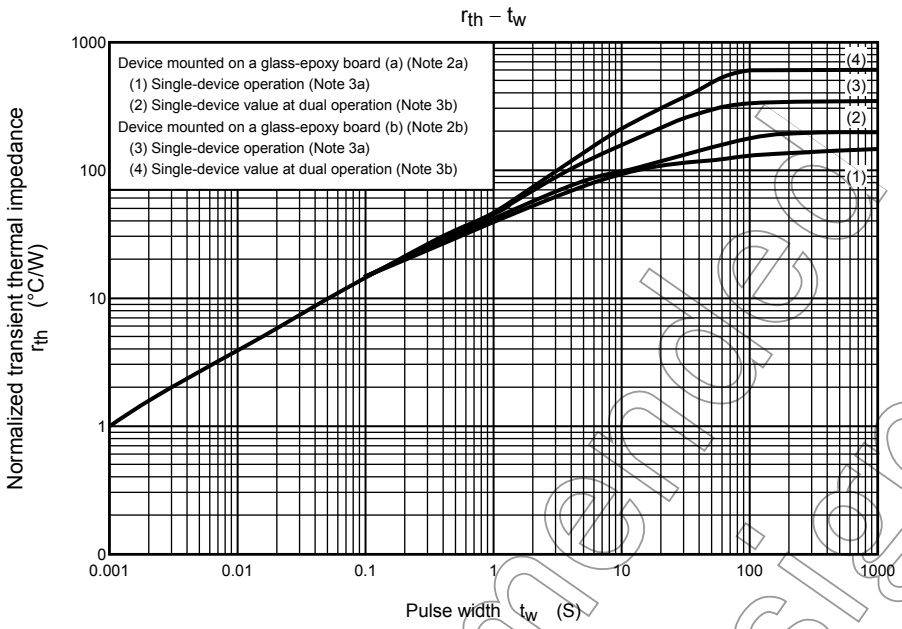
P_D – Ta

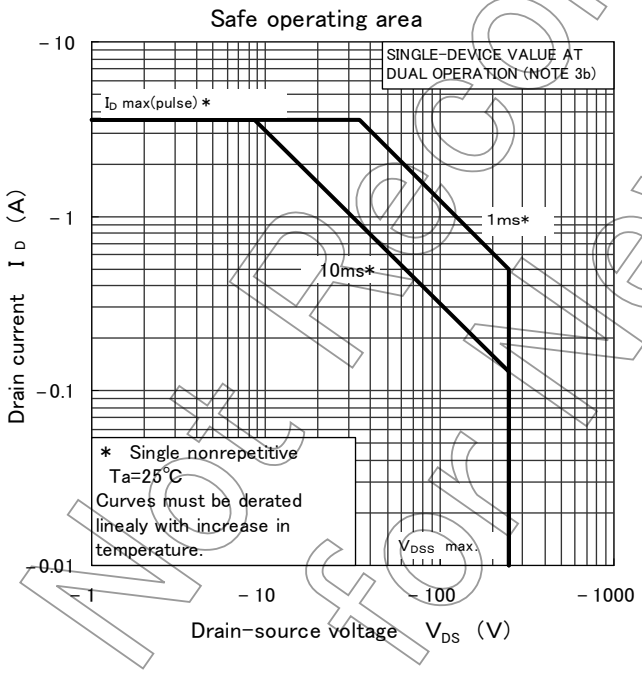


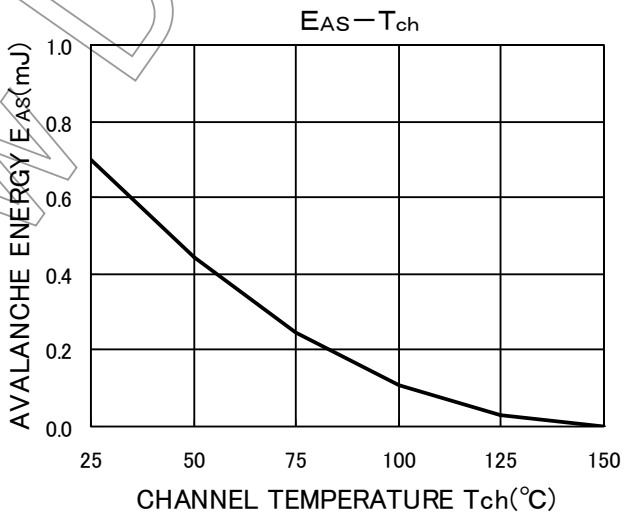
Dynamic input/output characteristics

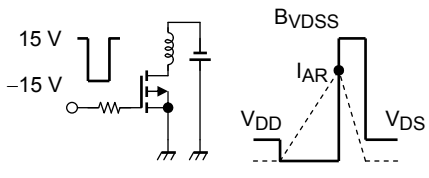


P-ch









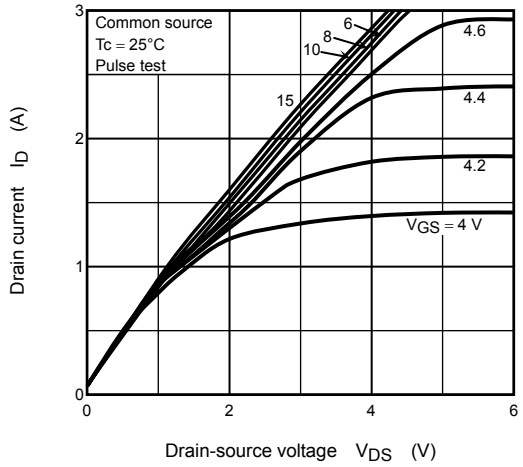
Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = -50$ V, L = 1 mH

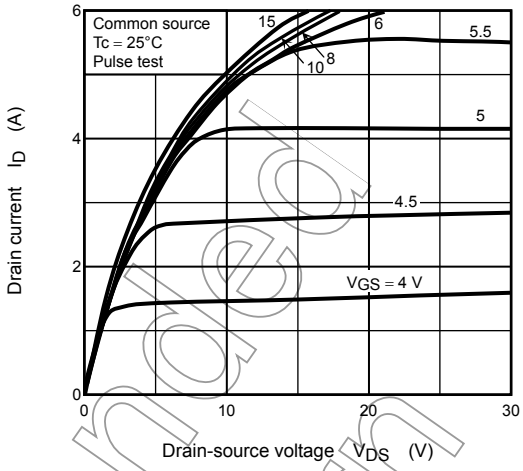
$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

N-ch

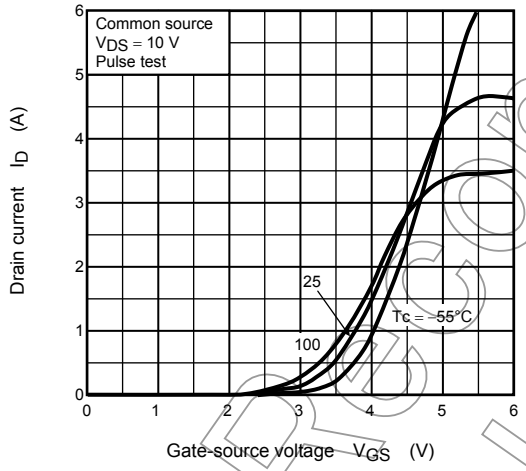
$I_D - V_{DS}$



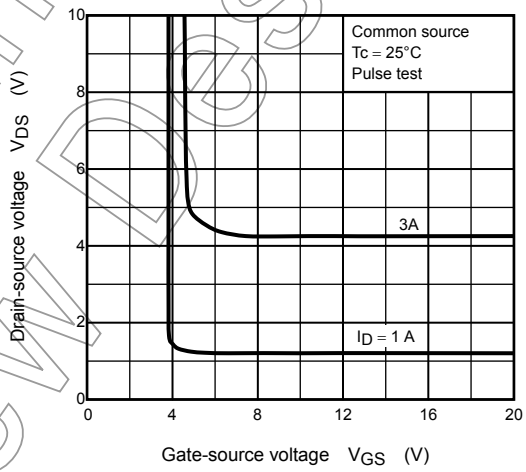
$I_D - V_{DS}$



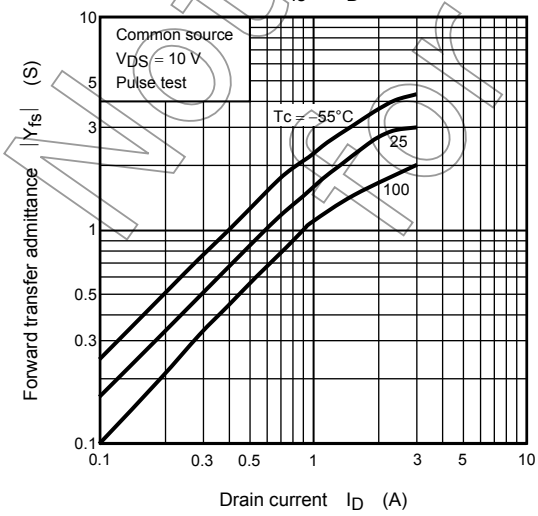
$I_D - V_{GS}$



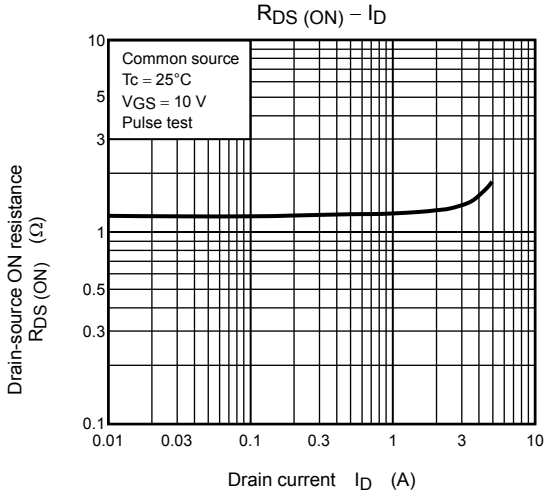
$V_{DS} - V_{GS}$



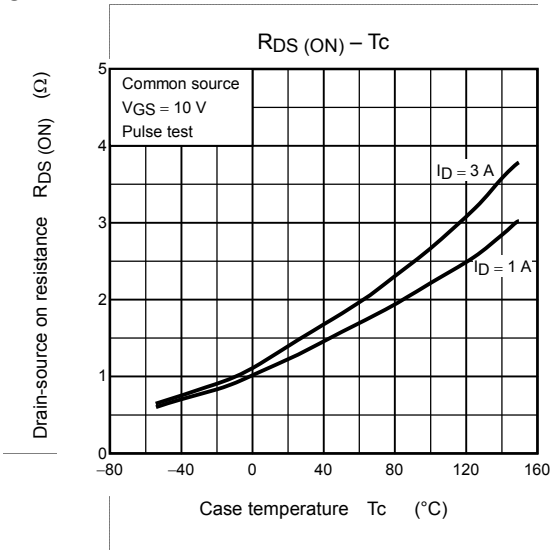
$|Y_{fs}| - I_D$

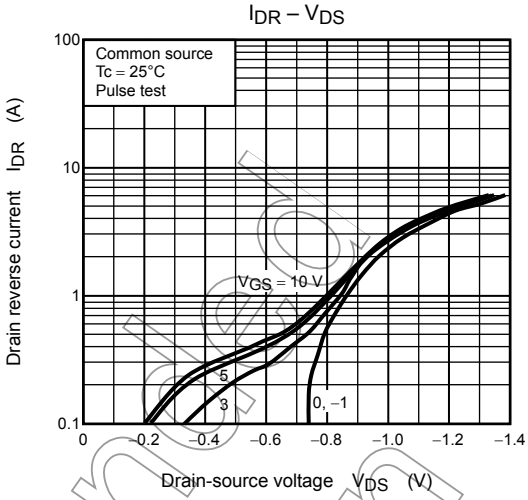


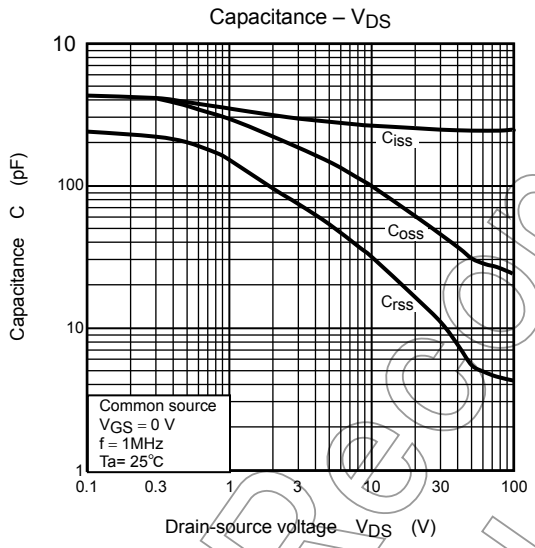
$R_{DS\ (ON)} - I_D$

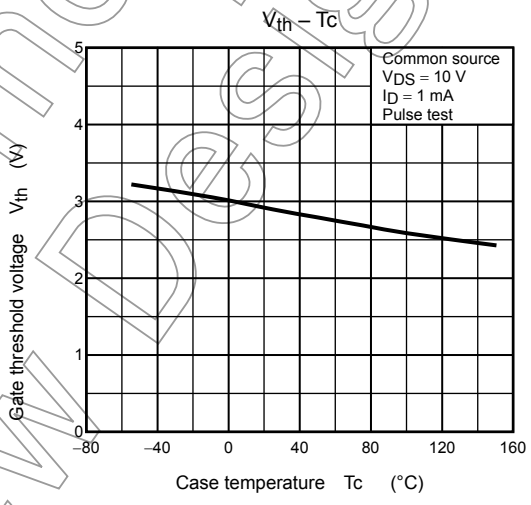


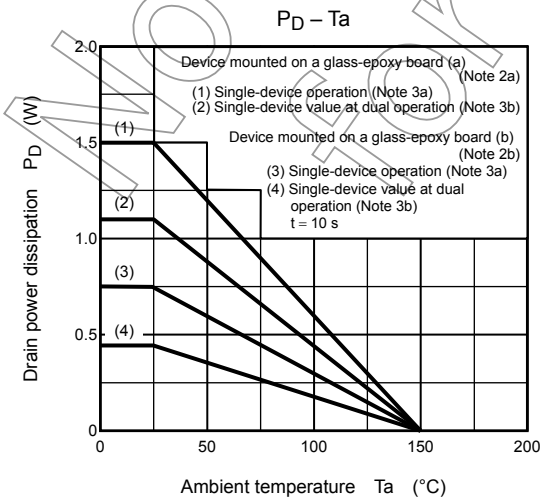
N-ch

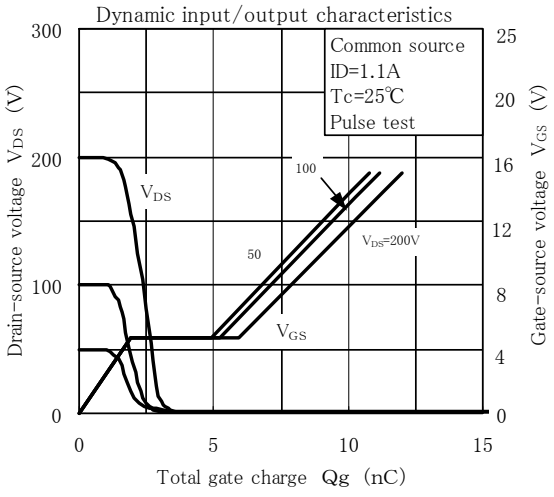






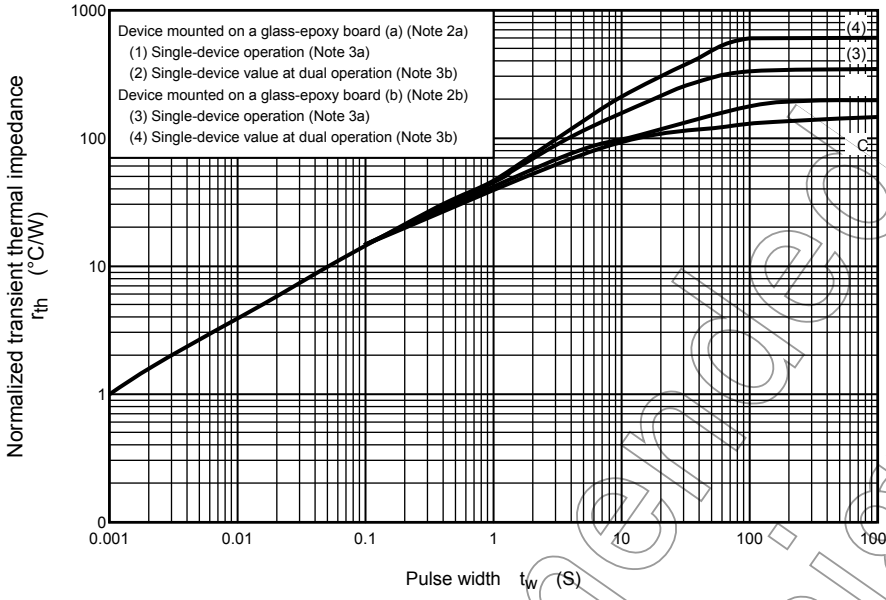




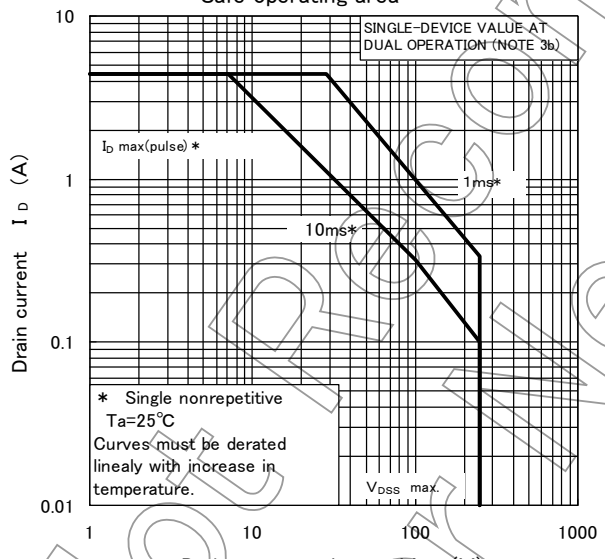


N-ch

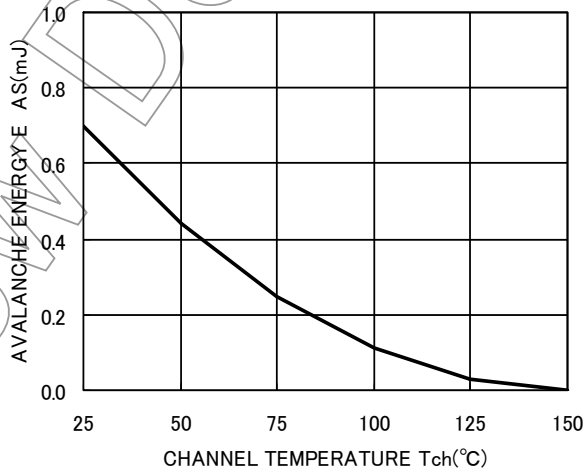
$r_{th} - t_w$

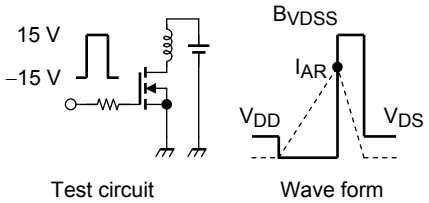


Safe operating area



EAS−Tch





$R_G = 25\ \Omega$
$V_{DD} = 50$ V, L = 1 mH

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