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TOSHIBA Transistor Silicon NPN Epitaxial Type

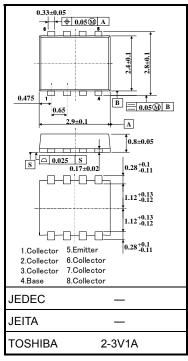
TPCP8501

Switching Applications DC-DC Converter Applications

- High DC current gain : $h_{FE} = 100$ to 300 (IC = 0.3 A)
- Low collector-emitter saturation : VCE (sat) = 0.2 V (max)
- High-speed switching : tf = 100 ns (typ.)

Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit | |
|--|----------------|------------------|------------|------|--|
| Collector-base voltage | | V _{CBO} | 180 | V | |
| Collector-emitter voltage | | V _{CEX} | 150 | V | |
| | | V _{CEO} | 100 | | |
| Emitter-base voltage | | V _{EBO} | 7 | V | |
| Collector current | DC (Note 1) | Ι _C | 2.0 | А | |
| | Pulse (Note 1) | I _{CP} | 4.0 | | |
| Base current | | Ι _Β | 0.2 | А | |
| Collector power dissipation (t = 10s) | t = 10s | Pc (Note 2) | 3.3 | W | |
| | DC | FC (NOLE 2) | 1.3 | | |
| Junction temperature | | Тj | 150 | °C | |
| Storage temperature range | | T _{stg} | -55 to 150 | °C | |



Weight: 0.017 g (typ.)

Note 1: Please use devices on condition that the junction temperature is below 150 $^{\rm o}{\rm C}.$

Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²)

Note 3: • on lower left on the marking indicates Pin 1.

※ Weekly code: (Three digits)



Week of manufacture

— (01 for first week of year, continues up to 52 or 53)

- Year of manufacture

(One low-order digits of calendar year)

Figure 1. Circuit configuration (top view)

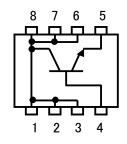
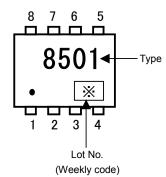


Figure 2. Marking (Note 3)



Unit: mm

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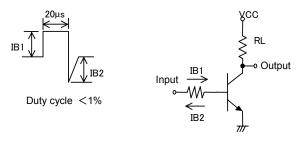


Electrical Characteristics (Ta = 25°C)

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| Characteristics | | Symbol | Test Condition | Min | Тур. | Max | Unit |
|--------------------------------------|--------------|-----------------------|---|-----|------|-----|------|
| Collector cut-off current | | I _{CBO} | $V_{CB} = 180 \text{ V}, \text{ I}_{E} = 0$ | _ | _ | 100 | nA |
| Emitter cut-off current | | I _{EBO} | $V_{EB}=7~V,~I_C=0$ | _ | _ | 100 | nA |
| Collector-base breakdown voltage | | V (BR) CBO | $I_C=1\ mA,\ I_B=0$ | 180 | _ | _ | V |
| Collector-emitter breakdown voltage | | V (BR) CEO | $I_C = 10 \text{ mA}, I_B = 0$ | 100 | _ | _ | V |
| DC current gain | | h _{FE} (1) | $V_{CE} = 2 V, I_C = 0.3 A$ | 100 | | 300 | |
| | | h _{FE} (2) | $V_{CE} = 2 V, I_C = 1.0 A$ | 80 | | | |
| Collector-emitter saturation voltage | | V _{CE (sat)} | $I_{C} = 1 \text{ A}, I_{B} = 33 \text{ mA}$ | _ | _ | 0.2 | V |
| Base-emitter saturation voltage | | V _{BE (sat)} | $I_{C} = 1 \text{ A}, I_{B} = 33 \text{ mA}$ | _ | | 1.1 | V |
| Collector output capacitance | | C _{ob} | $V_{CB} = 10 \text{ V}, \text{ I}_{E} = 0, \text{ f} = 1 \text{MHz}$ | _ | 23 | _ | pF |
| Switching time | Rise time | tr | See Figure 3 circuit diagram $V_{CC} \simeq 50 \text{ V}, \text{ R}_L = 50 \Omega$ $I_{B1} = -I_{B2} = 33 \text{ mA}$ | _ | 65 | | ns |
| | Storage time | t _{stg} | | _ | 1.4 | _ | μs |
| | Fall time | t _f | | | 100 | | ns |

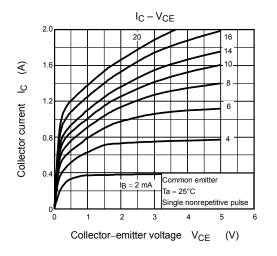
Figure 3. Switching Time Test Circuit & Timing Chart

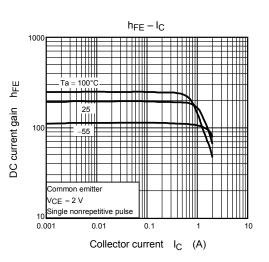


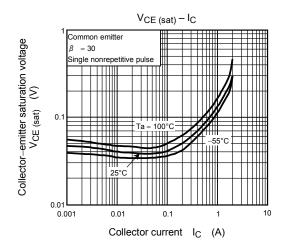
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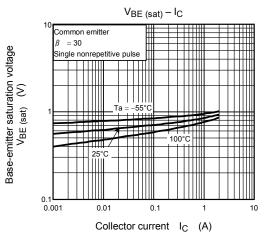
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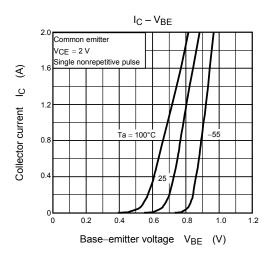
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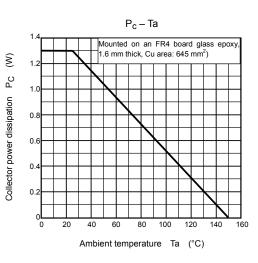






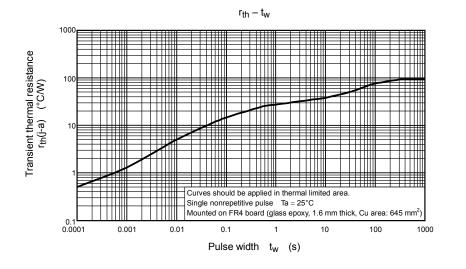


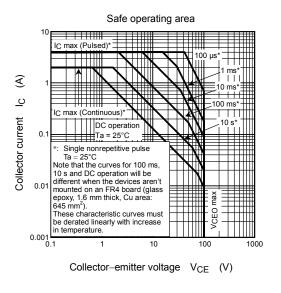




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