

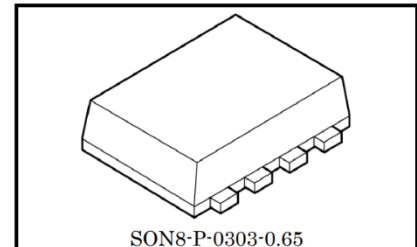
Toshiba Intelligent Power Device Silicon Monolithic MOS Integrated Circuit

# TPD1044F

Low-Side Switch for Motor, Solenoid and Lamp Drive

## 1. Description

The TPD1044F is a low-side switch. The IC has a vertical MOSFET output which can be directly driven from a CMOS or TTL logic circuit (e.g., an MPU). The IC is equipped with intelligent self-protection functions.



Weight: 0.017 g (typ.)

## 2. Applications

Motor drive, solenoid drive, lamp drive.

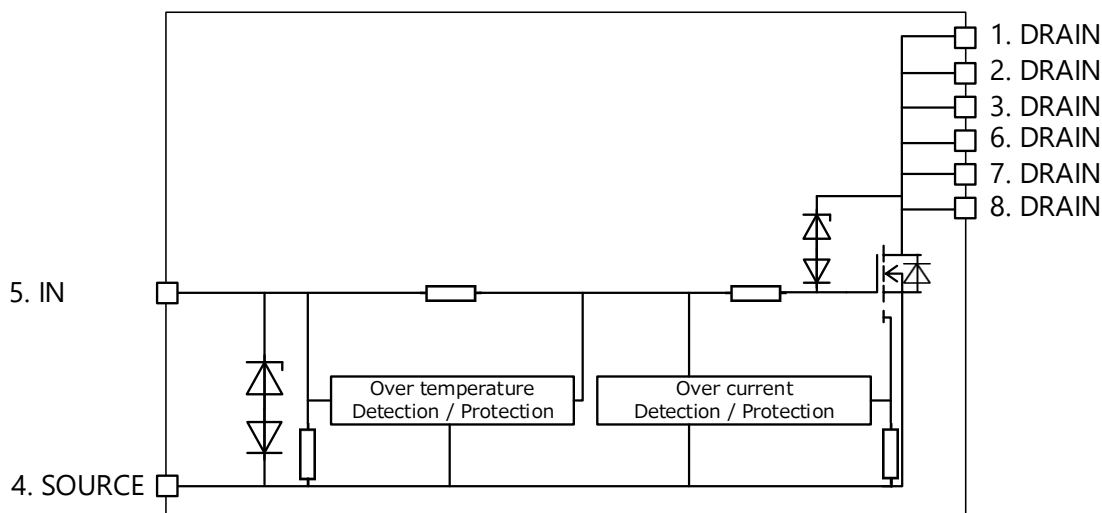
## 3. Features

- A monolithic IC with a new structure combining a control block and a vertical MOSFET on single chip.
- Can directly drive a power load from a CMOS or TTL logic IC.
- Built-in protection circuits against overvoltage (active clamp), overtemperature (thermal shutdown), and overcurrent (current limiter).
- Low Drain-Source ON-resistance:  $R_{DS(ON)} = 0.6 \Omega$  (max) (@ $V_{IN} = 5 \text{ V}$ ,  $I_D = 0.5 \text{ A}$ ,  $T_{ch} = 25 \text{ }^\circ\text{C}$ )
- Low Drain cut-off Current:  $I_{DSS} = 10 \mu\text{A}$  (max) (@ $V_{IN} = 0 \text{ V}$ ,  $V_{DS} = 30 \text{ V}$ ,  $T_{ch} = 25 \text{ }^\circ\text{C}$ )
- Low Input Current:  $I_{IN} = 300 \mu\text{A}$  (max) (@ $V_{IN} = 5 \text{ V}$ ,  $T_{ch} = 25 \text{ }^\circ\text{C}$ )
- AEC-Q100 qualified.
- It is a surface-mounted package "PS-8" (named by Toshiba), and the packing is embossed-tape packing.

Note : Due to its MOS structure, this product is sensitive to static electricity.

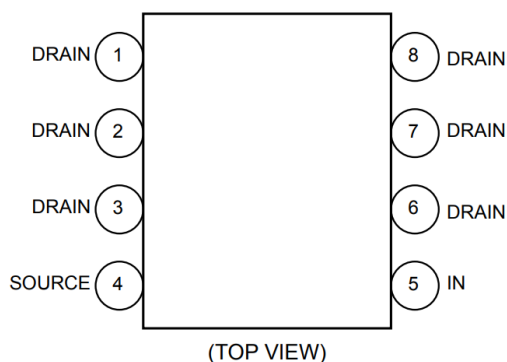
Start of commercial production  
2003-09

### 4. Block Diagram



**Figure 4.1 Block Diagram**

### 5. Pin Assignments (Top view)



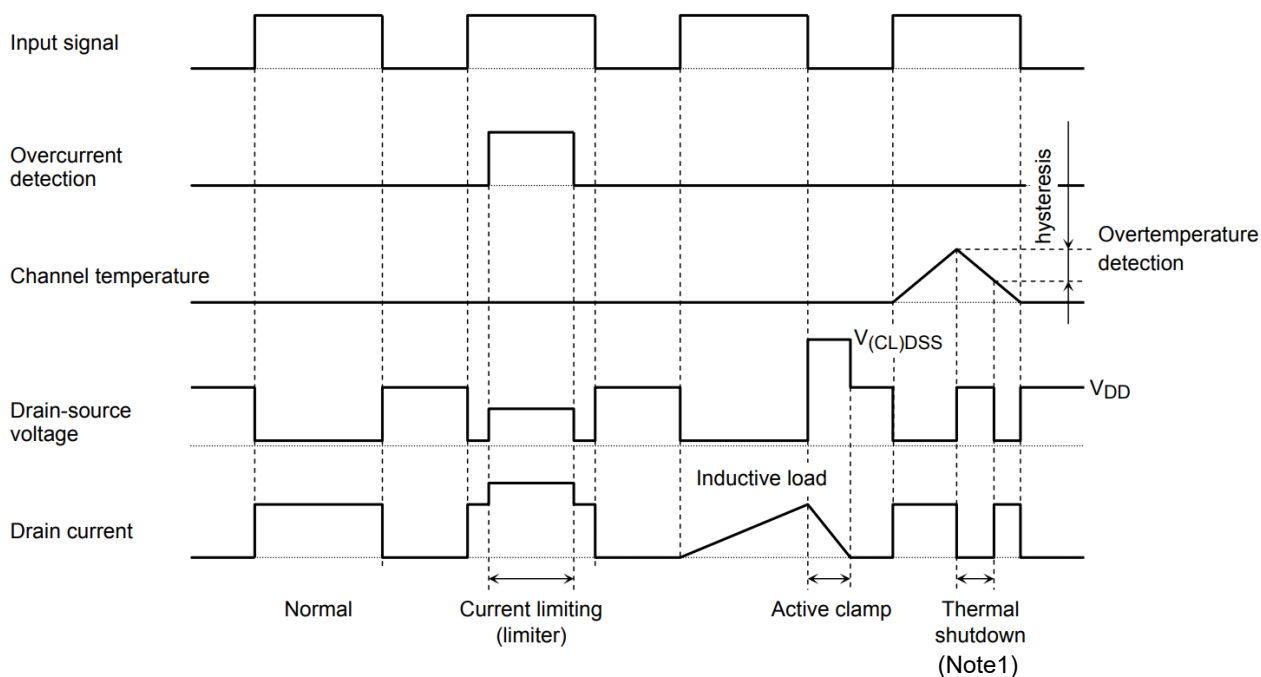
**Figure 5.1 Pin Assignments (Top view)**

### 6. Pin Description

**Table 6.1 Pin Description**

Pin No.	Symbol	Description
1,2,3,6,7,8	DRAIN	Drain current is limited (by current limiter) if it exceeds 1 A (min) in order to protect the IC.
4	SOURCE	Source pin.
5	IN	Input pin. This pin is connected to a pull-down resistor internally, so that even when input wiring is open-circuited, output can never be turned on inadvertently.

## 7. Timing chart



**Figure 7.1** Timing chart

Note 1: The overtemperature detection is self-recovery. The detection and recovery hysteresis is 5 °C (typ.).

## 8. Truth table

**Table 8.1** Truth table

IN	$V_{DS}$	Output state	Operation state
L	H	OFF	Normal
H	L	ON	
L	H	OFF	Overcurrent (load short)
H	H	current limiting (limiter)	
L	H	OFF	Overtemperature
H	H	OFF	

## 9. Absolute Maximum Ratings

**Table 9.1 Absolute Maximum Ratings (Ta = 25 °C) (Note)**

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V <sub>DS (DC)</sub>	41	V
Drain current	I <sub>D</sub>	Internally limited	A
Input voltage	V <sub>IN</sub>	-0.3 to 7.0	V
Power dissipation (Ta = 25 °C) (Note 1)	P <sub>D</sub>	0.9	W
Single pulse active clamp capability (Note 2)	E <sub>AS</sub>	125	mJ
Active clamp current	I <sub>AR</sub>	1	A
Repetitive active clamp capability (Note 3)	E <sub>AR</sub>	0.09	mJ
Operating temperature	T <sub>opr</sub>	-40 to 125	°C
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Refer to 10. Thermal Characteristics.

Note 2: Active clamp capability (single pulse) test condition V<sub>DS</sub> = 40 V, T<sub>ch</sub> = 25°C(initial), L = 50 mH, I<sub>AR</sub> = 1 A, R<sub>G</sub> = 25 Ω

Note 3: Repetitive rating, pulse width limited by maximum channel temperature.

## 10. Thermal Characteristics

**Table 10.1 Thermal characteristics**

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (Note 4)	R <sub>th (ch-a)</sub>	138.9	°C/W

$$P_D = (T_{ch} - T_a) / R_{th (ch-a)}$$

Note 4: Thermal resistance measurement conditions.

Mounted on glass epoxy board (FR-4) [25.4 mm × 25.4 mm × 0.8 mm]



## 11. Electrical Characteristics

Table 11.1 Electrical Characteristics (Ta = 25 °C)

Characteristics	Symbol	Test circuit	Test Condition	Min	Typ.	Max	Unit
Drain-source clamp voltage	$V_{(CL)DSS}$	-	$V_{IN} = 0\text{ V}$ , $I_D = 1\text{ mA}$	41	-	60	V
Input threshold voltage	$V_{th}$	-	$V_{DS} = 13\text{ V}$ , $I_D = 10\text{ mA}$	1.0	-	2.8	V
Protective circuit operation input voltage range	$V_{IN(opr)}$	-	-	3	-	6	V
Drain cut-off current	$I_{DSS}$	-	$V_{IN} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$	-	-	10	$\mu\text{A}$
Input current	$I_{IH(1)}$	-	$V_{IN} = 5\text{ V}$ , at normal operation	-	-	300	$\mu\text{A}$
	$I_{IH(2)}$	-	$V_{IN} = 5\text{ V}$ , when overcurrent protective circuit is actuated	-	-	350	
Drain-source on resistance	$R_{DS(ON)}$	-	$V_{IN} = 5\text{ V}$ , $I_D = 0.5\text{ A}$	-	0.44	0.60	$\Omega$
Overtemperature detection	$T_{OT}$	-	$V_{IN} = 5\text{ V}$	150	160	-	$^{\circ}\text{C}$
Overcurrent detection	$I_{OC}$	1	$V_{IN} = 5\text{ V}$	1.0	1.8	-	A
Switching time	$t_{on}$	2	$V_{DD} = 13\text{ V}$ , $V_{IN} = 0\text{ V} / 5\text{ V}$ , $I_D = 0.5\text{ A}$	-	10	-	$\mu\text{s}$
	$t_{off}$			-	15	-	

Test circuit 1: Overcurrent measuring circuit

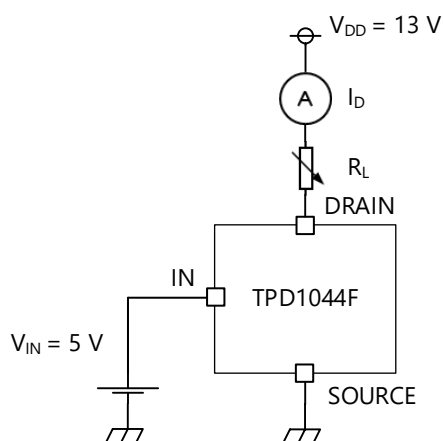


Figure 11.1 Test circuit 1

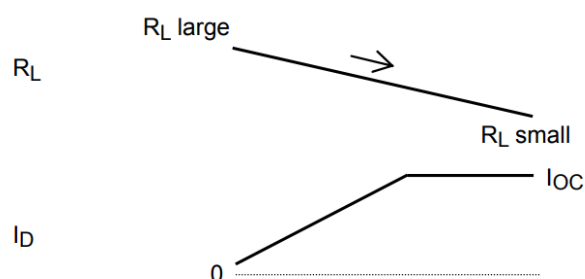


Figure 11.2 Measured waveforms 1

Test circuit 2: Switching time measuring circuit

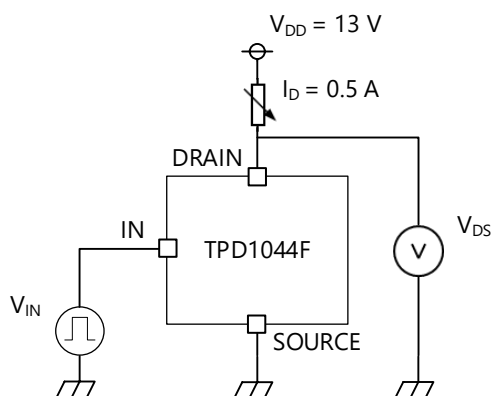


Figure 11.3 Test circuit 2

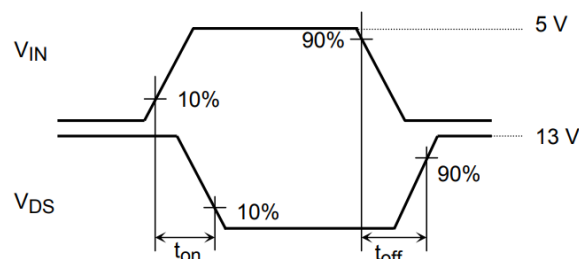


Figure 11.4 Measured waveforms 2

## 12. Characteristic curves

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

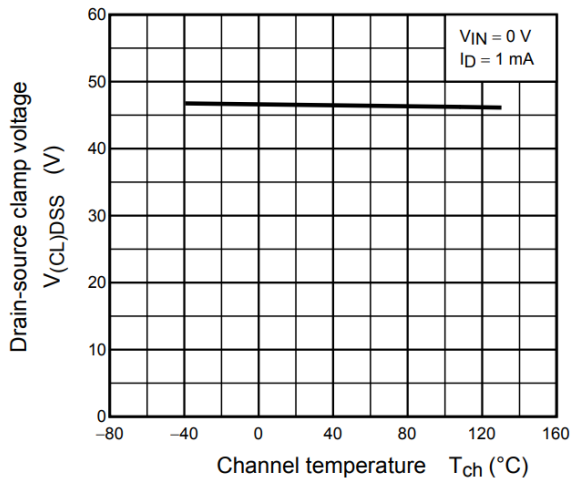


Figure 12.1  $V_{(CL)DSS} - T_{ch}$

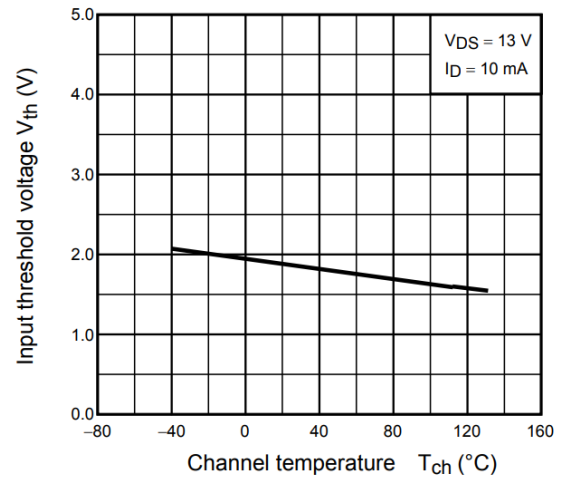


Figure 12.2  $V_{th} - T_{ch}$

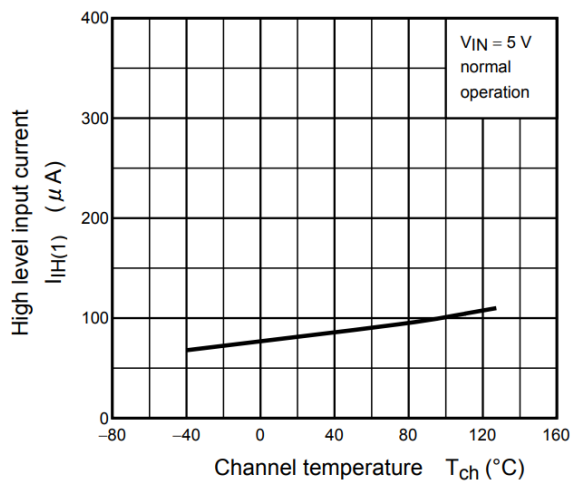


Figure 12.3  $I_{iH(1)} - T_{ch}$

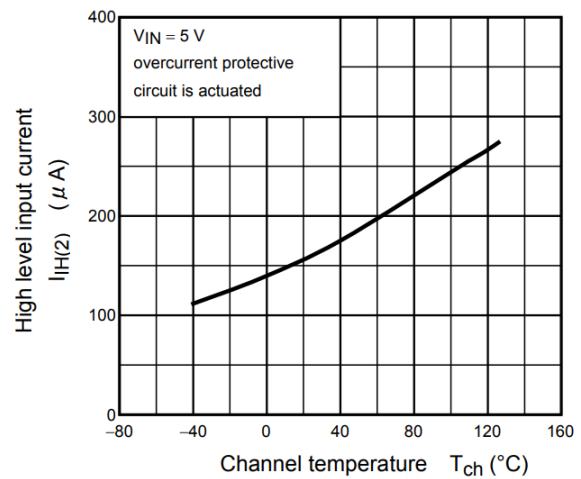


Figure 12.4  $I_{iH(2)} - T_{ch}$

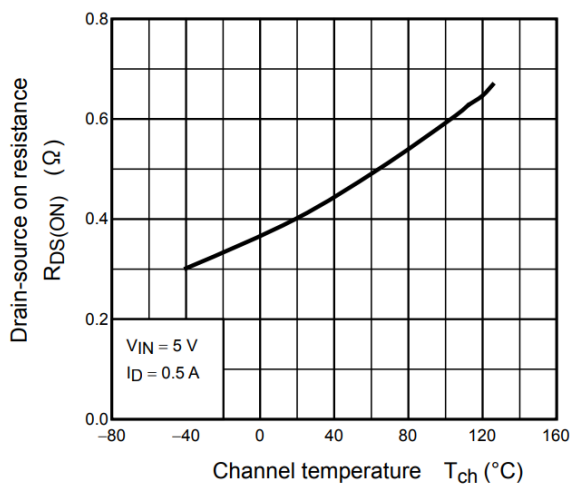


Figure 12.5  $R_{DS(ON)} - T_{ch}$

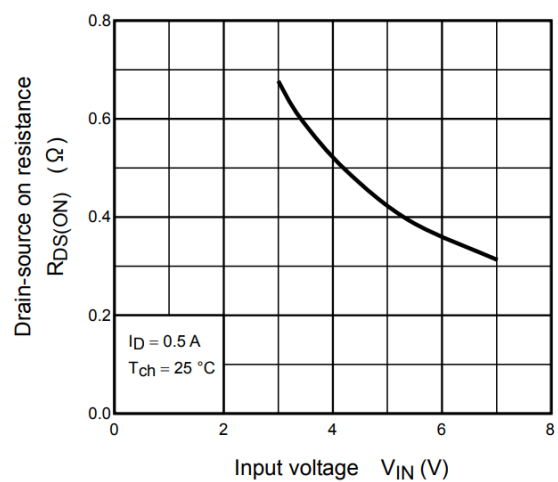


Figure 12.6  $R_{DS(ON)} - V_{IN}$

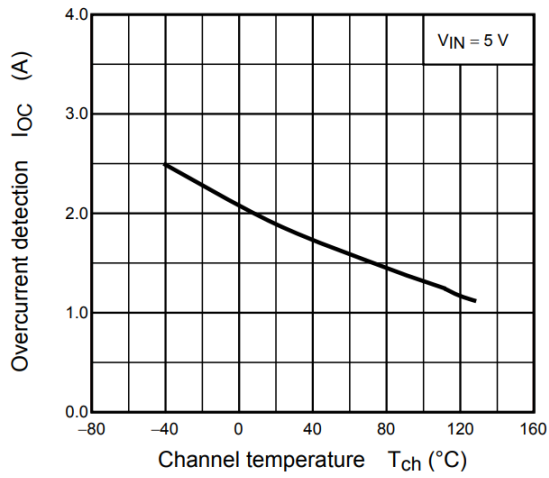


Figure 12.7  $I_{OC} - T_{ch}$

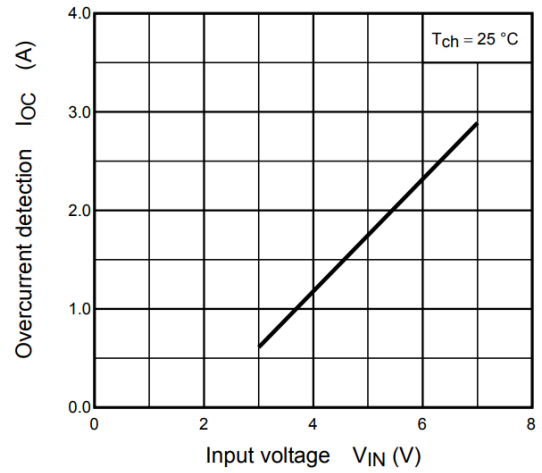


Figure 12.8  $I_{OC} - V_{IN}$

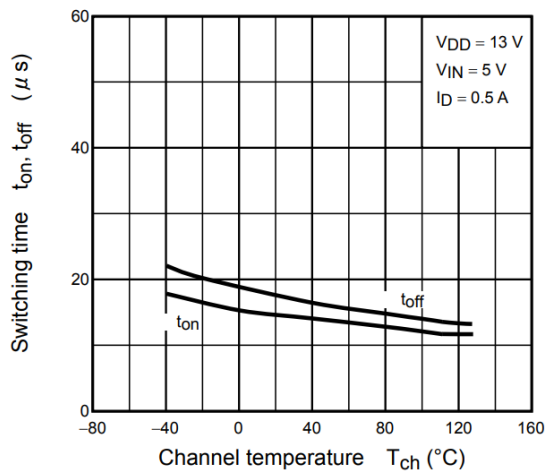


Figure 12.9  $t_{on}, t_{off} - T_{ch}$

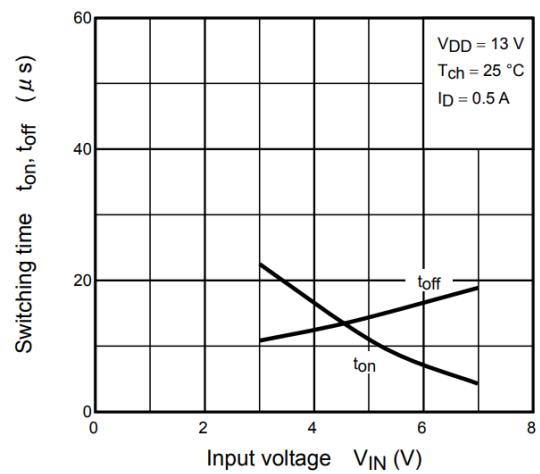


Figure 12.10  $t_{on}, t_{off} - V_{IN}$

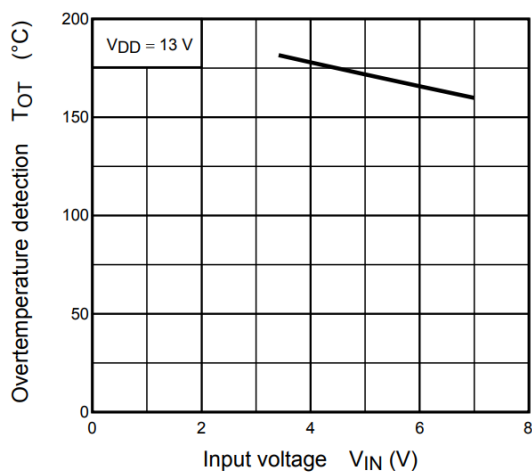


Figure 12.11  $T_{OT} - V_{IN}$

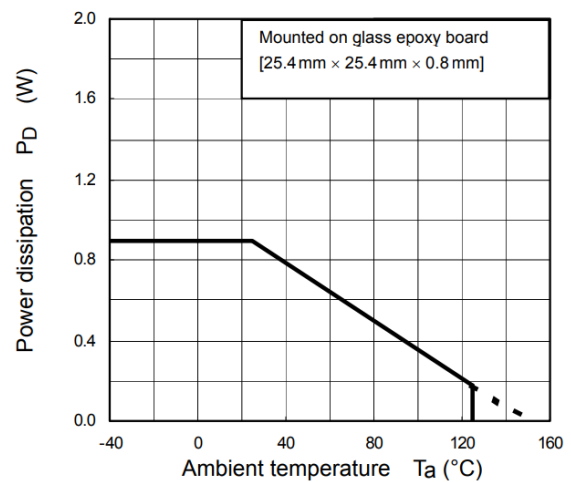


Figure 12.12  $P_D - T_a$

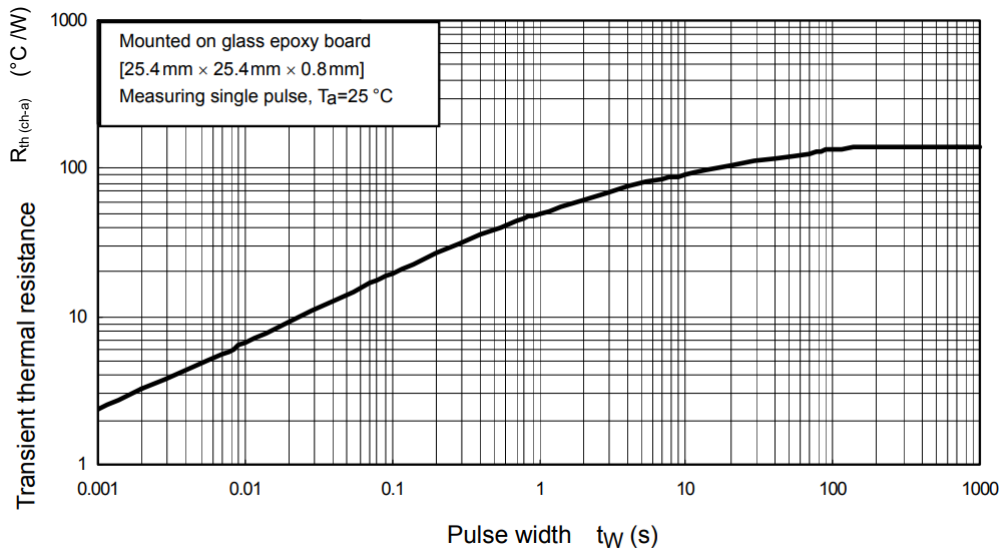
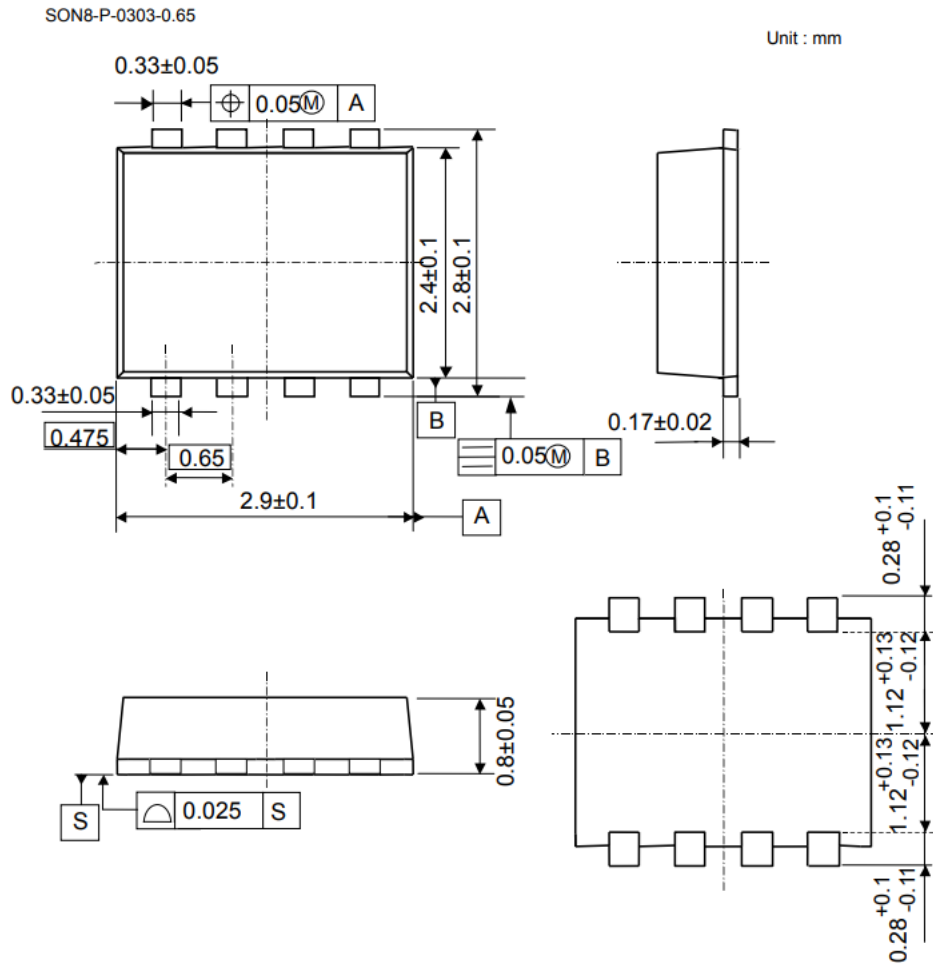


Figure 12.13  $R_{th(ch-a)} - t_w$



**13. Package Information**

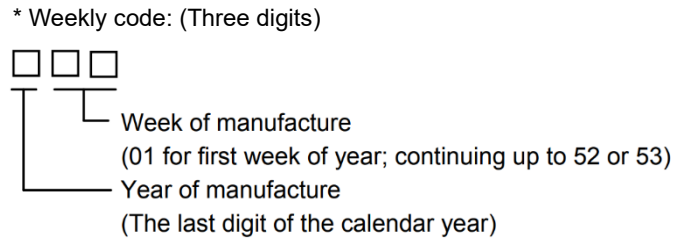
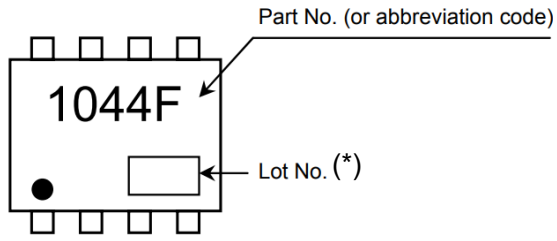
**13.1. Package Dimensions**



Weight: 0.017 g (Typ.)

**Figure 13.1 Package Dimensions**

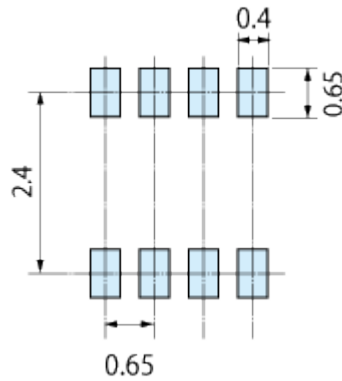
**13.2. Marking**



**Figure 13.2 Marking**

Note: The (●) on the lower left of the marking indicates Pin 1.

**13.3. Land Pattern Dimensions for Reference only**



**Figure 13.3 Land Pattern Dimensions for Reference only**

## **14. IC Usage Considerations**

### **14.1. Notes on Handling of ICs**

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. None of the multiple ratings can be exceeded. Exceeding the absolute maximum ratings may cause destruction, damage and deterioration, and may result in injury due to explosion or burning.

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