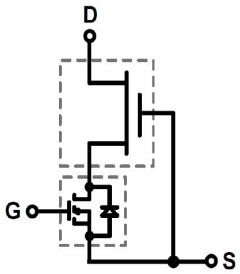
PRODUCT SUMMARY (TYPICAL)	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	0.15
Q_{rr} (nC)	54

GaN Power Low-loss Switch



TO-220 Package

Features

- Low Q_{rr}
- Free-wheeling diode not required
- High-side Quiet Tab™ for reduced EMI
- GSD pin layout improves high speed design
- RoHS compliant
- High frequency operation

Applications

- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies

Absolute Maximum Ratings (T_C=25 °C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous Drain Current @T_C=25 °C		17	A
$I_{D100°C}$	Continuous Drain Current @T_C=100 °C		12	A
I_{DM}	Pulsed Drain Current (pulse width:100 μs)		60	A
V_{DSS}	Drain to Source Voltage		600	V
V_{TDS}	Transient Drain to Source Voltage [a]		750	V
V_{GSS}	Gate to Source Voltage		±18	V
$P_{D25°C}$	Maximum Power Dissipation		96	W
T_C	Operating Temperature	Case	-55 to 150	°C
T_J		Junction	-55 to 175	°C
T_S	Storage Temperature		-55 to 150	°C
T_{Csold}	Soldering peak Temperature [b]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{ΘJC}$	Junction-to-Case	1.55	°C /W
$R_{ΘJA}$	Junction-to-Ambient	62	°C /W

Notes

a: For 1 usec, duty cycle D=0.1

b: For 10 sec, 1.6mm from the case

Electrical Characteristics (T_C=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typical	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Maximum Drain-Source Voltage	600	-	-	V	V_{GS}=0 V
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS}=V_{GS}, I_D=1 mA
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 25 °C)	-	0.15	0.18	Ω	V_{GS}=8V, I_D =11A, T_J = 25 °C
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 175 °C)	-	0.33	-	Ω	V_{GS}=8V, I_D =11A,T_J = 175 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 25 °C	-	2.5	90	μA	V_{DS}=600V, V_{GS}=0V, T_J = 25 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 150 °C	-	10	-	μA	V_{DS}=600V, V_{GS}=0V, T_J = 150 °C
I_{GSS}	Gate-to-Source Forward Leakage Current	-	-	100	nA	V_{GS}= 18 V
	Gate-to-Source Reverse Leakage Current	-	-	-100		V_{GS}= -18 V
Dynamic						
C_{ISS}	Input Capacitance	-	740	-	pF	V_{GS}=0 V, V_{DS}=100 V, *f* =1 MHz
C_{OSS}	Output Capacitance	-	133	-		
C_{RSS}	Reverse Transfer Capacitance	-	3.6	-		
$C_{O(er)}$	Output Capacitance, energy related [a]	-	56	-		V_{GS}=0 V, V_{DS}=0 V to 480 V
$C_{O(tr)}$	Output Capacitance, time related [a]	-	110	-		
Q_g	Total Gate Charge [b]	-	6.2	9.3	nC	V_{DS} =100 V [a], V_{GS}= 0-4.5 V, I_D = 11 A
Q_{gs}	Gate-Source Charge	-	2.1	-		
Q_{gd}	Gate-Drain Charge	-	2.2	-		
$t_{d(on)}$	Turn-On Delay	-	4	-	ns	V_{DS} =480 V , V_{GS}= 0-10 V, I_D = 11 A, R_G= 2 Ω
t_r	Rise Time	-	3	-		
$T_{d(off)}$	Turn-Off Delay	-	10.5	-		
t_f	Fall Time	-	3.5	-		
Reverse operation						
I_S	Reverse Current	-	-	11	A	V_{GS}=0 V, T_J=100 °C
V_{SD}	Reverse Voltage	-	2.3	2.8	V	V_{GS}=0 V, I_S=11 A, T_J=25 °C
V_{SD}	Reverse Voltage	-	1.6	1.9	V	V_{GS}=0 V, I_S=5.5 A, T_J=25 °C
t_{rr}	Reverse Recovery Time	-	30	-	ns	I_S=11 A, V_{DD}=480 V, di/dt =450 A/μs, T_J=25 °C
Q_{rr}	Reverse Recovery Charge	-	54	-	nC	

Notes
a: Fixed while V_{DS} is rising from 0 to 80% V_{DSS} ;
b: Q_g does not change for V_{DS}>100 V.

Typical Characteristic Curves 25 °C unless otherwise noted

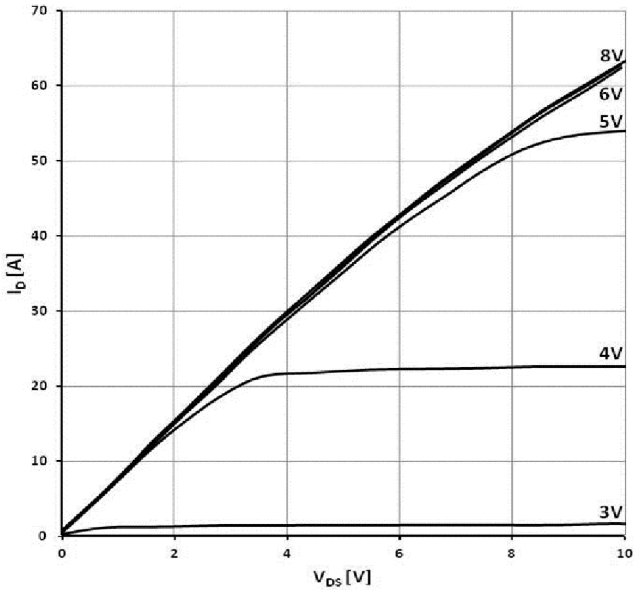


Fig. 1. Typical Output Characteristics T_J= 25 °C
Parameter: V_{GS}

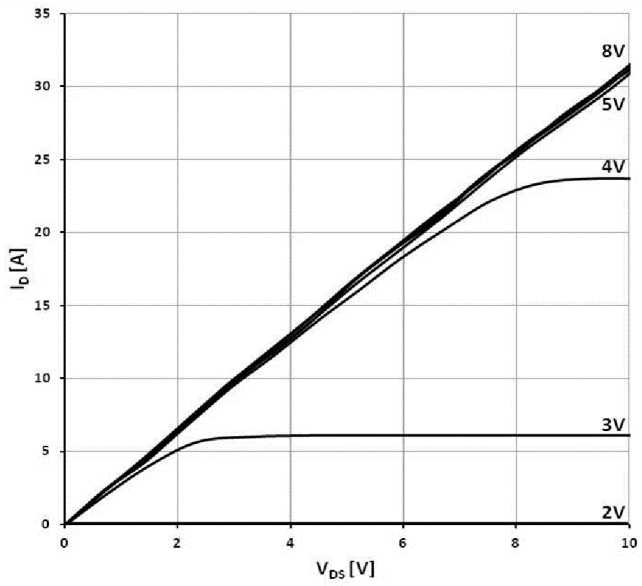


Fig. 2. Typical Output Characteristics T_J=175 °C
Parameter: V_{GS}

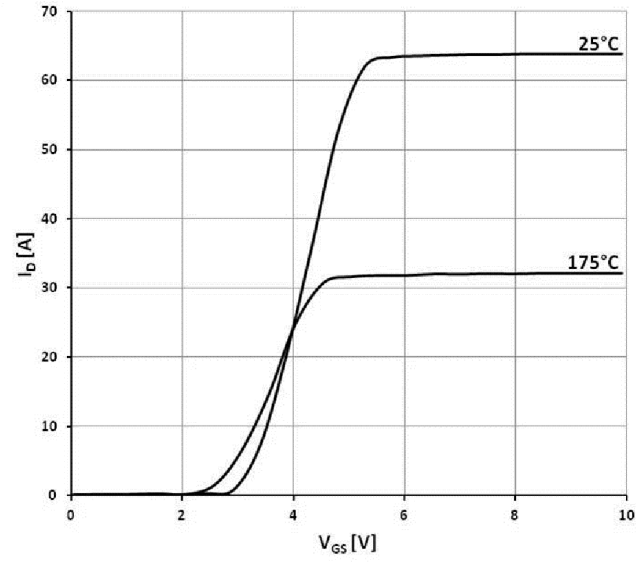


Fig. 3. Typical Transfer Characteristics
V_{DS}=10 V, Parameter: T_J

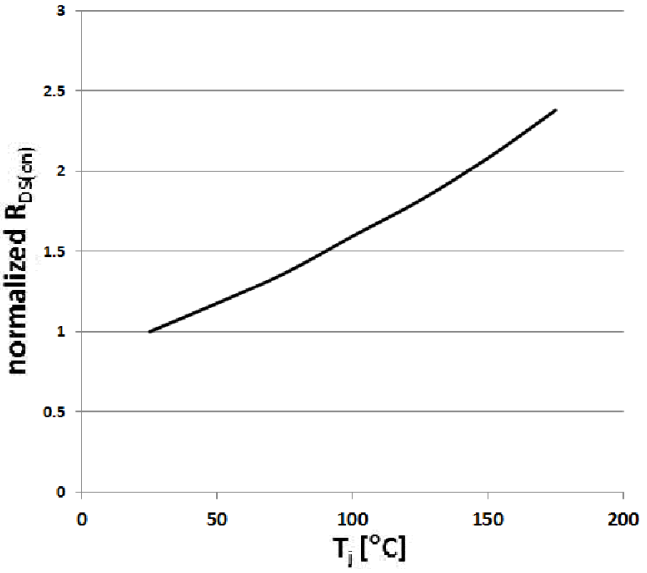


Fig. 4. Normalized On-Resistance
I_D=12 A, V_{GS}=8 V

Typical Characteristic Curves 25 °C unless otherwise noted

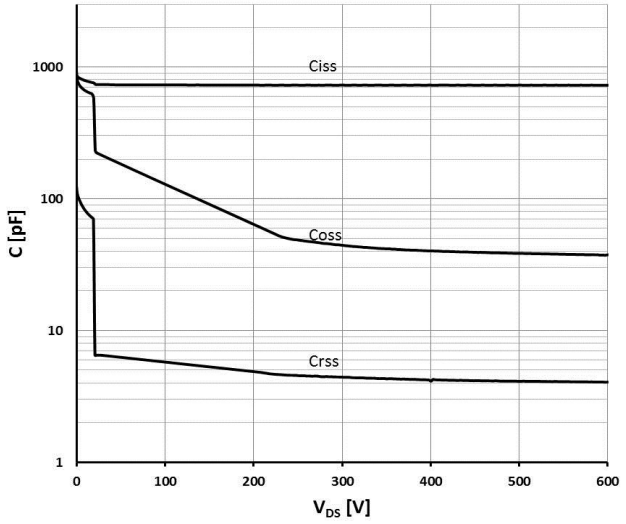


Fig. 5. Typical Capacitance
V_{GS}=0 V, f=1 MHz

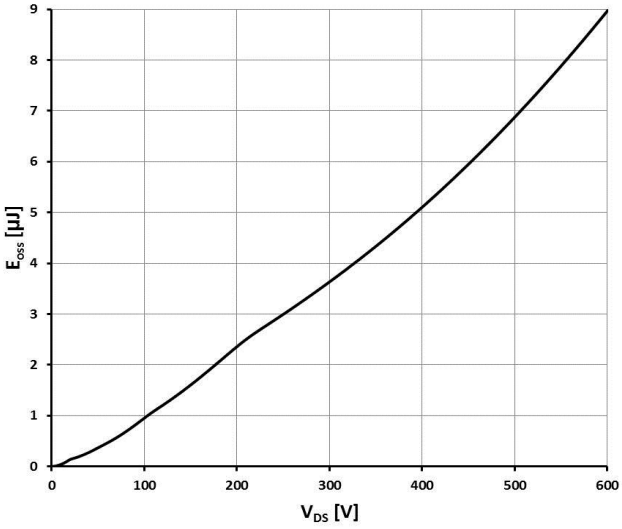


Fig. 6. Typical C_{OSS} Stored Energy

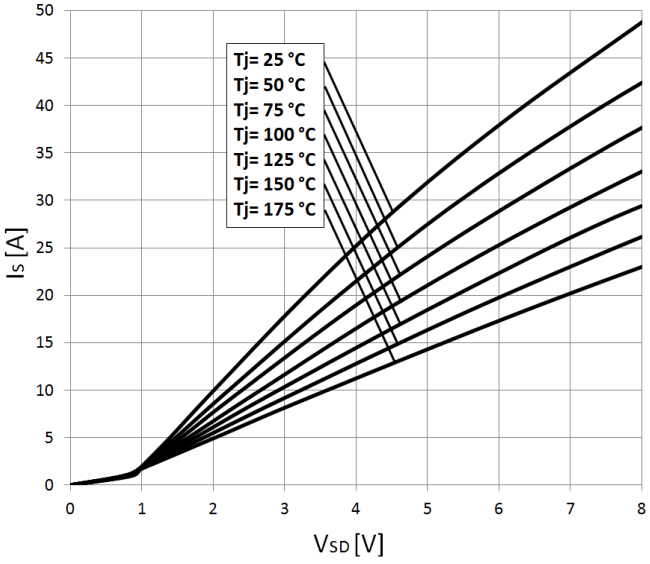


Fig. 7. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}); parameter Tj

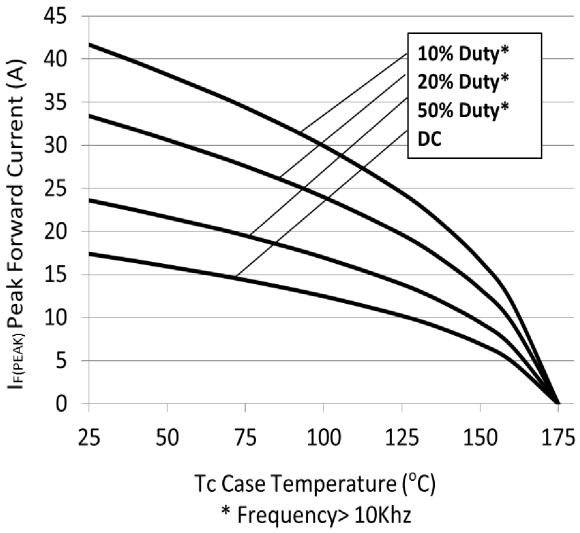


Fig. 8. Current Derating

Typical Characteristic Curves 25 °C unless otherwise noted

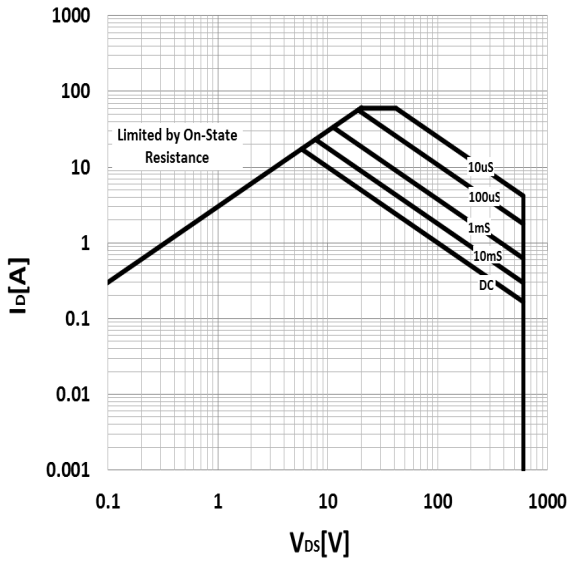


Fig. 9. Safe Operating Area T_C = 25 °C

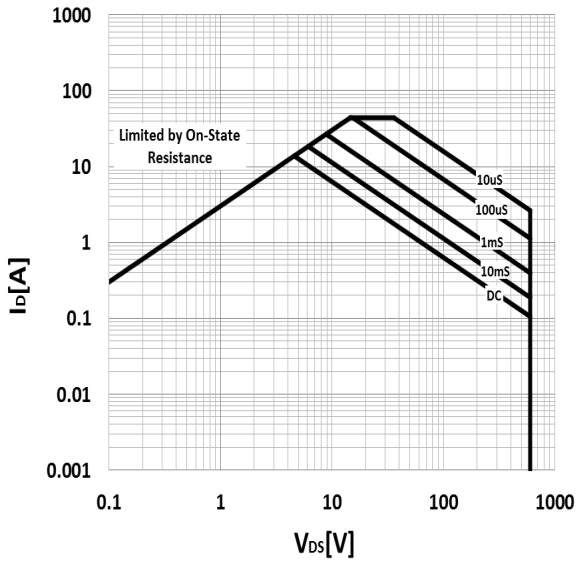


Fig. 10. Safe Operating Area T_C = 80 °C

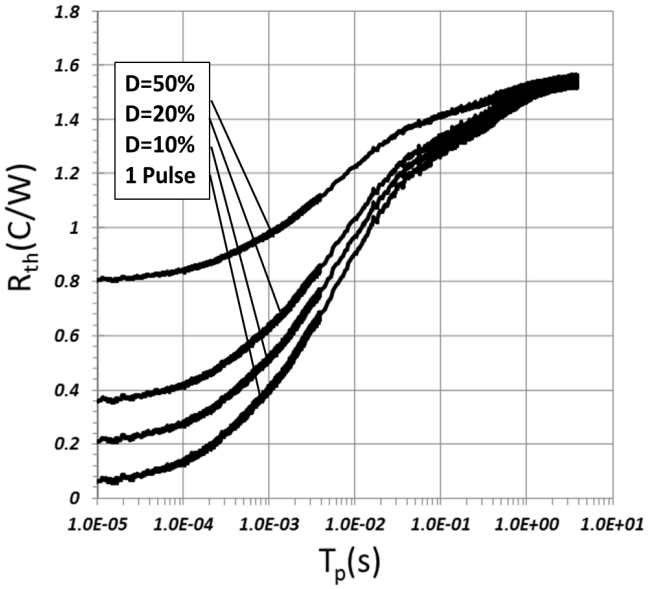


Fig. 11. Transient Thermal Resistance

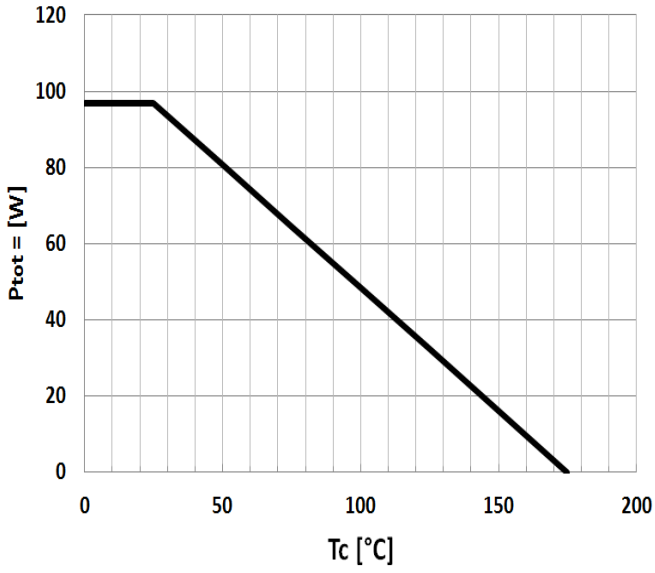


Fig. 12. Power Dissipation

Test Circuits and Waveforms

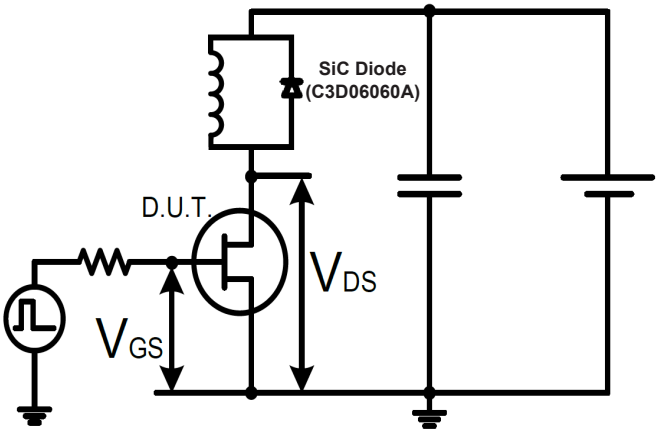


Fig. 13. Switching Time Test Circuit

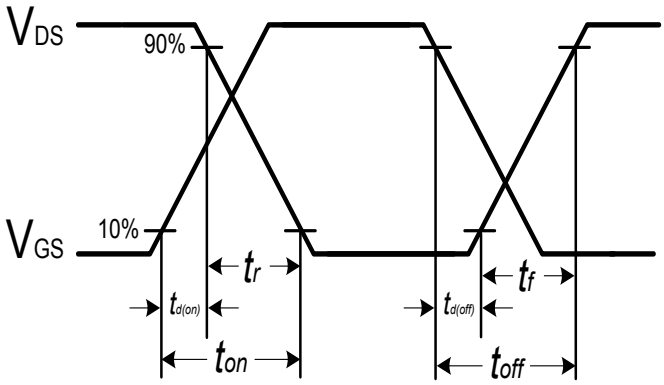


Fig. 14. Switching Time Waveform

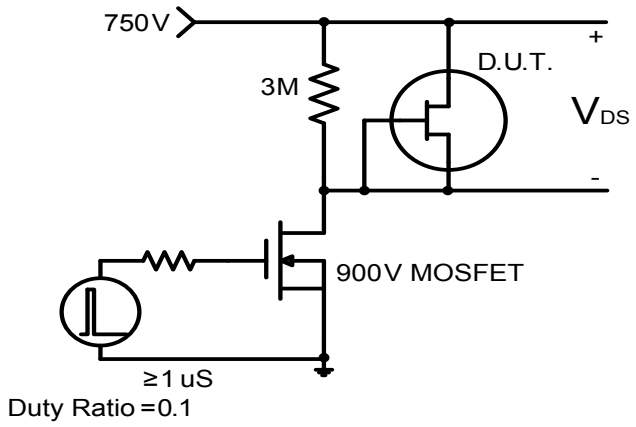


Fig. 15. Spike Voltage Test Circuit

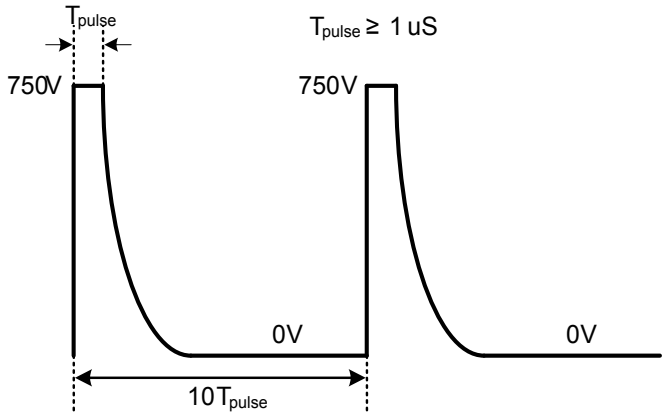


Fig. 16. Spike Voltage Waveform

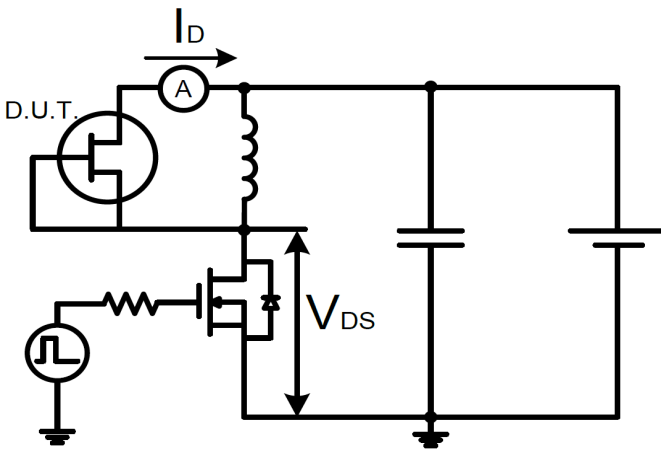


Fig. 17. Test Circuit for Reverse Diode Characteristics

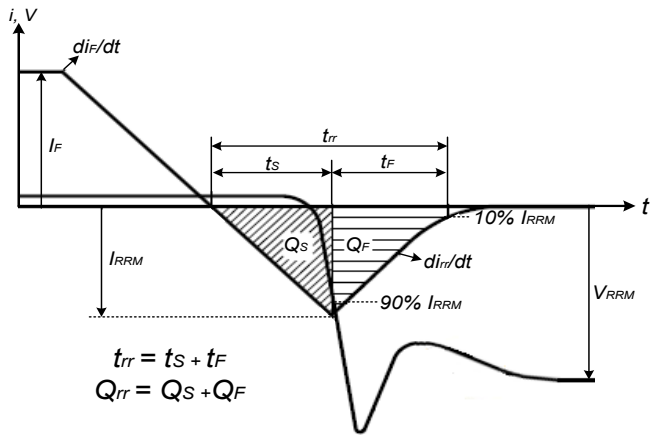
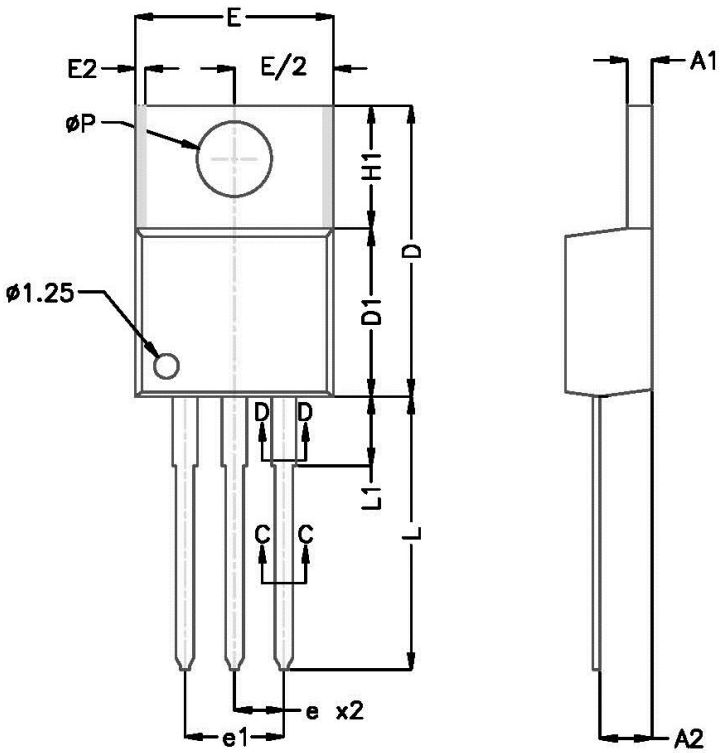


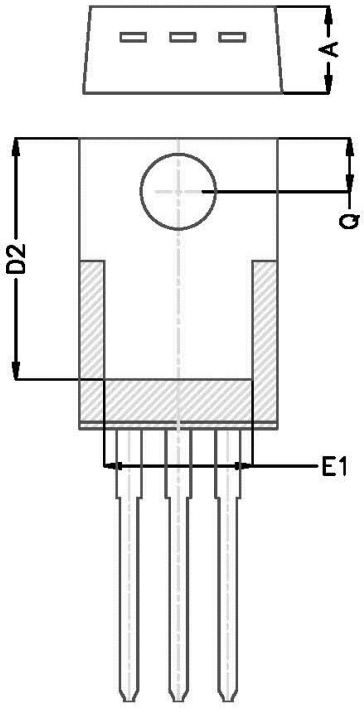
Fig. 18. Diode Recovery Waveform

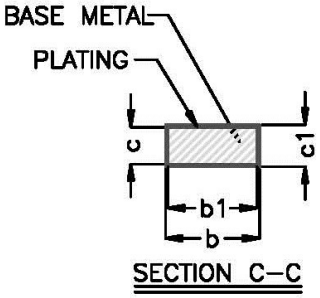
MECHANICAL

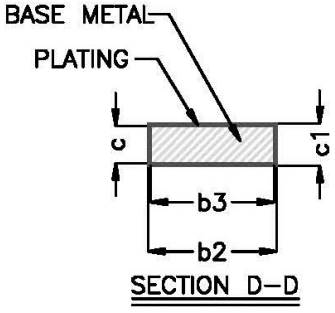
TO-220 Package



SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	–	2.92	0.080	–	0.115
b	0.38	–	1.01	0.015	–	0.040
b1	0.38	–	0.97	0.015	–	0.038
b2	1.14	–	1.78	0.045	–	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.38	–	0.61	0.014	–	0.024
c1	0.38	0.38	0.56	0.014	0.015	0.022
D	14.22	–	16.51	0.560	–	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	–	12.88	0.460	–	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	–	8.89	0.270	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.86	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	–	–	6.35	–	–	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	–	3.42	0.100	–	0.135







NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO–220AB.

TO-220 Package

Pin 1: Gate, Pin 2: Source, Pin 3: Drain, Tab: Drain

Important Notice

Transphorm Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques .

Transphorm suggests visiting application note “Printed Circuit Board Layout and Probing for GaN Power Switches” before evaluating Transphorm GaN switches. Below are some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Switches	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing. Attach the probe and its ground connection directly to the test points	Use differential mode probe, or probe ground clip with long wire