

### PRODUCT SUMMARY (TYPICAL)

$V_{DS}$ (V)	600
$R_{DS(on)}$ ( $\Omega$ )	0.15
$Q_{rr}$ (nC)	54

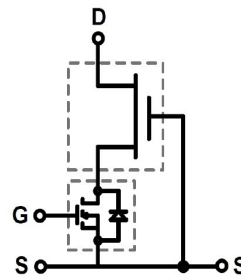
### GaN Power Low-loss Switch

#### Features

- Low  $Q_{rr}$
- Free-wheeling diode not required
- Low-side Quiet Tab™ for reduced EMI
- GSD pin layout improves high speed design
- RoHS compliant
- High frequency operation

#### Applications

- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies



TO-220 Package

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Limit Value	Unit
$I_{D25^\circ\text{C}}$	Continuous Drain Current @ $T_C=25^\circ\text{C}$	17	A
$I_{D100^\circ\text{C}}$	Continuous Drain Current @ $T_C=100^\circ\text{C}$	12	A
$I_{DM}$	Pulsed Drain Current (pulse width: 100 $\mu\text{s}$ )	60	A
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{TDS}$	Transient Drain to Source Voltage <sup>a</sup>	750	V
$V_{GSS}$	Gate to Source Voltage	$\pm 18$	V
$P_{D25^\circ\text{C}}$	Maximum Power Dissipation	96	W
$T_C$	Operating Temperature	Case	-55 to 150
		Junction	-55 to 175
$T_J$	Junction	-55 to 175	$^\circ\text{C}$
$T_S$	Storage Temperature	-55 to 150	$^\circ\text{C}$
$T_{Csold}$	Soldering peak Temperature <sup>b</sup>	260	$^\circ\text{C}$

### Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-Case	1.55	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	62	$^\circ\text{C/W}$

#### Notes

a: For 1 usec, duty cycle  $D=0.1$

b: For 10 sec, 1.6mm from the case

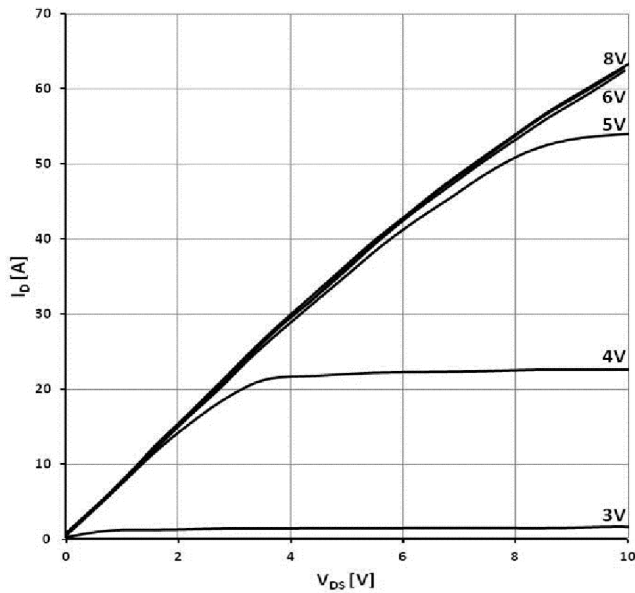
Electrical Characteristics (T <sub>C</sub> =25 °C unless otherwise stated)						
Symbol	Parameter	Min	Typical	Max	Unit	Test Conditions
<b>Static</b>						
V <sub>DSS-MAX</sub>	Maximum Drain-Source Voltage	600	-	-	V	V <sub>GS</sub> =0 V
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.8	2.35	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =1 mA
R <sub>DS(on)</sub>	Drain-Source On-Resistance (T <sub>J</sub> = 25 °C)	-	0.15	0.18	Ω	V <sub>GS</sub> =8V, I <sub>D</sub> =11A, T <sub>J</sub> = 25 °C
R <sub>DS(on)</sub>	Drain-Source On-Resistance (T <sub>J</sub> = 175 °C)	-	0.33	-	Ω	V <sub>GS</sub> =8V, I <sub>D</sub> =11A, T <sub>J</sub> = 175 °C
I <sub>DSS</sub>	Drain-to-Source Leakage Current, T <sub>J</sub> = 25 °C	-	2.5	90	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> = 25 °C
I <sub>DSS</sub>	Drain-to-Source Leakage Current, T <sub>J</sub> = 150 °C	-	10	-	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> = 150 °C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage Current	-	-	100	nA	V <sub>GS</sub> = 18 V
	Gate-to-Source Reverse Leakage Current	-	-	-100		V <sub>GS</sub> = -18 V
<b>Dynamic</b>						
C <sub>ISS</sub>	Input Capacitance	-	740	-	pF	V <sub>GS</sub> =0 V, V <sub>DS</sub> =100 V, f =1 MHz
C <sub>OSS</sub>	Output Capacitance	-	133	-		
C <sub>RSS</sub>	Reverse Transfer Capacitance	-	3.6	-		
C <sub>O(er)</sub>	Output Capacitance, energy related <sup>a</sup>	-	56	-	pF	V <sub>GS</sub> =0 V, V <sub>DS</sub> =0 V to 480 V
C <sub>O(tr)</sub>	Output Capacitance, time related <sup>a</sup>	-	110	-		
Q <sub>g</sub>	Total Gate Charge <sup>b</sup>	-	6.2	9.3	nC	V <sub>DS</sub> =100 V <sup>a</sup> , V <sub>GS</sub> = 0-4.5 V, I <sub>D</sub> = 11 A
Q <sub>gs</sub>	Gate-Source Charge	-	2.1	-		
Q <sub>gd</sub>	Gate-Drain Charge	-	2.2	-		
t <sub>d(on)</sub>	Turn-On Delay	-	4	-	ns	V <sub>DS</sub> =480 V, V <sub>GS</sub> = 0-10 V, I <sub>D</sub> = 11 A, R <sub>G</sub> = 2 Ω
t <sub>r</sub>	Rise Time	-	3	-		
T <sub>d(off)</sub>	Turn-Off Delay	-	10.5	-		
t <sub>f</sub>	Fall Time	-	3.5	-		
<b>Reverse operation</b>						
I <sub>S</sub>	Reverse Current	-	-	11	A	V <sub>GS</sub> =0 V, T <sub>J</sub> =100 °C
V <sub>SD</sub>	Reverse Voltage	-	2.3	2.8	V	V <sub>GS</sub> =0 V, I <sub>S</sub> =11 A, T <sub>J</sub> =25 °C
V <sub>SD</sub>	Reverse Voltage	-	1.6	1.9	V	V <sub>GS</sub> =0 V, I <sub>S</sub> =5.5 A, T <sub>J</sub> =25 °C
t <sub>rr</sub>	Reverse Recovery Time	-	30	-	ns	I <sub>S</sub> =11 A, V <sub>DD</sub> =480 V, di/dt =450 A/μs, T <sub>J</sub> =25 °C
Q <sub>rr</sub>	Reverse Recovery Charge	-	54	-	nC	

**Notes**

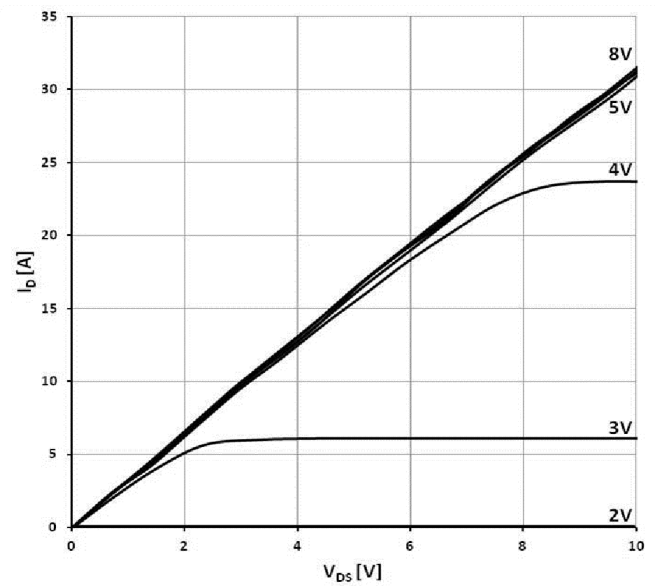
 a: Fixed while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>;

 b: Q<sub>g</sub> does not change for V<sub>DS</sub>>100 V.

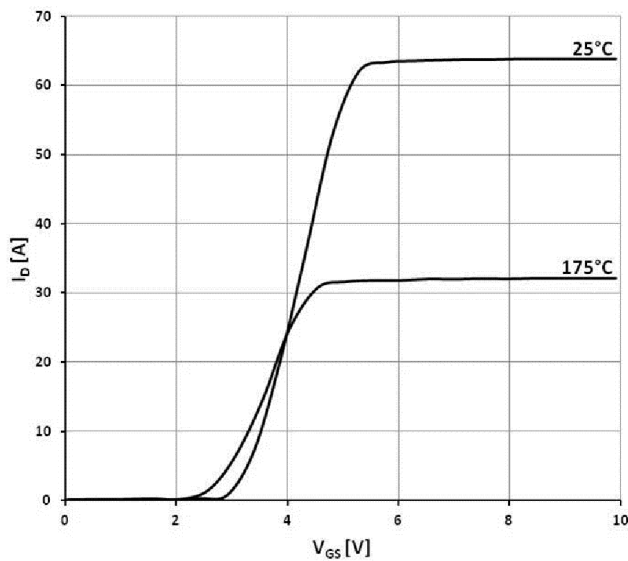
### Typical Characteristic Curves 25 °C unless otherwise noted



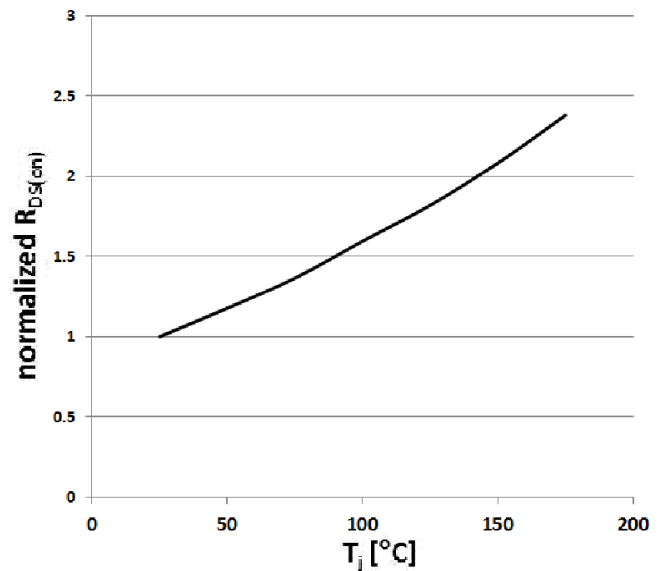
**Fig. 1. Typical Output Characteristics  $T_J = 25\text{ °C}$**   
Parameter:  $V_{GS}$



**Fig. 2. Typical Output Characteristics  $T_J = 175\text{ °C}$**   
Parameter:  $V_{GS}$

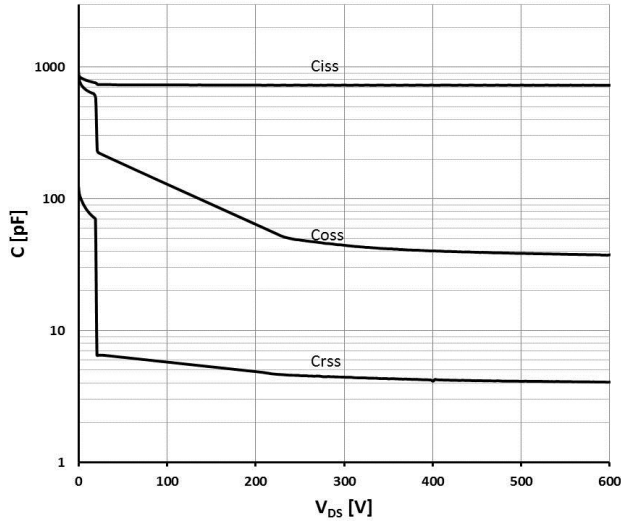


**Fig. 3. Typical Transfer Characteristics**  
 $V_{DS} = 10\text{ V}$ , Parameter:  $T_J$

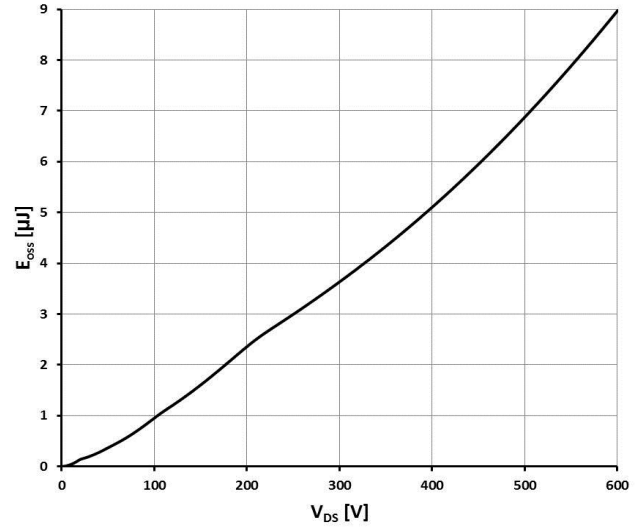


**Fig. 4. Normalized On-Resistance**  
 $I_D = 12\text{ A}$ ,  $V_{GS} = 8\text{ V}$

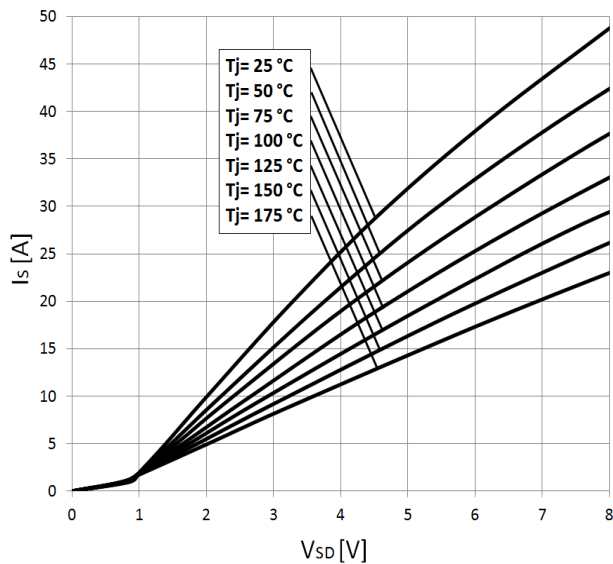
## Typical Characteristic Curves 25 °C unless otherwise noted



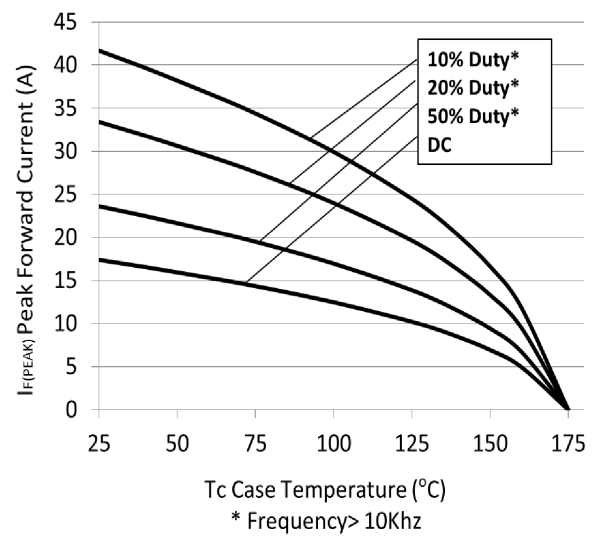
**Fig. 5. Typical Capacitance**  
V<sub>GS</sub>=0 V, f=1 MHz



**Fig. 6. Typical C<sub>oss</sub> Stored Energy**



**Fig. 7. Forward Characteristics of Rev. Diode**  
I<sub>S</sub>=f(V<sub>SD</sub>); parameter T<sub>j</sub>



**Fig. 8. Current Derating**  
\* Frequency > 10Khz

## Typical Characteristic Curves 25 °C unless otherwise noted

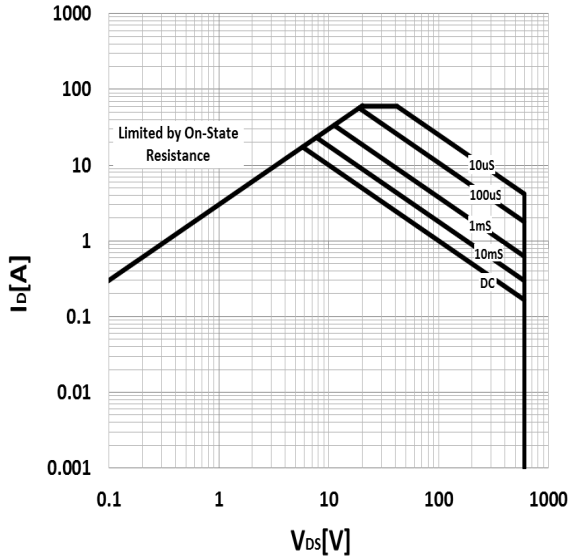


Fig. 9. Safe Operating Area  $T_c = 25\text{ }^\circ\text{C}$

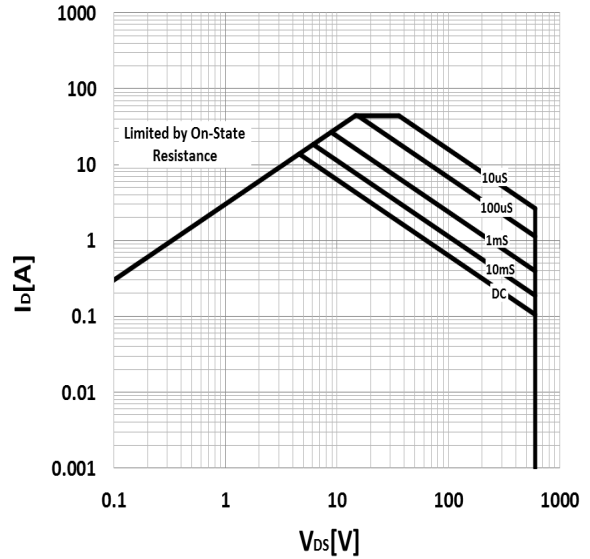


Fig. 10. Safe Operating Area  $T_c = 80\text{ }^\circ\text{C}$

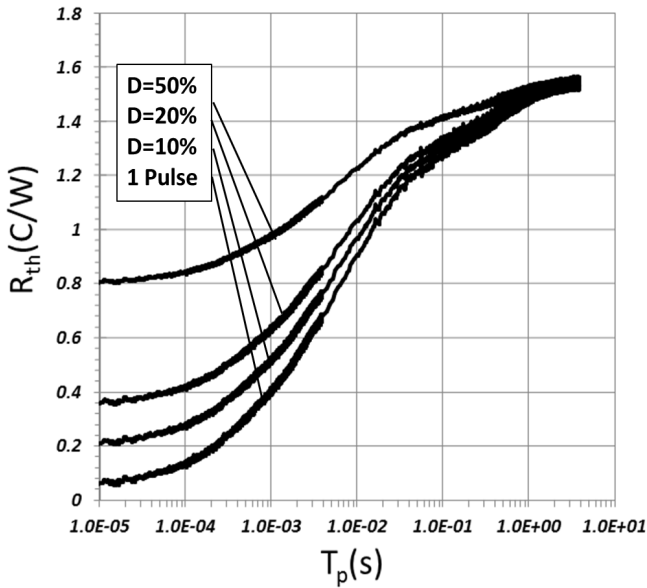


Fig. 11. Transient Thermal Resistance

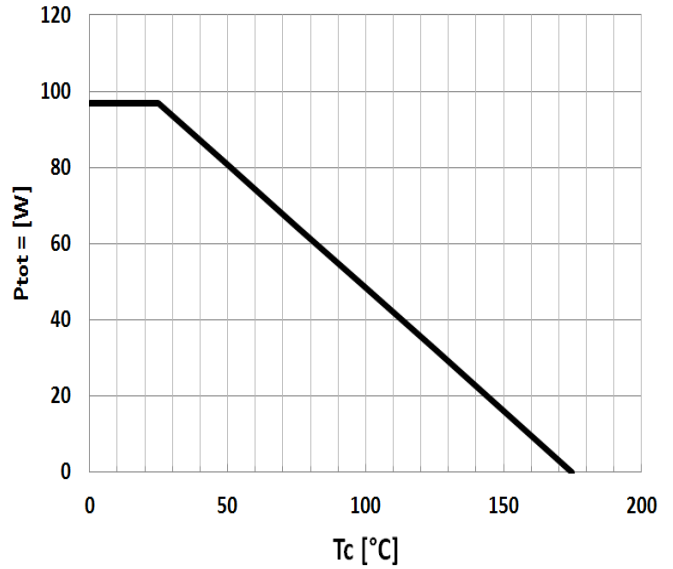


Fig. 12. Power Dissipation

## Test Circuits and Waveforms

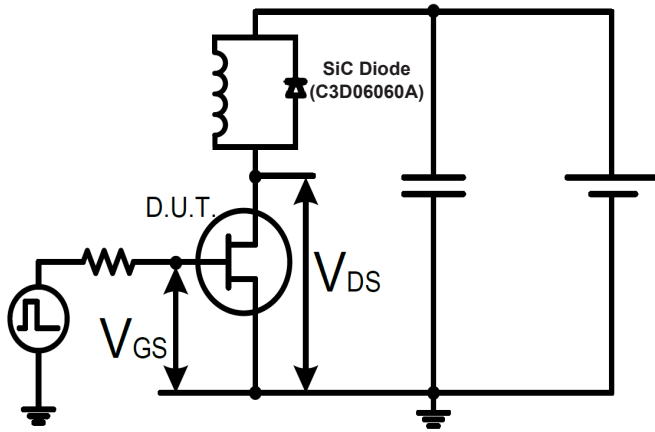


Fig. 13. Switching Time Test Circuit

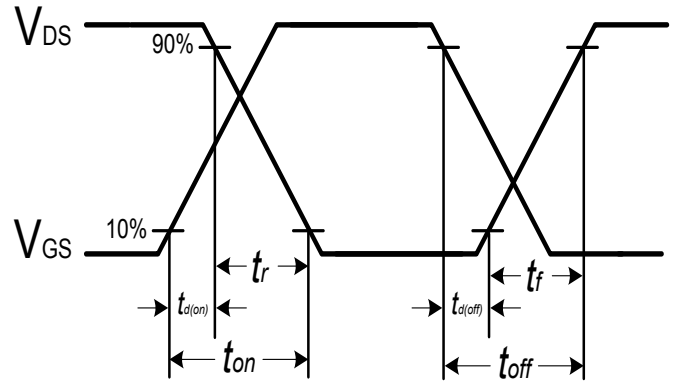


Fig. 14. Switching Time Waveform

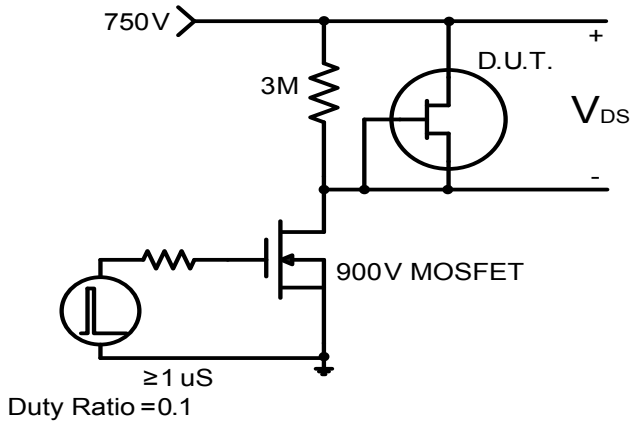


Fig. 15. Spike Voltage Test Circuit

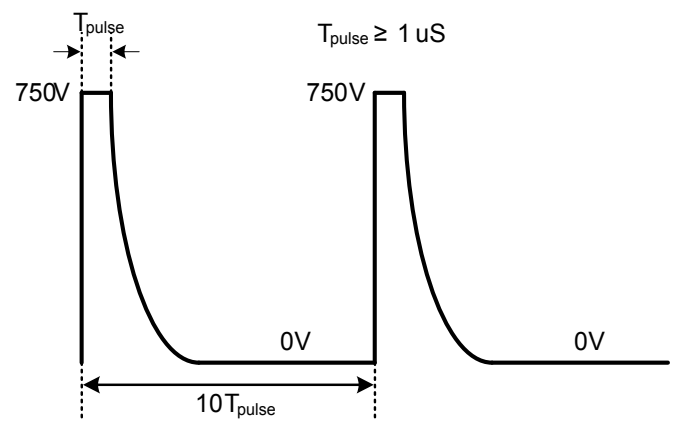


Fig. 16. Spike Voltage Waveform

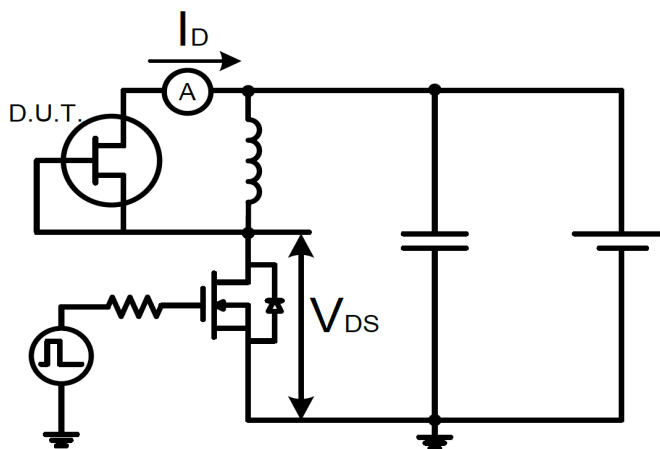


Fig. 17. Test Circuit for Reverse Diode Characteristics

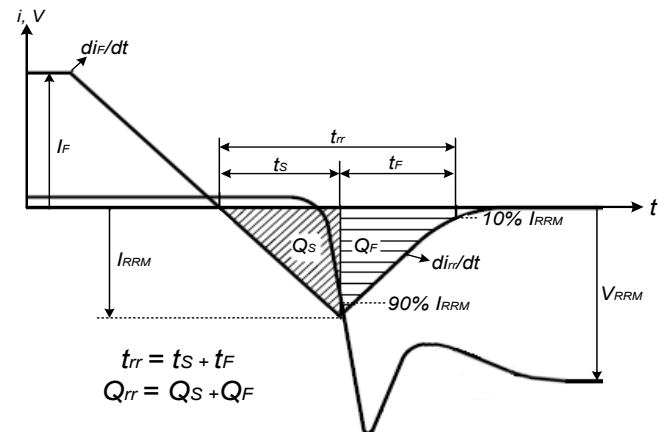
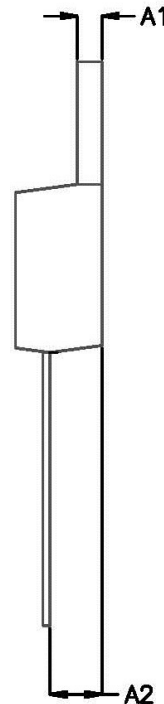
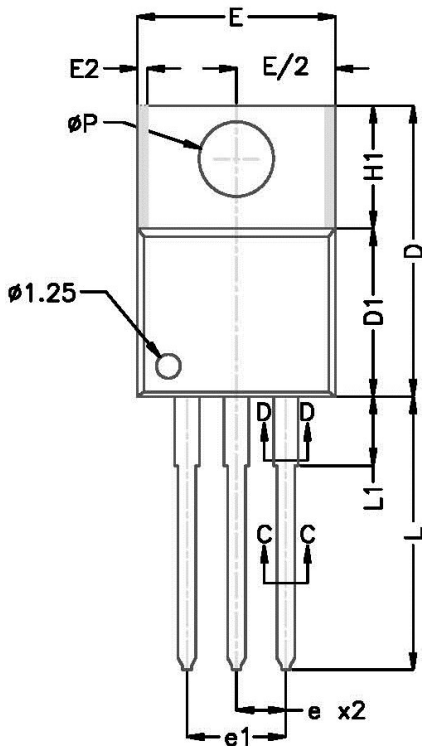


Fig. 18. Diode Recovery Waveform

## MECHANICAL

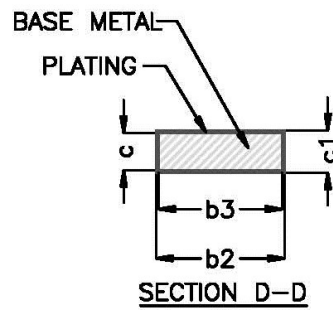
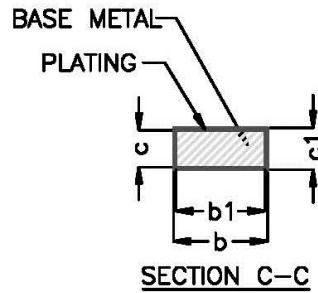
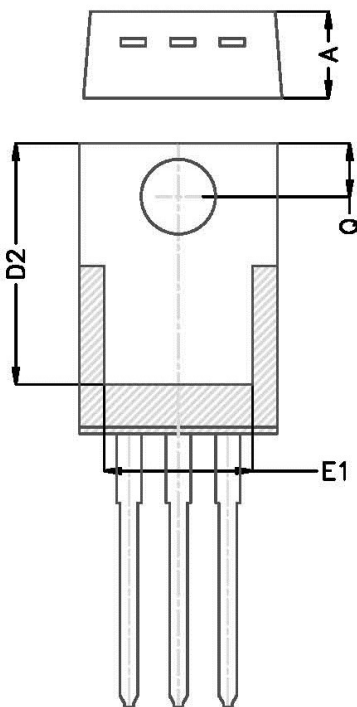
## TO-220 Package



SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.58	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	-	2.92	0.080	-	0.115
b	0.38	-	1.01	0.015	-	0.040
b1	0.38	-	0.97	0.015	-	0.038
b2	1.14	-	1.78	0.045	-	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.38	-	0.61	0.014	-	0.024
c1	0.38	0.38	0.58	0.014	0.015	0.022
D	14.22	-	18.51	0.560	-	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	-	12.88	0.460	-	0.507
E	8.85	10.19	10.67	0.380	0.401	0.420
E1	6.88	-	8.89	0.270	-	0.350
E2	-	-	0.76	-	-	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.88	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	-	-	6.35	-	-	0.250
ØP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	-	3.42	0.100	-	0.135

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO-220AB.



TO-220 Package

Pin 1: Gate, Pin 2: Source, Pin 3: Drain, Tab: Source

## Important Notice

Transphorm Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques .

Transphorm suggests visiting application note “Printed Circuit Board Layout and Probing for GaN Power Switches” before evaluating Transphorm GaN switches. Below are some practical rules that should be followed during the evaluation.

<b>When Evaluating Transphorm GaN Switches</b>	
<b>DO</b>	<b>DO NOT</b>
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing. Attach the probe and its ground connection directly to the test points	Use differential mode probe, or probe ground clip with long wire