transphorm

TPH3205WS

600V Cascode GaN FET in TO-247 (source tab)

Not recommended for new designs—see TP65H050WS

Description

The TPH3205WS 600V, 52mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Ordering Information

Part Number	Package	Package Configuration
TPH3205WS	3 Lead TO-247	Common Source

Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 136nC—no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

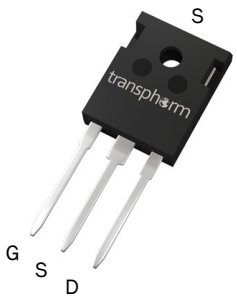
Benefits

- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

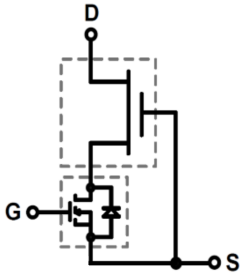
- Renewable energy
- Industrial
- Telecom and datacom
- Servo motors

TPH3205WS
TO-247
(top view)



Key Specifications	
V_{DS} (V) min	600
V_{TDS} (V) max	750
$R_{DS(on)}$ (mΩ) max*	63
Q_{rr} (nC) typ	136
Qg (nC) typ	28

* Dynamic $R_{(on)}$



Cascode Device Structure

Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25°C [a]		36	A
$I_{D100°C}$	Continuous drain current @T_C=100°C [a]		25	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		150	A
V_{DSS}	Drain to source voltage		600	V
V_{TDS}	Transient drain to source voltage [b]		750	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25°C}$	Maximum power dissipation		150	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +175	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [c]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	°C/W

Notes:
a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.1, spike duration <1µs
c. For 10 sec., 1.6mm from the case

Electrical Parameters (T_C=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS-MAX}$	Maximum drain-source voltage	600	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage [d]	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.7mA
$R_{DS(on)}$	Drain-source on-resistance (T_J=25°C) [a]	—	52	63	mΩ	V_{GS}=8V, I_D=24A, T_J=25°C
	Drain-source on-resistance (T_J=175°C) [a]	—	120	—		V_{GS}=8V, I_D=24A, T_J=175°C
I_{DSS}	Drain-to-source leakage current (T_J=25°C)	—	4	40	μA	V_{DS}=600V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current (T_J=150°C)	—	15	—		V_{DS}=600V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
C_{ISS}	Input capacitance	—	2200	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	115	—		
C_{RSS}	Reverse transfer capacitance	—	19	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	175	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	285	—		
Q_g	Total gate charge	—	28	42	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=24A
Q_{gs}	Gate-source charge	—	10	—		
Q_{gd}	Gate-drain charge	—	6	—		
$t_{d(on)}$	Turn-on delay	—	22	—	ns	V_{DS}=480V, V_{GS}=0V to 10V, I_D=24A, R_G=2Ω
t_r	Rise time	—	7.5	—		
$T_{d(off)}$	Turn-off delay	—	33	—		
t_f	Fall time	—	4.5	—		
Reverse Device Characteristics						
I_S	Reverse current	—	—	25	A	V_{GS}=0V, T_C=100°C ≤50% Duty Cycle
V_{SD}	Reverse voltage [a]	—	2.2	2.6	V	V_{GS}=0V, I_S=24A, T_J=25°C
		—	1.6	1.9		V_{GS}=0V, I_S=12A, T_J=25°C
t_{rr}	Reverse recovery time	—	30	—	ns	I_S=24A, V_{DD}=400V, di/dt=1000A/μs, T_J=25°C
Q_{rr}	Reverse recovery charge	—	136	—	nC	

Notes:
a. Dynamic value
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V
d. Recommended gate drive: Turn on +8V, turn off 0 or -5V. For half bridge, use isolated driver ICs with 5V UVLO.

Typical Characteristics (25 °C unless otherwise stated)

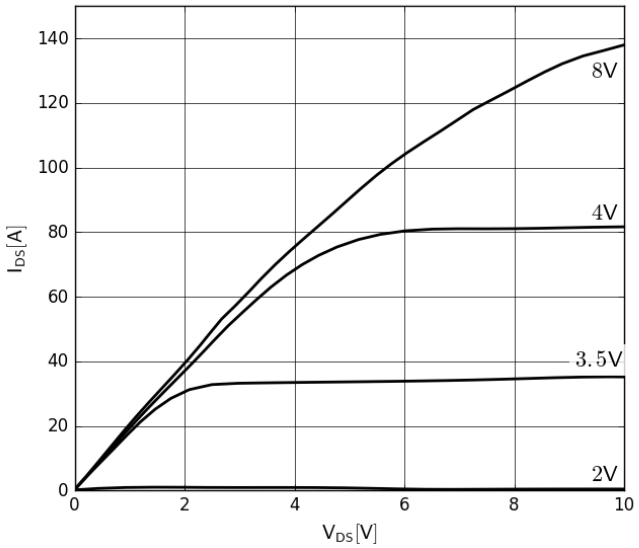


Figure 1. Typical Output Characteristics T_J=25 °C
Parameter: V_{GS}

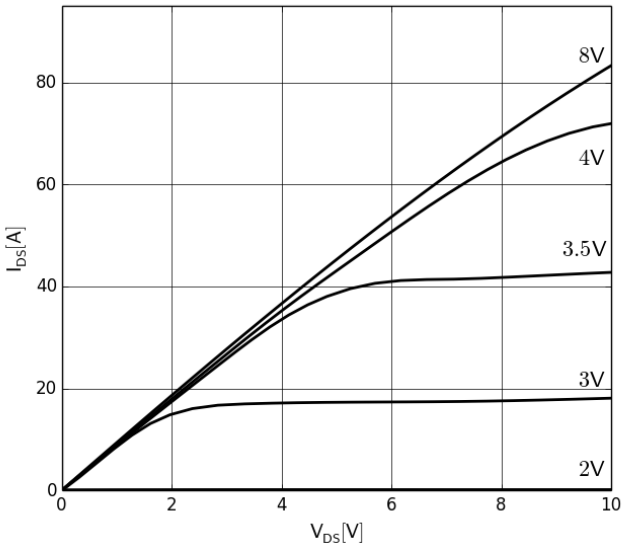


Figure 2. Typical Output Characteristics T_J=175 °C
Parameter: V_{GS}

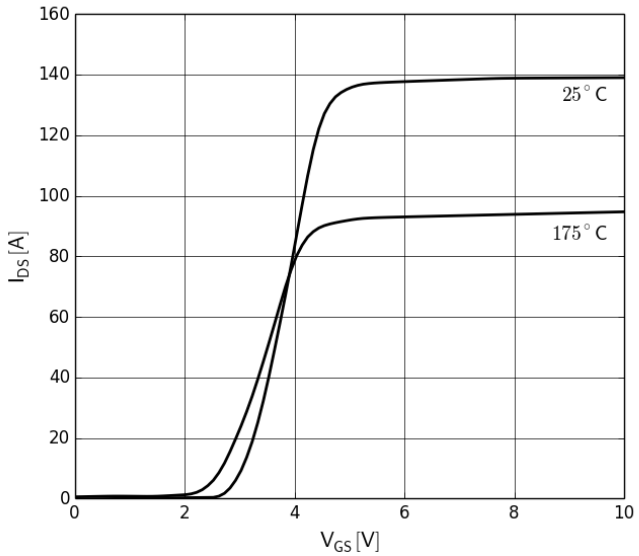


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

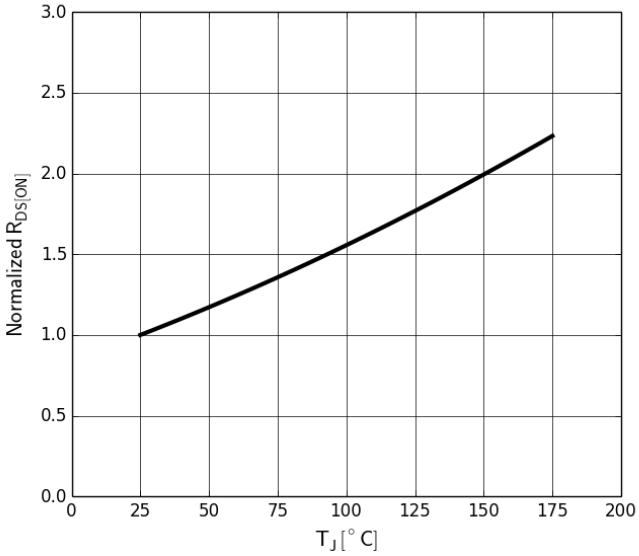


Figure 4. Normalized On-Resistance
I_D=12A, V_{GS}=8V

Typical Characteristics (25 °C unless otherwise stated)

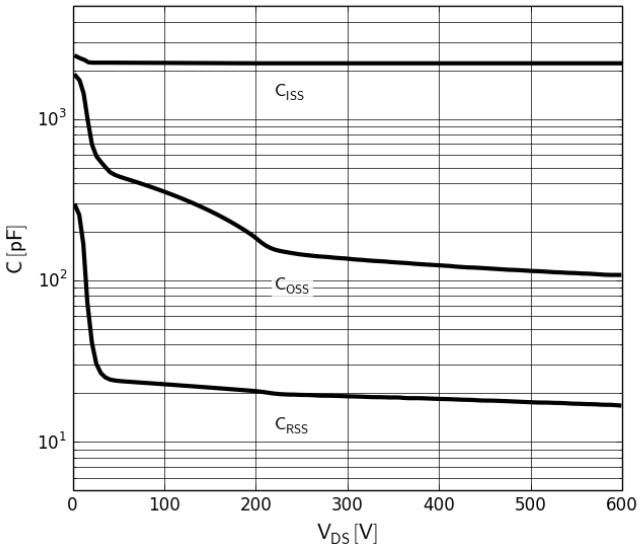


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

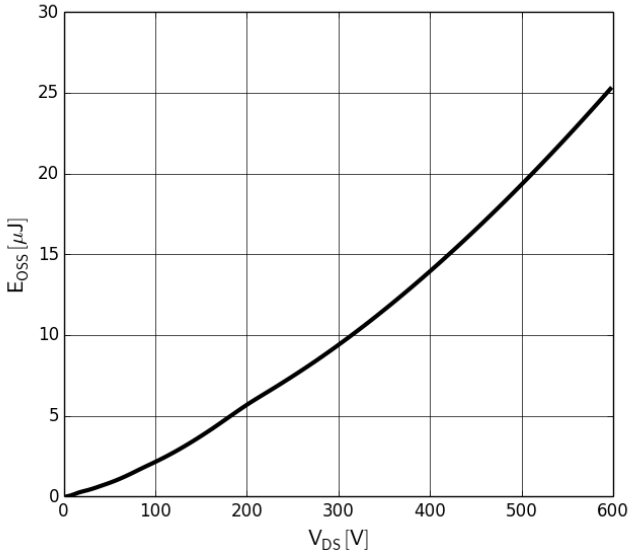


Figure 6. Typical C_{oss} Stored Energy

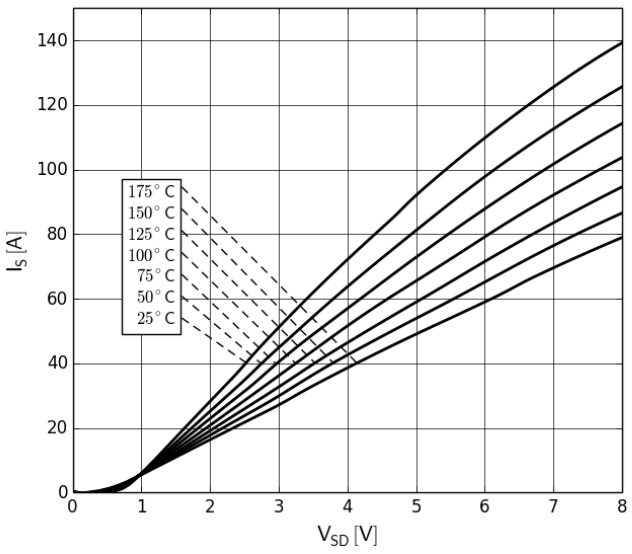


Figure 7. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$, parameter: T_J

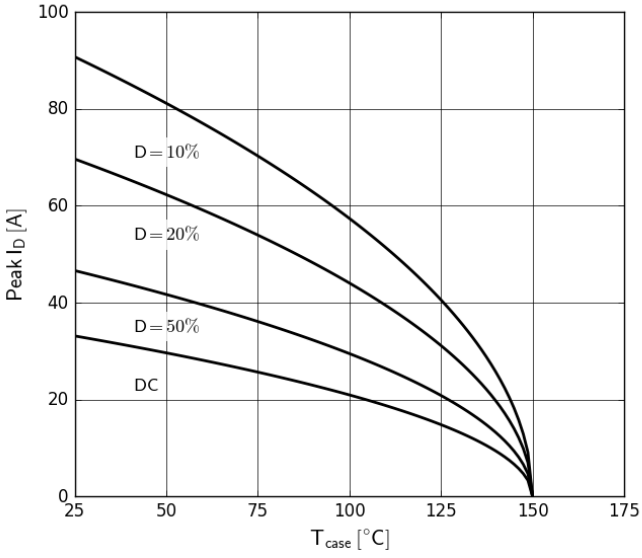


Figure 8. Current Derating
Pulse width = 10µs

Typical Characteristics (25 °C unless otherwise stated)

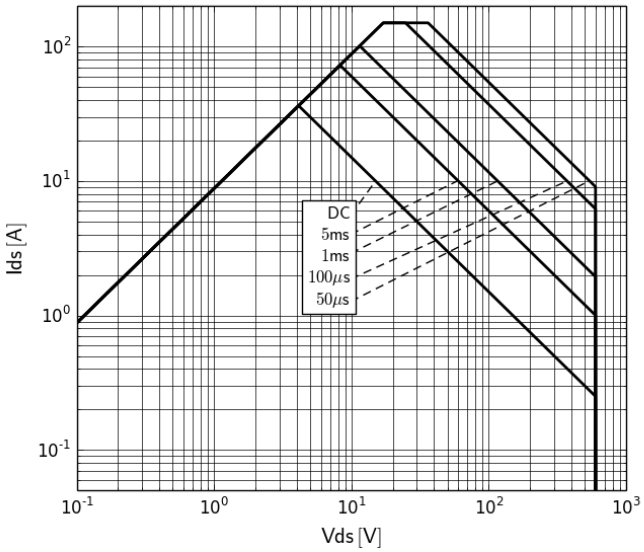


Figure 9. Safe Operating Area T_C=25 °C (calculated based based on thermal limit)

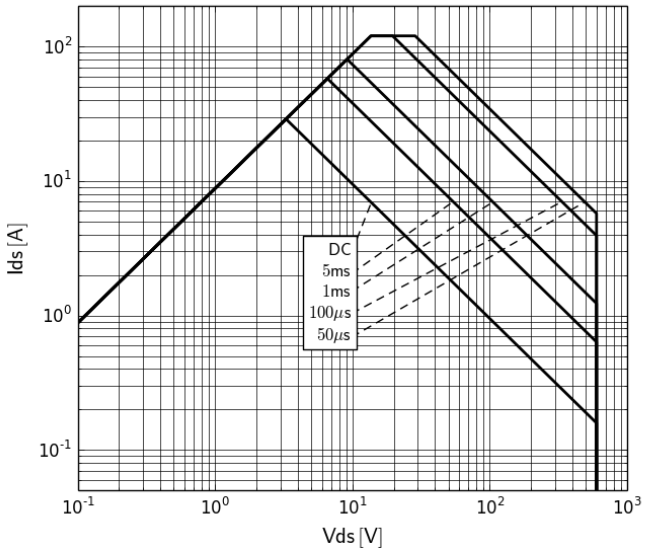


Figure 10. Safe Operating Area T_C=80 °C (calculated based on thermal limit)

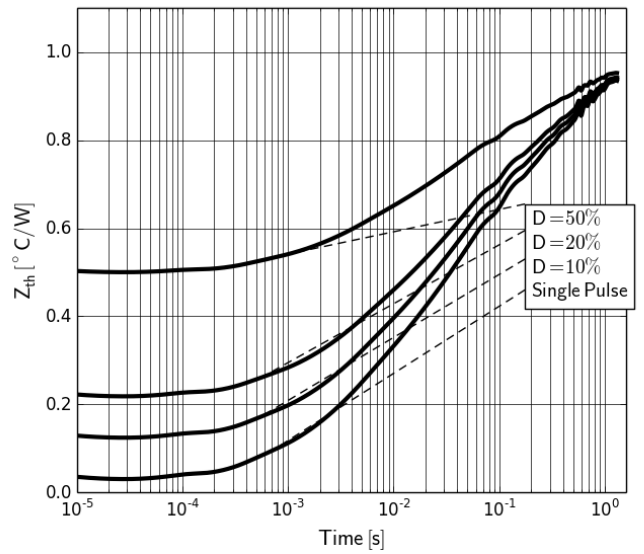


Figure 11. Transient Thermal Resistance

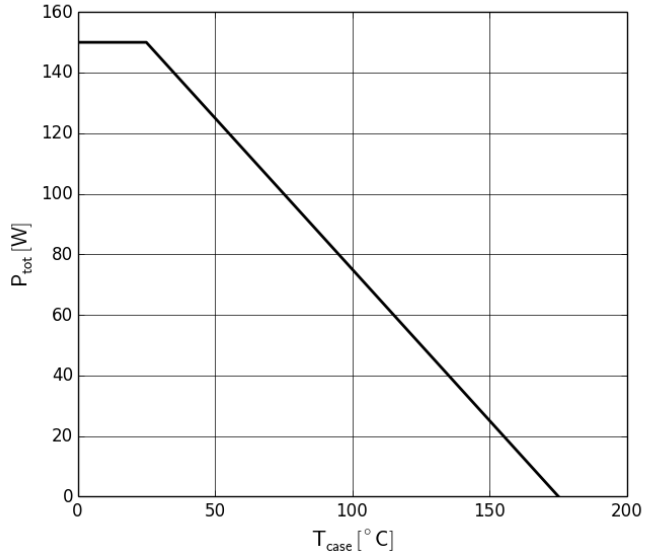


Figure 12. Power Dissipation

Test Circuits and Waveforms

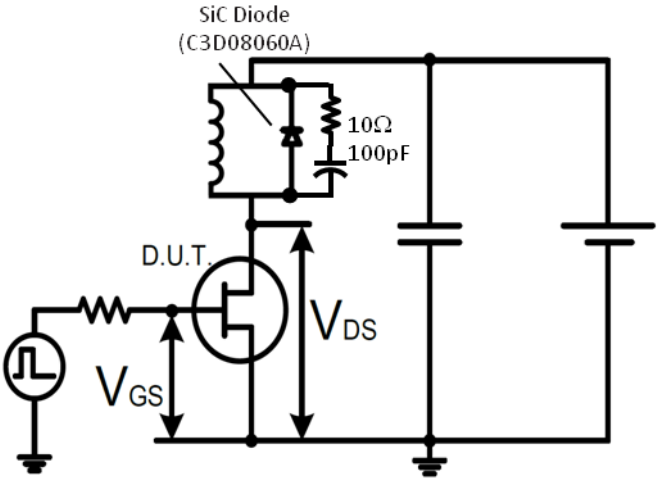


Figure 13. Switching Time Test Circuit
***See app note AN0009 for methods to ensure clean switching**

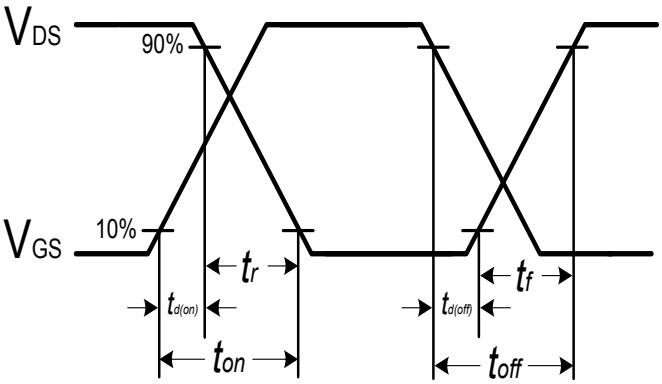


Figure 14. Switching Time Waveform

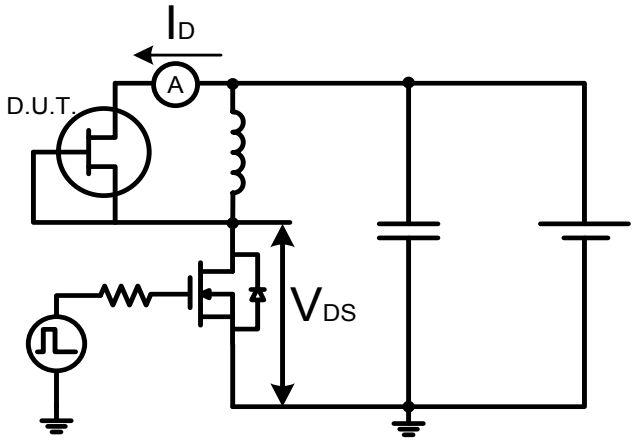


Figure 15. Test Circuit for Diode Characteristics

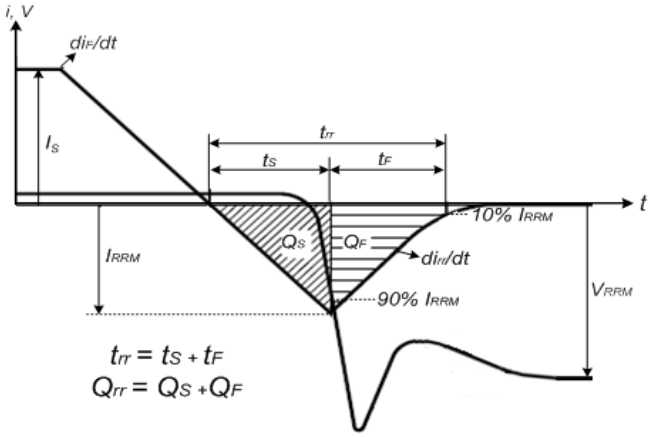


Figure 16. Diode Recovery Waveform

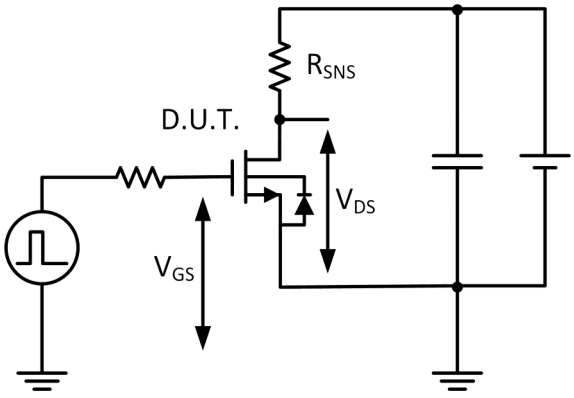


Figure 17. Test Circuit for Dynamic $R_{DS(on)}$

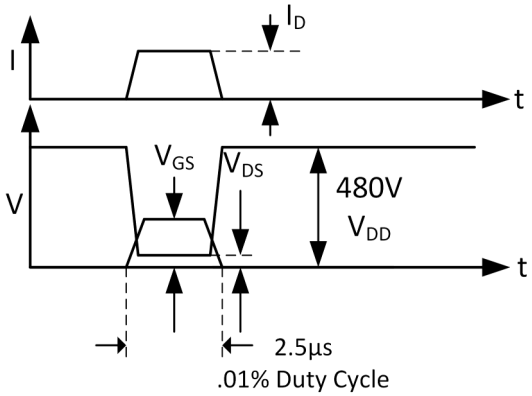
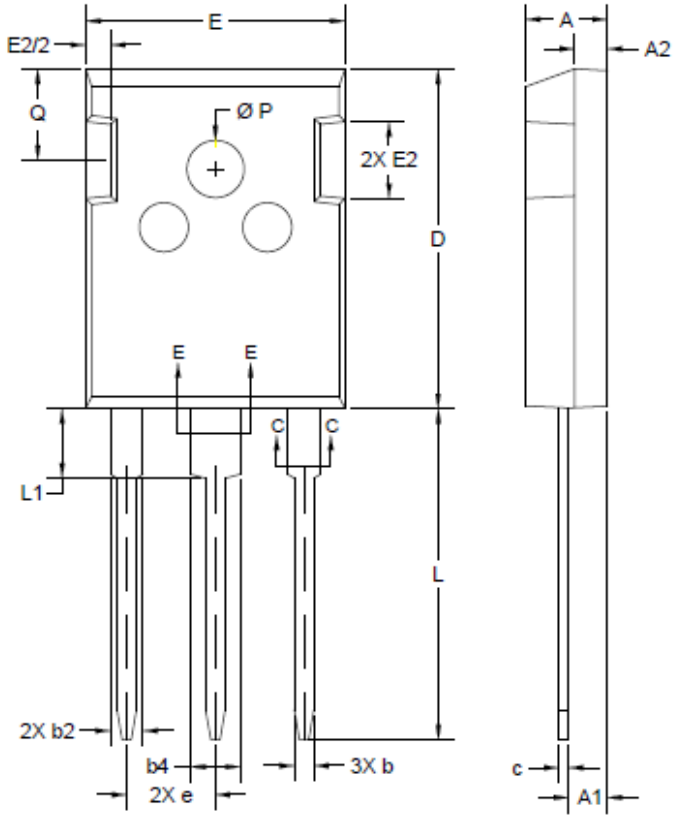


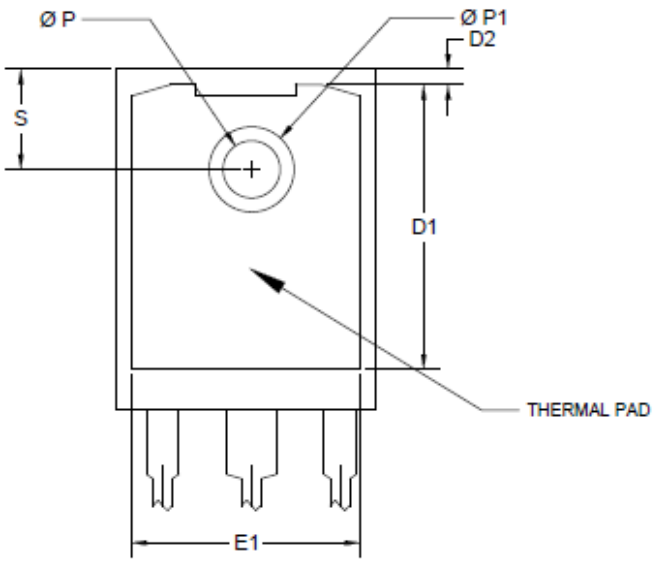
Figure 18. Dynamic $R_{DS(on)}$ Waveform

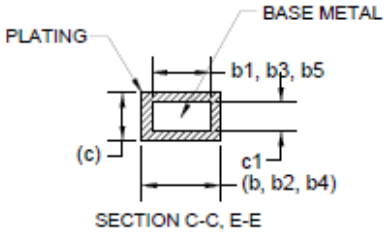
Mechanical

3 Lead TO-247 Package



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.82	5.00	5.19	0.190	0.197	0.204
A1	2.20	2.39	2.57	0.087	0.094	0.101
A2	1.82	2.01	2.18	0.072	0.079	0.086
b	1.09	1.19	1.35	0.043	0.047	0.053
b1	1.09	-	1.30	0.043	-	0.051
b2	1.87	2.03	2.31	0.074	0.080	0.091
b3	1.87	-	2.27	0.074	-	0.089
b4	2.94	3.05	3.22	0.116	0.120	0.127
b5	2.94	-	3.18	0.116	-	0.125
c	0.50	0.58	0.68	0.020	0.023	0.027
c1	0.50	-	0.64	0.020	-	0.025
D	20.67	20.85	21.11	0.814	0.821	0.831
D1	17.20	-	17.63	0.677	-	0.694
D2	0.81	-	1.20	0.032	-	0.048
E	15.72	15.90	16.15	0.619	0.626	0.636
E1	13.79	-	14.25	0.543	-	0.561
E2	4.30	-	4.86	0.169	-	0.191
e	5.46 BSC			0.215 BSC		
L	19.55	19.94	20.38	0.770	0.785	0.802
L1	3.93	4.11	4.48	0.155	0.162	0.176
ØP	3.50	3.61	3.69	0.138	0.142	0.145
ØP1	7.08	7.19	7.32	0.279	0.283	0.288
Q	5.41	-	5.85	0.213	-	0.230
S	6.15 BSC			0.242 BSC		





NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

TO-247 3L			
transphorm			
SCALE: 1:1	SHEET 1/1	DRAWING NO. 200019	VER. 3

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

Evaluation Boards

- TDPS2800E2C1-KIT: 2.8kW totem-pole PFC evaluation platform
- TDPS3500E0E10-KIT: 3.5kW hard-switched half-bridge, buck, or boost evaluation platform

Revision History

Version	Date	Change(s)
17	11/14/2016	Added application note AN0009, Marked NRND—see TPH3205WSB
18	12/12/2016	Formatting Changes to p. 3, revision of dynamic measurement verbiage
19	2/15/2017	Updated evaluation boards and package drawing, added gate drive suggestion
20	7/16/2018	marked NRND—see TP65H050WS