

MOSFETs Silicon N-channel MOS (U-MOSIX-H)

# TPHR9203PL

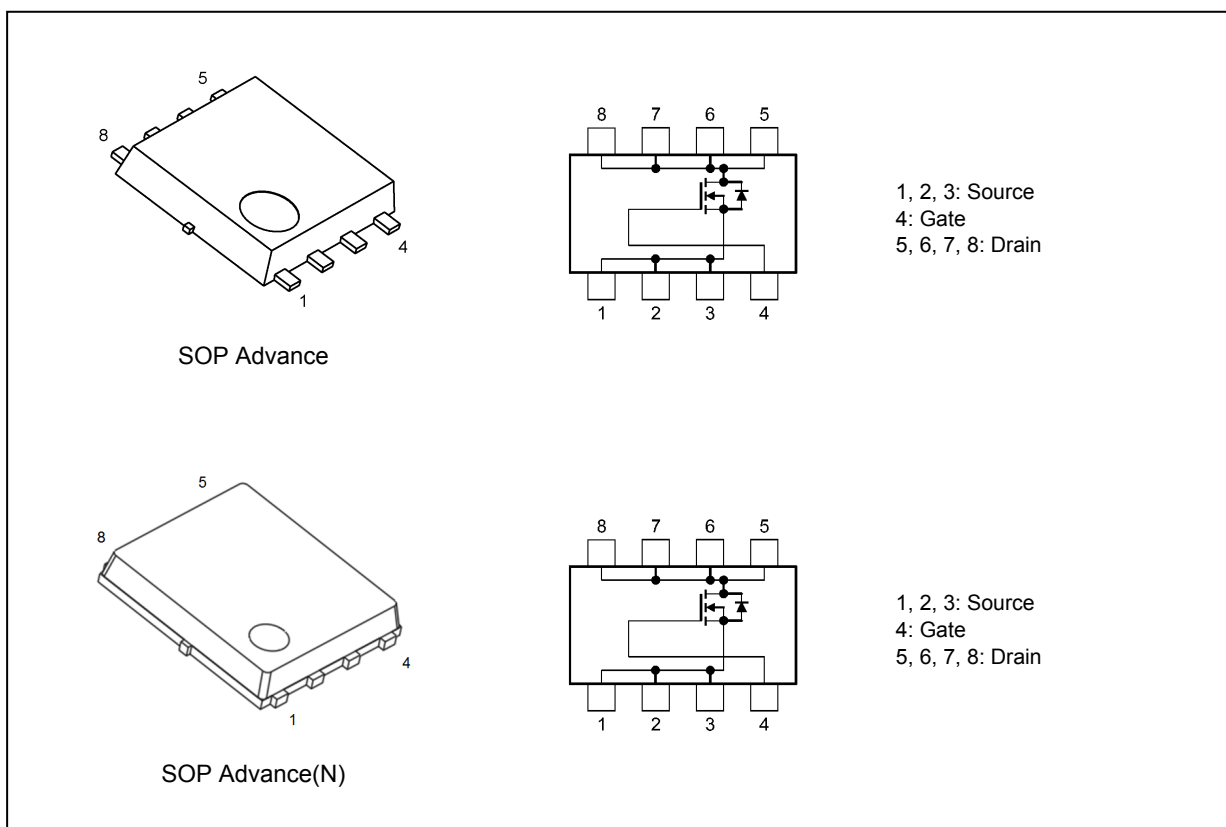
## 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

## 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 19 \text{ nC}$  (typ.)
- (3) Small output charge:  $Q_{OSS} = 51 \text{ nC}$  (typ.)
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 0.61 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (5) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 30 \text{ V}$ )
- (6) Enhancement mode:  $V_{th} = 1.1 \text{ to } 2.1 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.5 \text{ mA}$ )

## 3. Packaging and Internal Circuit



The package can be selected according to your preference. For details, please contact your TOSHIBA sales representative.

Start of commercial production

2016-06

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                                                    | Symbol    | Rating     | Unit               |
|--------------------------------------------------------------------|-----------|------------|--------------------|
| Drain-source voltage                                               | $V_{DSS}$ | 30         | V                  |
| Gate-source voltage (Note 1)                                       | $V_{GSS}$ | $\pm 20$   |                    |
| Drain current (DC) ( $T_c = 25\text{ }^{\circ}\text{C}$ ) (Note 2) | $I_D$     | 150        | A                  |
| Drain current (DC) (Silicon limit) (Note 2), (Note 3)              | $I_D$     | 280        |                    |
| Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 2)   | $I_{DP}$  | 500        |                    |
| Power dissipation ( $T_c = 25\text{ }^{\circ}\text{C}$ )           | $P_D$     | 132        | W                  |
| Power dissipation (Note 4)                                         | $P_D$     | 3.0        |                    |
| Power dissipation (Note 5)                                         | $P_D$     | 0.96       |                    |
| Single-pulse avalanche energy (Note 6)                             | $E_{AS}$  | 108        | mJ                 |
| Single-pulse avalanche current (Note 6)                            | $I_{AS}$  | 120        | A                  |
| Channel temperature                                                | $T_{ch}$  | 175        | $^{\circ}\text{C}$ |
| Storage temperature                                                | $T_{stg}$ | -55 to 175 |                    |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

## 5. Thermal Characteristics

| Characteristics                                                                       | Symbol         | Max  | Unit                 |
|---------------------------------------------------------------------------------------|----------------|------|----------------------|
| Channel-to-case thermal resistance ( $T_c = 25\text{ }^{\circ}\text{C}$ )             | $R_{th(ch-c)}$ | 1.13 | $^{\circ}\text{C/W}$ |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^{\circ}\text{C}$ ) (Note 4) | $R_{th(ch-a)}$ | 50   |                      |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^{\circ}\text{C}$ ) (Note 5) | $R_{th(ch-a)}$ | 156  |                      |

Note 1: +20 V/-16 V ensured at DC condition.

-20 V ensured at pulse condition (duty 5 %).

Note 2: Ensure that the channel temperature does not exceed 175  $^{\circ}\text{C}$ .

Note 3: Limited 150 A by package capability.

Note 4: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 5: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 6:  $V_{DD} = 24\text{ V}$ ,  $T_{ch} = 25\text{ }^{\circ}\text{C}$  (initial),  $L = 5.8\text{ }\mu\text{H}$ ,  $I_{AS} = 120\text{ A}$

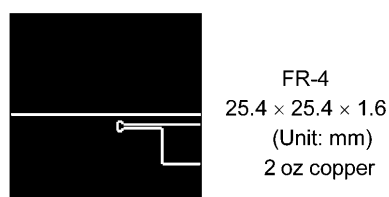


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

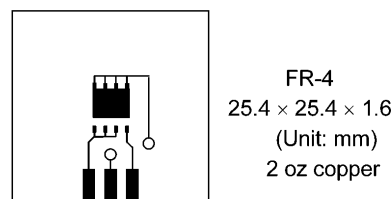


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

## 6. Electrical Characteristics

### 6.1. Static Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol        | Test Condition                                     | Min | Typ. | Max       | Unit             |
|-----------------------------------------|---------------|----------------------------------------------------|-----|------|-----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ | —   | —    | $\pm 0.1$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$     | —   | —    | 10        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}$ , $V_{GS} = 0\text{ V}$       | 30  | —    | —         | V                |
| Drain-source breakdown voltage (Note 7) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}$ , $V_{GS} = -20\text{ V}$     | 15  | —    | —         |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}$ , $I_D = 0.5\text{ mA}$     | 1.1 | —    | 2.1       |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 4.5\text{ V}$ , $I_D = 50\text{ A}$      | —   | 0.91 | 1.29      | $\text{m}\Omega$ |
|                                         |               | $V_{GS} = 10\text{ V}$ , $I_D = 50\text{ A}$       | —   | 0.61 | 0.92      |                  |

Note 7: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition                                                      | Min | Typ. | Max  | Unit        |
|--------------------------------|-----------|---------------------------------------------------------------------|-----|------|------|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ | —   | 5800 | 7540 | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |                                                                     | —   | 190  | 335  |             |
| Output capacitance             | $C_{oss}$ |                                                                     | —   | 1750 | —    |             |
| Gate resistance                | $r_g$     | —                                                                   | —   | 0.5  | 1.0  | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1                                                    | —   | 8    | —    | ns          |
| Switching time (turn-on time)  | $t_{on}$  |                                                                     | —   | 20   | —    |             |
| Switching time (fall time)     | $t_f$     |                                                                     | —   | 18   | —    |             |
| Switching time (turn-off time) | $t_{off}$ |                                                                     | —   | 71   | —    |             |

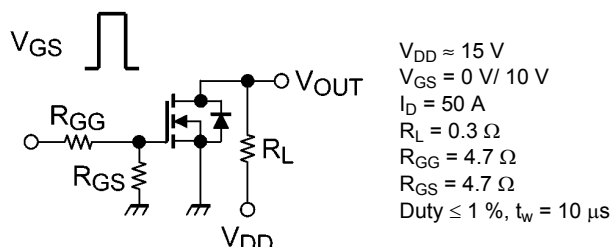


Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                                 | Symbol    | Test Condition                                                               | Min | Typ. | Max | Unit        |
|-------------------------------------------------|-----------|------------------------------------------------------------------------------|-----|------|-----|-------------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 15\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 50\text{ A}$  | —   | 81   | —   | $\text{nC}$ |
|                                                 |           | $V_{DD} \approx 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 50\text{ A}$ | —   | 38   | —   |             |
| Gate-source charge 1                            | $Q_{gs1}$ | $V_{DD} \approx 15\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 50\text{ A}$  | —   | 17   | —   |             |
| Gate-drain charge                               | $Q_{gd}$  |                                                                              | —   | 11   | —   |             |
| Gate switch charge                              | $Q_{SW}$  |                                                                              | —   | 19   | —   |             |
| Output charge                                   | $Q_{oss}$ | $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$          | —   | 51   | —   |             |

6.4. Source-Drain Characteristics (T<sub>a</sub> = 25 °C unless otherwise specified)

| Characteristics                         | Symbol           | Test Condition                                          | Min | Typ. | Max  | Unit |
|-----------------------------------------|------------------|---------------------------------------------------------|-----|------|------|------|
| Reverse drain current (pulsed) (Note 8) | I <sub>DRP</sub> | (t = 100 μs)                                            | —   | —    | 500  | A    |
| Diode forward voltage                   | V <sub>DSF</sub> | I <sub>DR</sub> = 150 A, V <sub>GS</sub> = 0 V          | —   | —    | -1.2 | V    |
| Reverse recovery time                   | t <sub>rr</sub>  | V <sub>R</sub> = 15 V, I <sub>DR</sub> = 37.5 A,        | —   | 46   | —    | ns   |
| Reverse recovery charge                 | Q <sub>rr</sub>  | V <sub>GS</sub> = 0 V, -dI <sub>DR</sub> /dt = 100 A/μs | —   | 44   | —    | nC   |

Note 8: Ensure that the channel temperature does not exceed 175 °C.

7. Marking

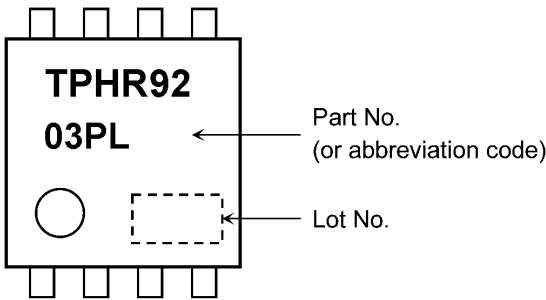


Fig. 7.1 Marking

## 8. Characteristics Curves (Note)

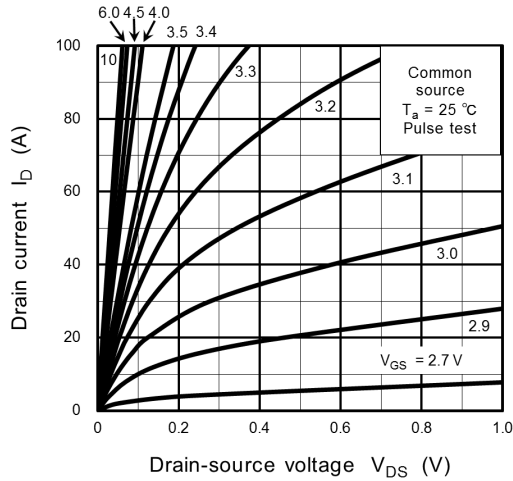


Fig. 8.1  $I_D - V_{DS}$

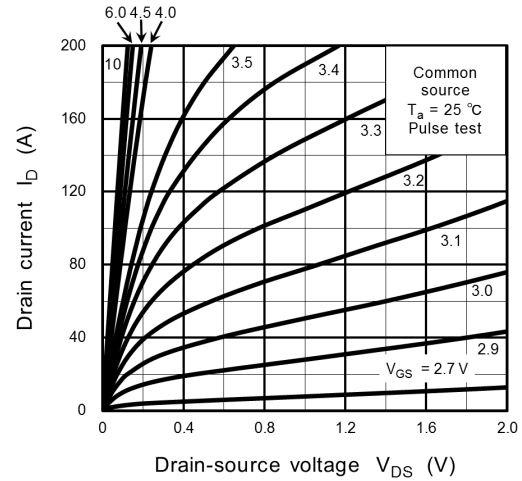


Fig. 8.2  $I_D - V_{DS}$

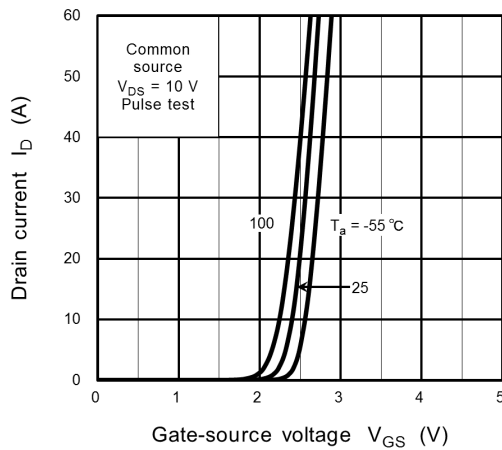


Fig. 8.3  $I_D - V_{GS}$

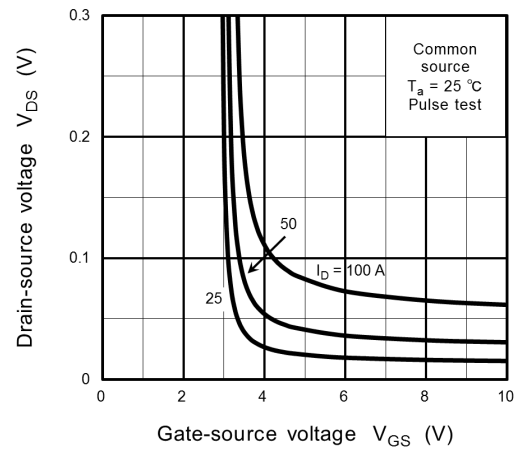


Fig. 8.4  $V_{DS} - V_{GS}$

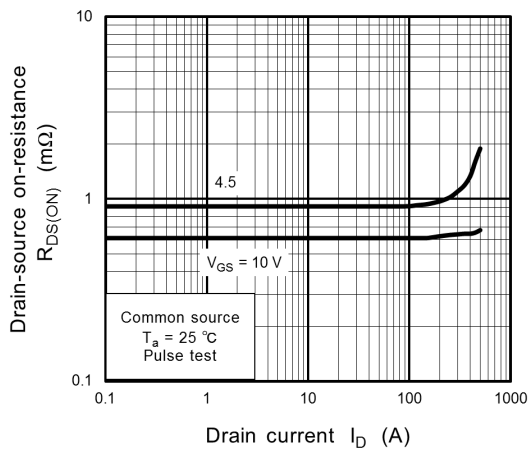


Fig. 8.5  $R_{DS(ON)} - I_D$

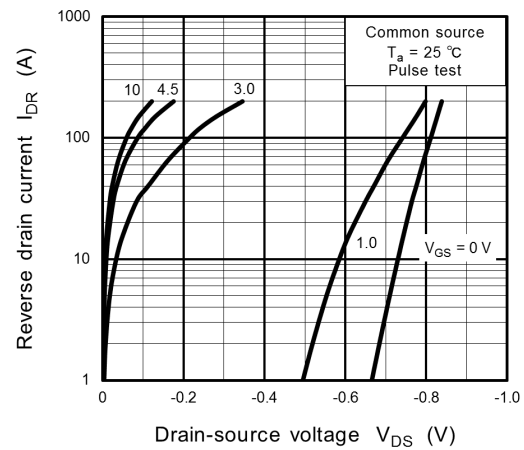


Fig. 8.6  $I_{DR} - V_{DS}$

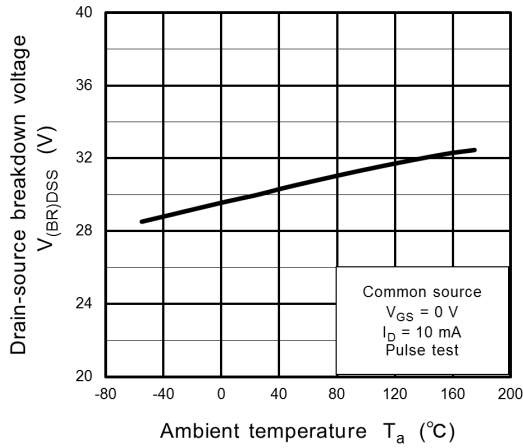


Fig. 8.7  $V_{(BR)DSS} - T_a$

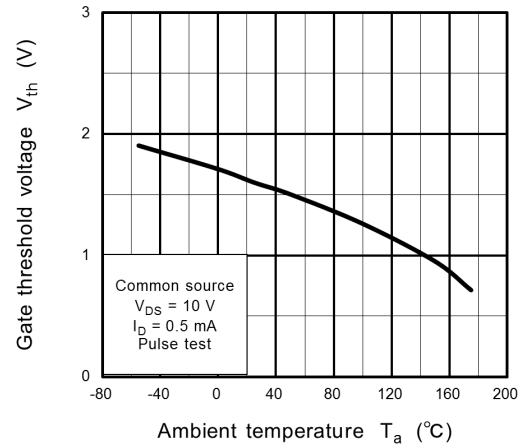


Fig. 8.8  $V_{th} - T_a$

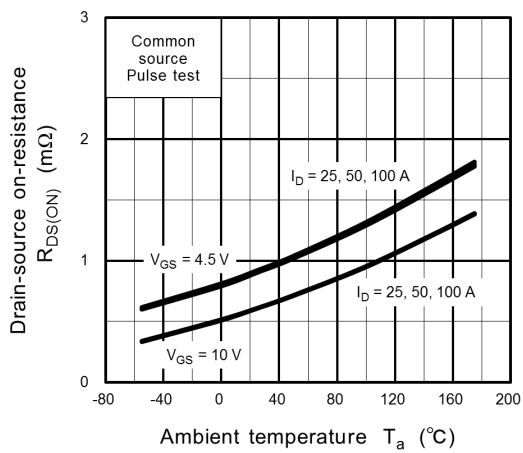


Fig. 8.9  $R_{DS(ON)} - T_a$

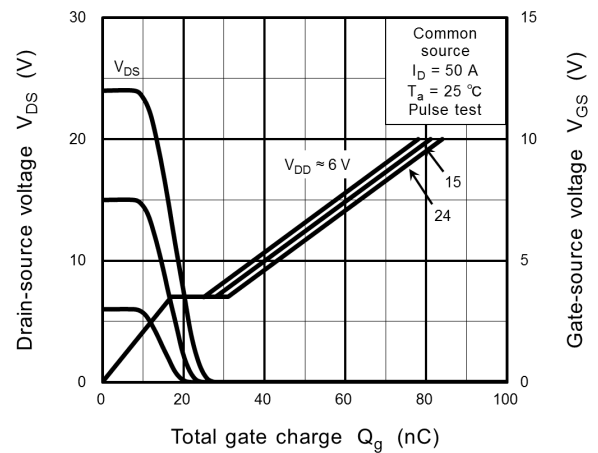


Fig. 8.10 Dynamic Input/Output Characteristics

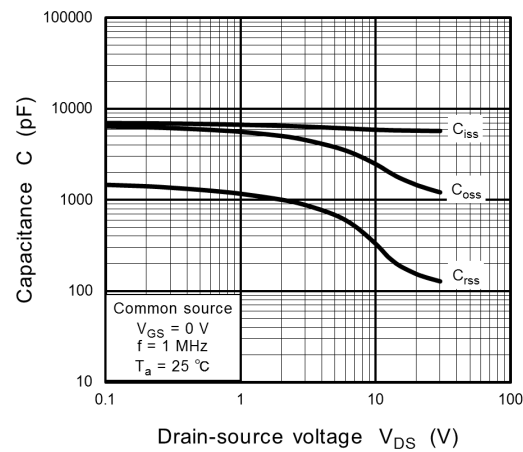


Fig. 8.11 Capacitance -  $V_{DS}$

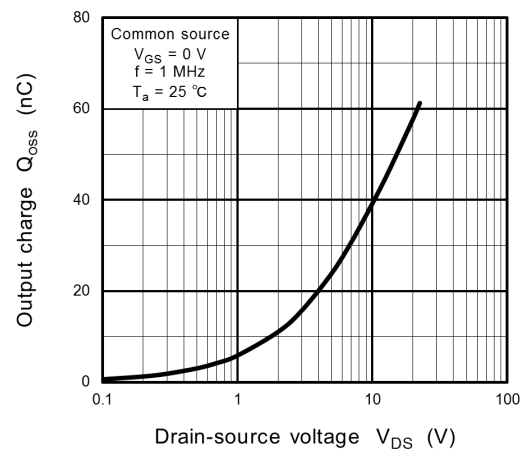
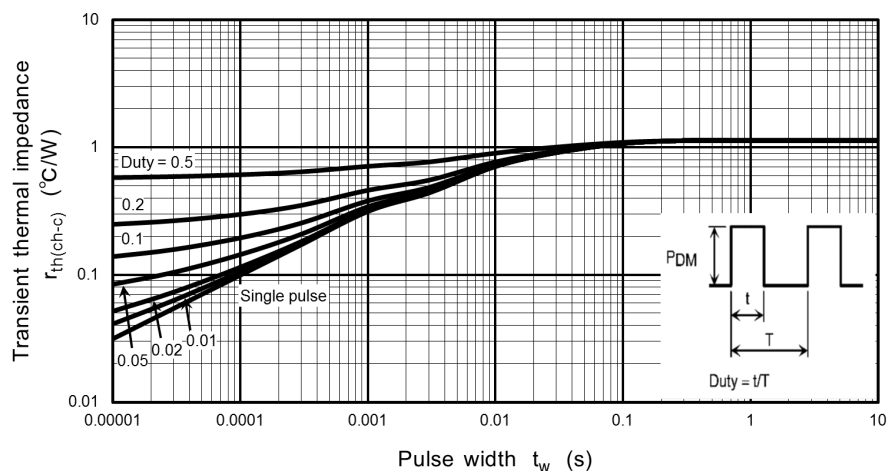
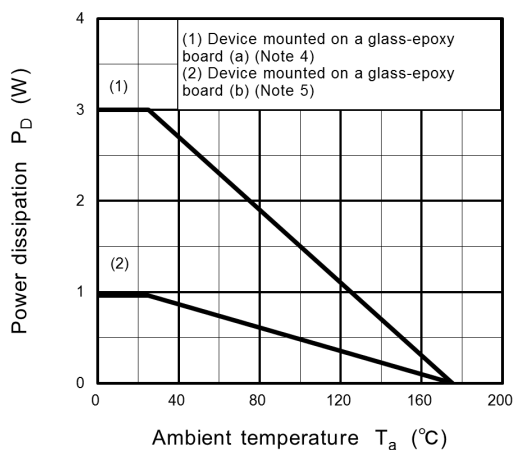


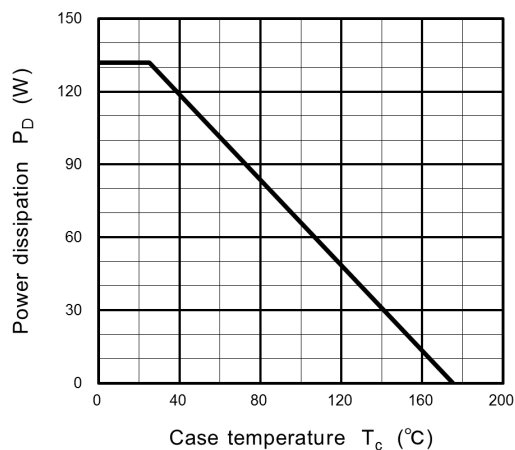
Fig. 8.12  $Q_{oss} - V_{DS}$



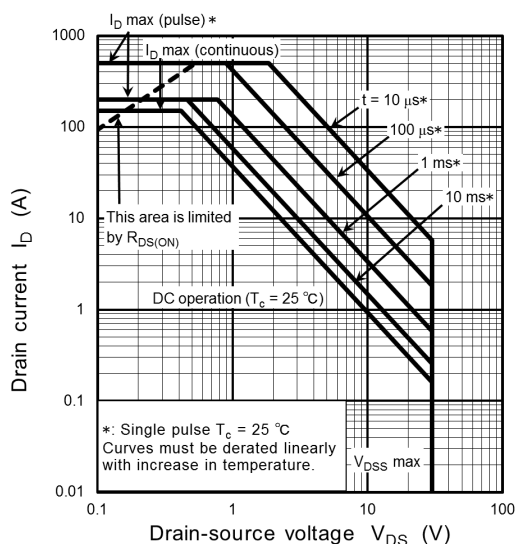
**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_a$**   
(Guaranteed Maximum)



**Fig. 8.15  $P_D - T_c$**   
(Guaranteed Maximum)

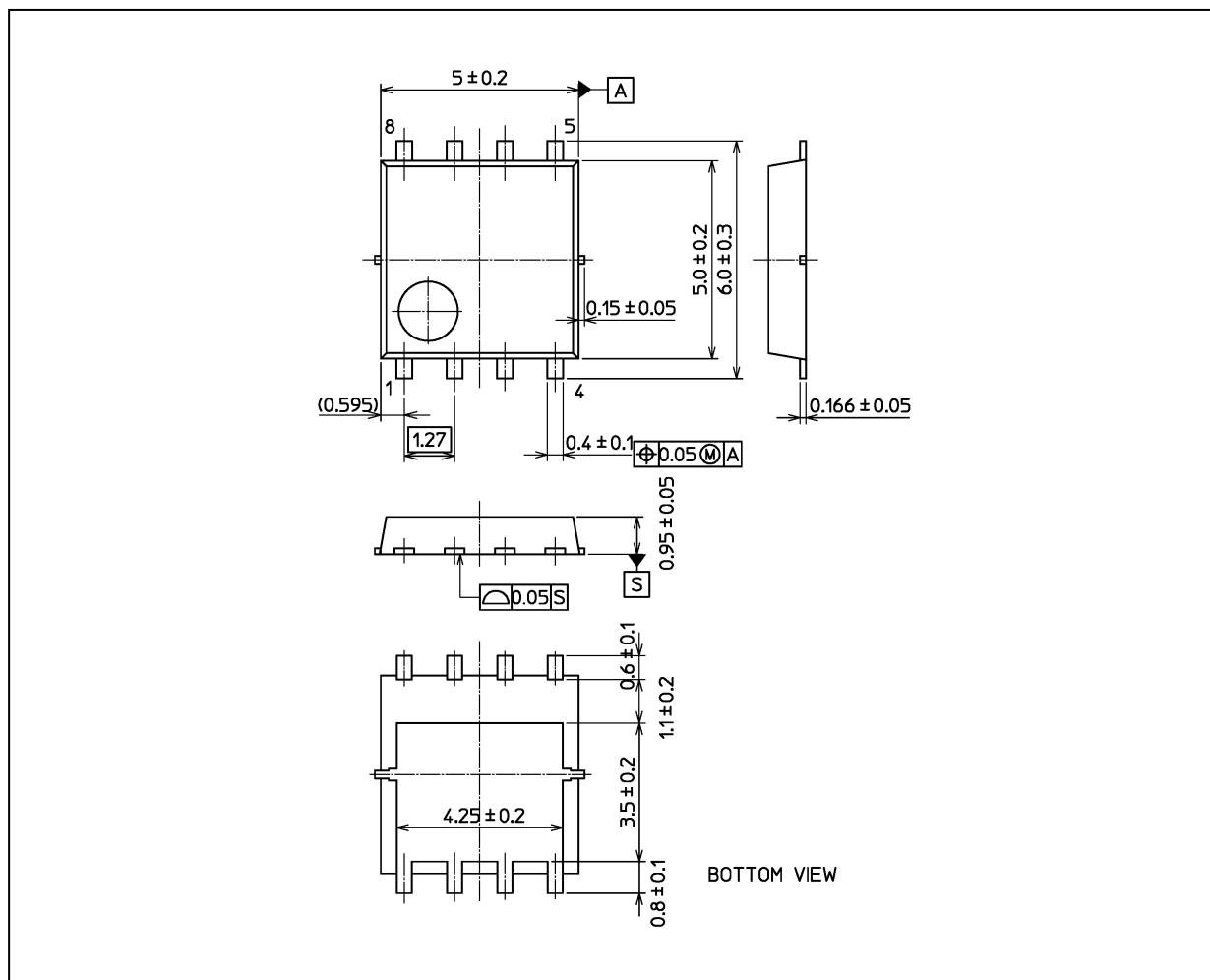


**Fig. 8.16 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm



The package can be selected according to your preference. For details, please contact your TOSHIBA sales representative.

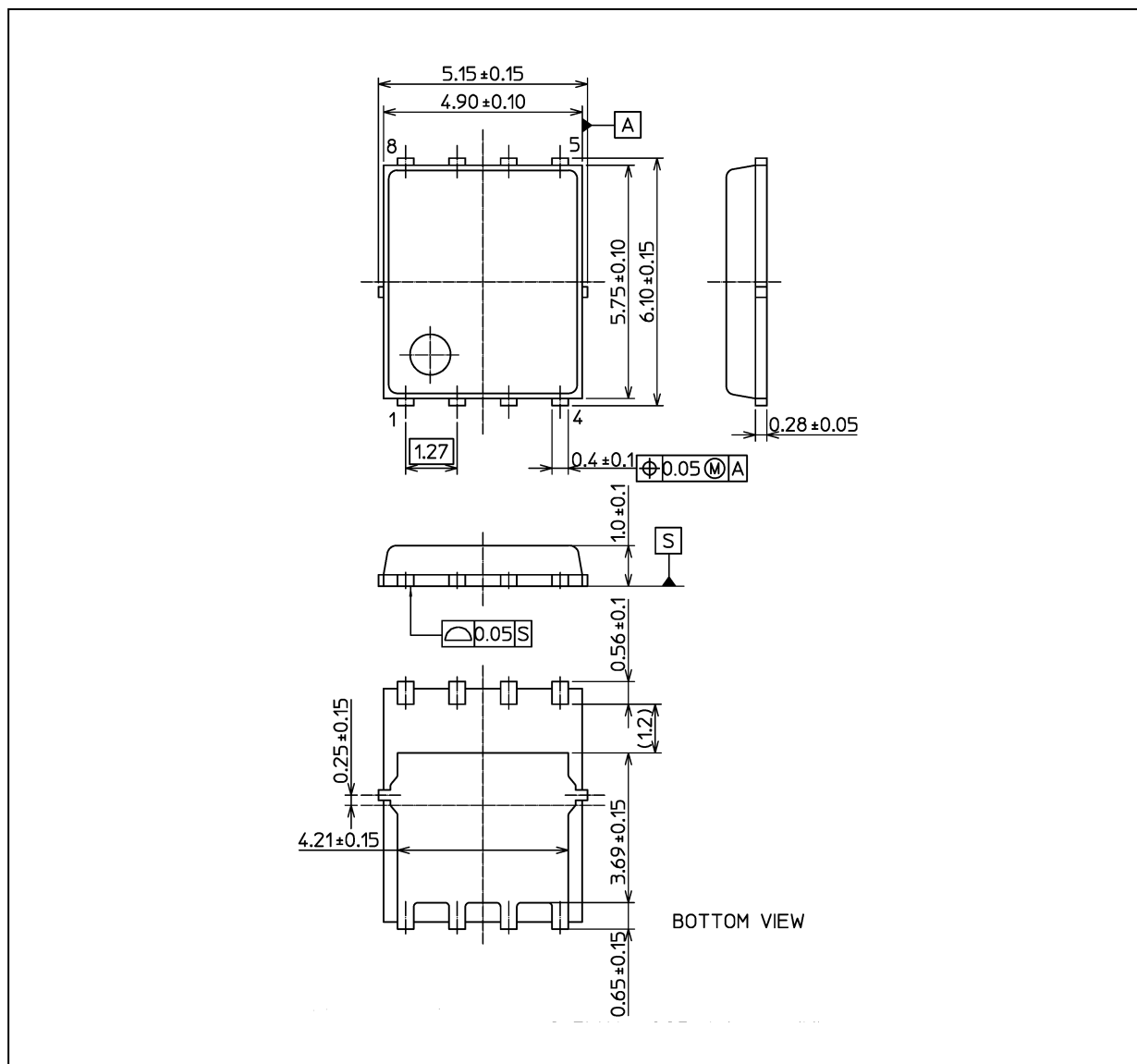
Weight: 0.079 g (typ.)

| Package Name(s)       |
|-----------------------|
| TOSHIBA: 2-5Q1S       |
| Nickname: SOP Advance |



## Package Dimensions

Unit: mm



The package can be selected according to your preference. For details, please contact your TOSHIBA sales representative.

Weight: 0.105 g (typ.)

| Package Name(s)          |
|--------------------------|
| TOSHIBA: 2-5W1A          |
| Nickname: SOP Advance(N) |

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