SLIS049 - NOVEMBER 1996

- Low r_{DS(on)} . . . 0.3 Ω Typ
- High Output Voltage . . . 60 V
- Pulsed Current . . . 6 A Per Channel
- Avalanche Energy Capability . . . 36 mJ
- Input Transient Protection ... 2000 V

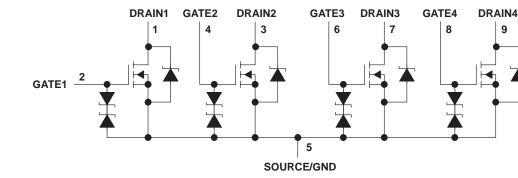
description

schematic

The TPIC2401 is a monolithic power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. Each transistor features integrated high-current zener diodes to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 2000 V of ESD protection when tested using the human-body model.

The TPIC2401 is offered in a 9-pin PowerFLEXTM (KTA) package and is characterized for operation over the case temperature range of -40° C to 125°C.

KTA PACKAGE (TOP VIEW) q 🔟 DRAIN4 🔟 GATE4 8 7 GATE3 6 SOURCE/GND 5 □ GATE2 4 3 □ GATE1 2 1 □ DRAIN1



NOTE A: For correct operation, no output pin may be taken below GND.



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SLIS049 - NOVEMBER 1996

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V _{DS}	
Continuous drain current, each output, all outputs on, T _C = 25°C	1.5 A
Pulsed drain current, each output, I_Omax , $T_C = 25^{\circ}C$ (see Note 1 and Figure 7)	6 A
Continuous gate-to-source zener diode current, T _C = 25°C	±25 mA
Pulsed gate-to-source zener diode current, $T_C = 25^{\circ}C$	±250 mA
Single-pulse avalanche energy, E_{AS} , $T_{C} = 25^{\circ}C$ (see Figures 4 and 6)	
Continuous total power dissipation at (or below) T _A = 25°C	1.7 W
Power dissipation at (or below) T _C = 75°C, all outputs on	
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range, T _{stg}	–40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	$V_{GS} = 0$	60			V
VGS(th)	Gate-to-source threshold voltage	I _D = 1 mA,	V _{DS} = V _{GS} ,	1.5	2.05	2.2	V
VGS(th)match	Gate-to-source threshold voltage matching	See Figure 5			5	40	V
V(BR)GS	Gate-to-source breakdown voltage	IGS = 250 μA		18			V
V(BR)SG	Source-to-gate breakdown voltage	I _{SG =} 250 μA		9			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 1.5A, See Notes 2 and 3	V _{GS} = 10 V,		0.45	0.54	V
V _{F(SD)}	Forward on-state voltage, source-to-drain	$I_S = 1.5A$, $V_{GS} = 0 V$, See Notes 2 and 3 and Figure 12			0.85	1	V
		V _{DS} = 48 V,	$T_{C} = 25^{\circ}C$		0.05	1	μA
IDSS	Zero-gate-voltage drain current	$V_{GS} = 0$	$T_{C} = 125^{\circ}C$		0.5	10	
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 15 V,	$V_{DS} = 0$		20	200	nA
IGSSR	Reverse gate current, drain short circuited to source	$V_{SG} = 5 V,$	$V_{DS} = 0$		10	100	nA
•	Static duais to acurac an atota registerios	V _{GS} = 10 V, I _D =1.5 A,	$T_{C} = 25^{\circ}C$		0.3	0.36	0
^r DS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7 $T_{C} = 125^{\circ}C$		0.48	0.6	Ω	
9fs	Forward transconductance	V _{DS} = 15 V, See Notes 2 and 3 ar	I _D = 1 A, nd Figure 9	0.9	1.15		S
C _{iss}	Short-circuit input capacitance, common source				180	225	
C _{OSS}	Short-circuit output capacitance, common source	V _{DS} = 25 V, f = 1 MHz,	V _{GS} = 0, See Figure 11		100	138	pF
C _{rss}	Short-circuit reverse transfer capacitance, common source	, – , , , , , , , , , , , , , , , , , ,			75	100	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



SLIS049 - NOVEMBER 1996

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{rr}	Reverse-recovery time	$I_{S} = 0.75 \text{ A}, V_{DS} = 48 \text{ V},$		80		ns
Q _{RR}	Total diode charge	V _{GS} = 0, di/dt = 100 A/μs, See Figures 1 and 14		180		nC

resistive-load switching characteristics, T_C = 25°C

	PARAMETER	Т	EST CONDITION	IS	MIN	TYP	MAX	UNIT	
^t d(on)	Delay time, V_{GS}^{\uparrow} to V_{DS}^{\downarrow} turn on					194			
^t d(off)	Delay time, $V_{GS}\downarrow$ to $V_{DS}\uparrow$ turn off	V _{DD} = 25 V,	/ _{DD} = 25 V, R _L = 25 Ω,	t _{en} = 10 ns,		430			
tr	Rise time, V _{DS}			See Figure 2	180		ns		
t _f	Fall time, V _{DS}					90			
Qg	Total gate charge					4	5		
Qgs(th)	Threshold gate-to-source charge	V _{DD} = 48 V, See Figure 3	I _D = 1 A,	I A, V _{GS} = 10 V,		0.45	0.56	nC	
Q _{gd}	Gate-to-drain charge					1.55	1.93		
LD	Internal drain inductance					5		الم	
LS	Internal source inductance					5		nH	
Rg	Internal gate resistance					500		Ω	

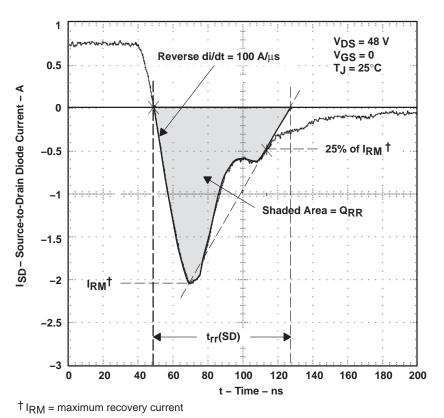
thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			72	
R _{θJC}	Junction-to-case thermal resistance	All outputs with equal power			5	°C/W
		One output dissipating power			8.5	

NOTES:

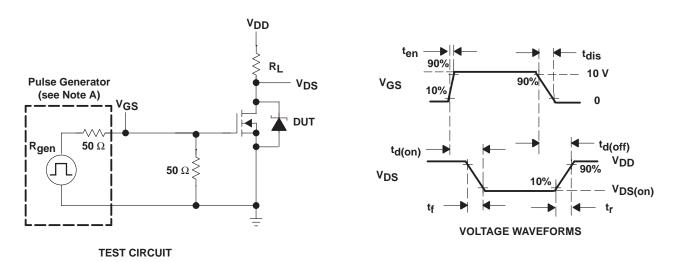


SLIS049 - NOVEMBER 1996



PARAMETER MEASUREMENT INFORMATION

Figure 1. Reverse-Recovery Current Waveform of Source-to-Drain Diode

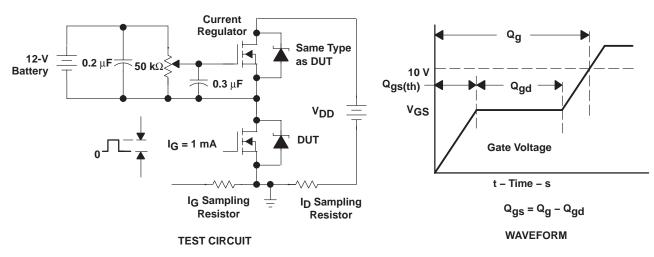


NOTE A: The pulse generator has the following characteristics: $t_{en} \le 10$ ns, $t_{dis} \le 10$ ns, $Z_O = 50 \Omega$.

Figure 2. Resistive Switching

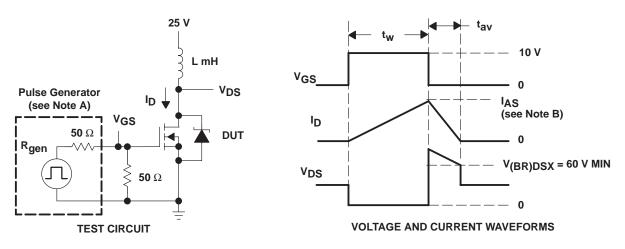


SLIS049 - NOVEMBER 1996



PARAMETER MEASUREMENT INFORMATION



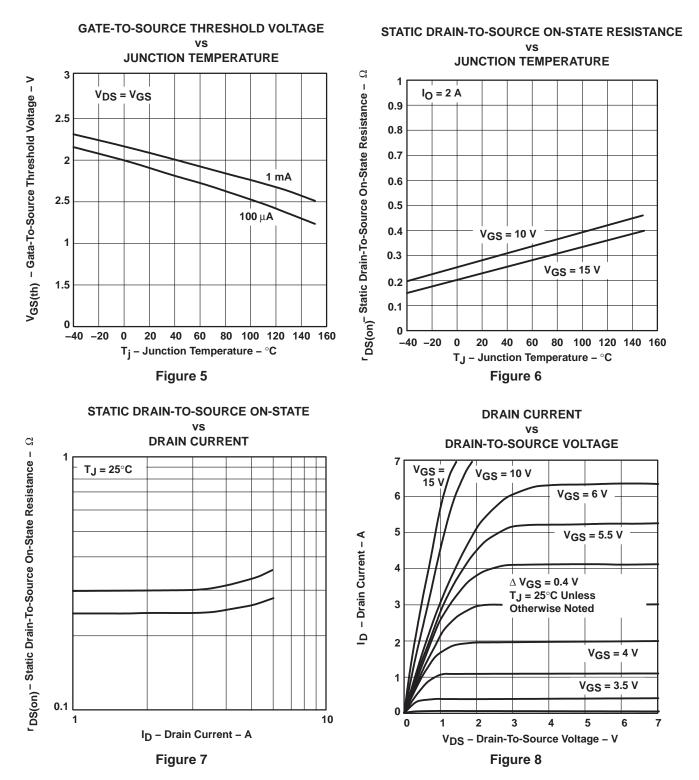


NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50 \Omega$. B. Input pulse duration (t_W) is increased until peak current I_{AS} = 1.5 A. Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 36 \text{ mJ}$ minimum where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms



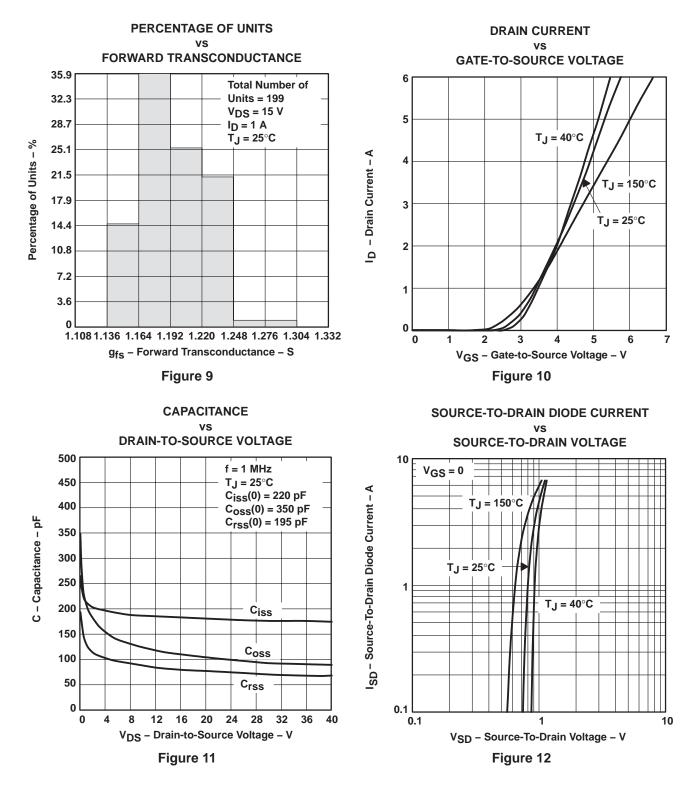
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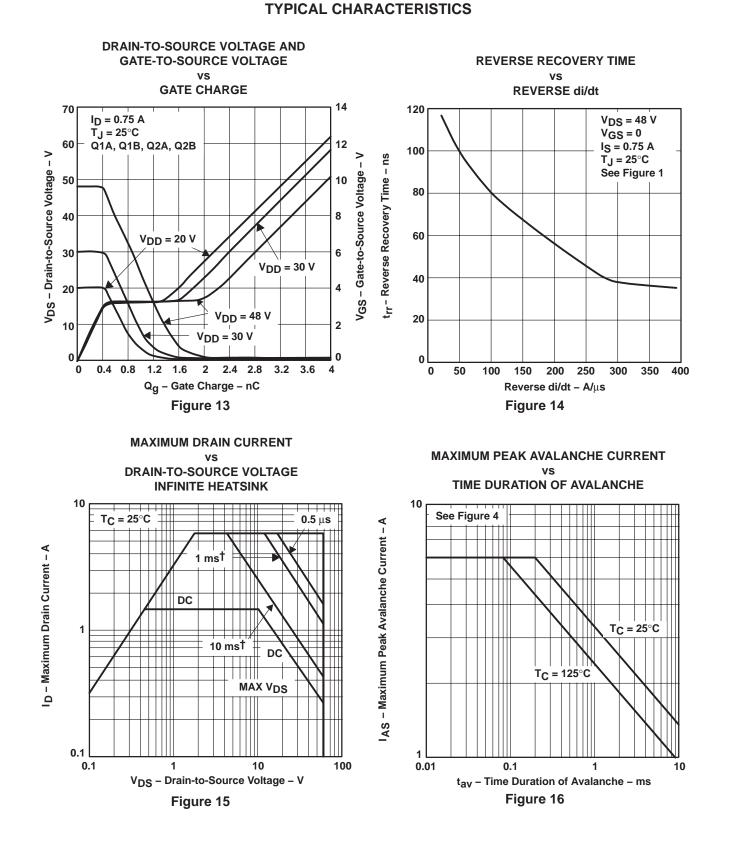
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TYPICAL CHARACTERISTICS



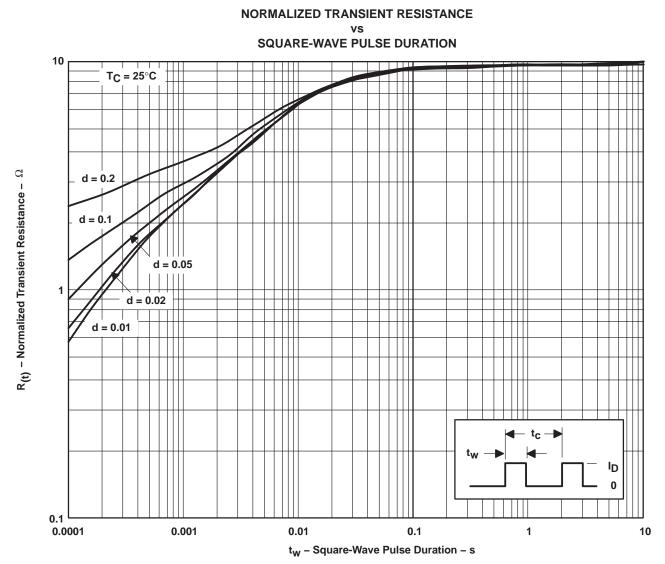
SLIS049 - NOVEMBER 1996





SLIS049 - NOVEMBER 1996

THERMAL INFORMATION



[†] Package mounted in intimate contact with infinite heat sink.

NOTE A: $Z_{\Theta JC}(t) = r(t) R_{\Theta JC}$ $t_W = pulse duration$ $t_C = cycle time$ $d = duty cycle = t_W/t_C$

Figure 17



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