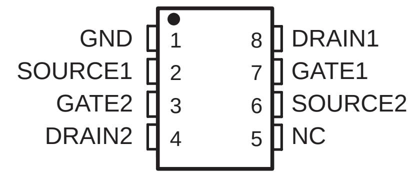
TPIC5203
2-CHANNEL INDEPENDENT GATE-PROTECTED POWER DMOS ARRAY

SLIS040 − SEPTEMBER 1994

- **Low $r_{DS(on)}$ . . . 0.26 Ω Typ**
- **High Voltage Output . . . 60 V**
- **Extended ESD Capability . . . 4000 V**
- **Pulsed Current . . . 8 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)



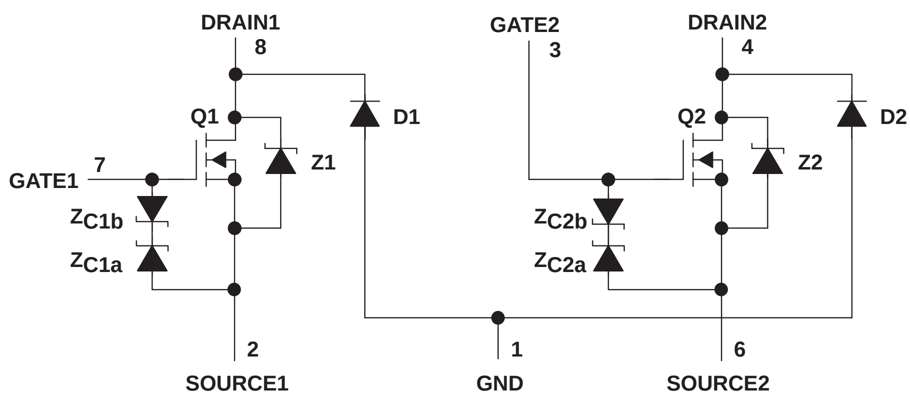
NC − No internal connection

description

The TPIC5203 is a monolithic gate-protected power DMOS array that consists of two independent electrically isolated N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-kΩ resistor.

The TPIC5203 is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2)	100 V
Drain-to-GND voltage (Q1, Q2)	100 V
Gate-to-source voltage range, V_{GS}	−9 V to 18 V
Continuous drain current, each output, T_C = 25°C	1.6 A
Continuous source-to-drain diode current, T_C = 25°C	1.6 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	8 A
Continuous gate-to-source zener diode current, T_C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T_C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figures 4, 15, and 16)	21.6 mJ
Continuous total dissipation, T_C = 25°C (see Figure 15)	962 mW
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 5		1.5	2.05	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	I_{GS} = 250 µA		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	I_{SG} = 250 µA		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1.6 A, V_{GS} = 10 V, See Notes 2 and 3			0.42	0.5	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.6 A, V_{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1.6 A (D1, D2), See Notes 2 and 3			5		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	V_{GS} = 15 V, V_{DS} = 0			20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	V_{SG} = 5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.6 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.26	0.31	Ω
			T_C = 125°C		0.41	0.45	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 800 mA, See Notes 2 and 3 and Figure 9		1.5	1.83		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 11			150	275	pF
C_{oss}	Short-circuit output capacitance, common source				100	150	
C_{rss}	Short-circuit reverse transfer capacitance, common source				40	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 800 mA, V_{DS} = 48 V, V_{GS} = 0, di/dt = 100 A/µs, See Figures 1 and 14	Z1 and Z2		50		ns
			D1 and D2		265		
Q_{RR}	Total diode charge		Z1 and Z2		63		nC
			D1 and D2		1240		

resistive-load switching characteristics, T_C = 25°C

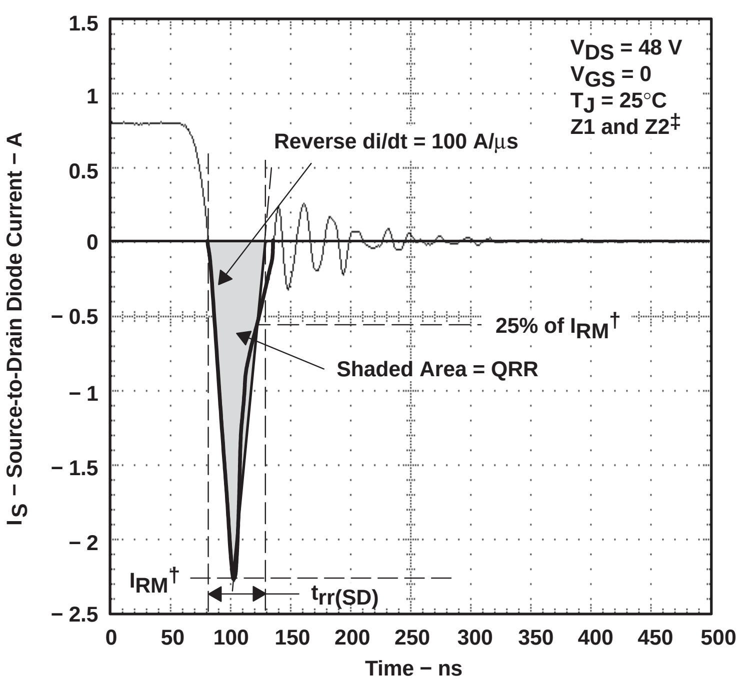
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 30 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			27	50	
t_r	Rise time			15	30	
t_f	Fall time			7	15	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.8 A, V_{GS} = 10 V, See Figure 3		4.7	5.9	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			1.9	2.4	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7		130		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7		79		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7		34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink
5. Package mounted on a 24 inch^2, 4-layer FR4 printed-circuit board
6. Package mounted in intimate contact with infinite heatsink
7. All outputs with equal power

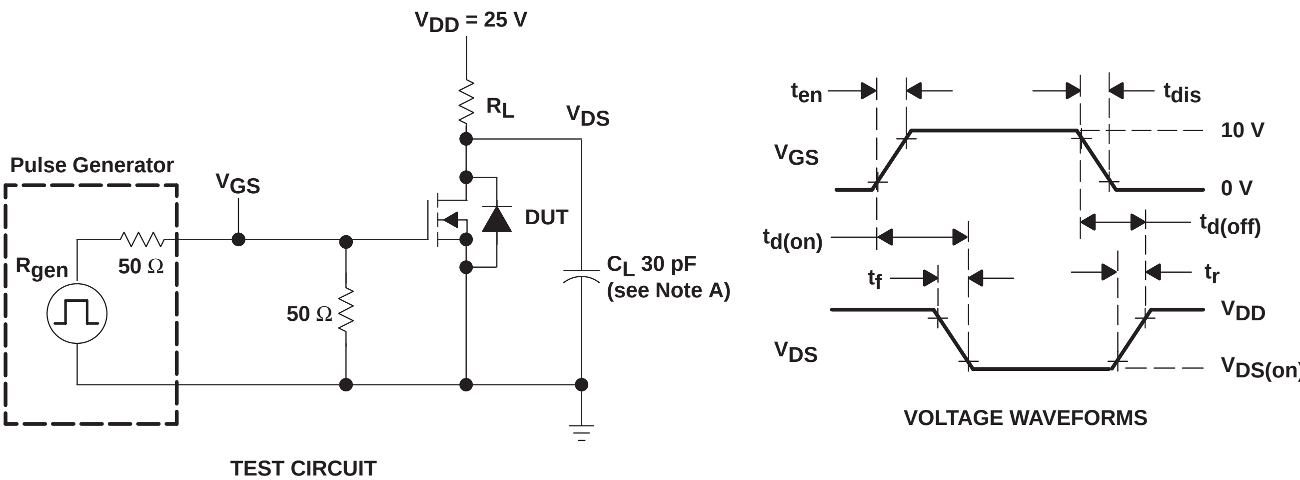
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current
‡ The above waveform is representative of D1 and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

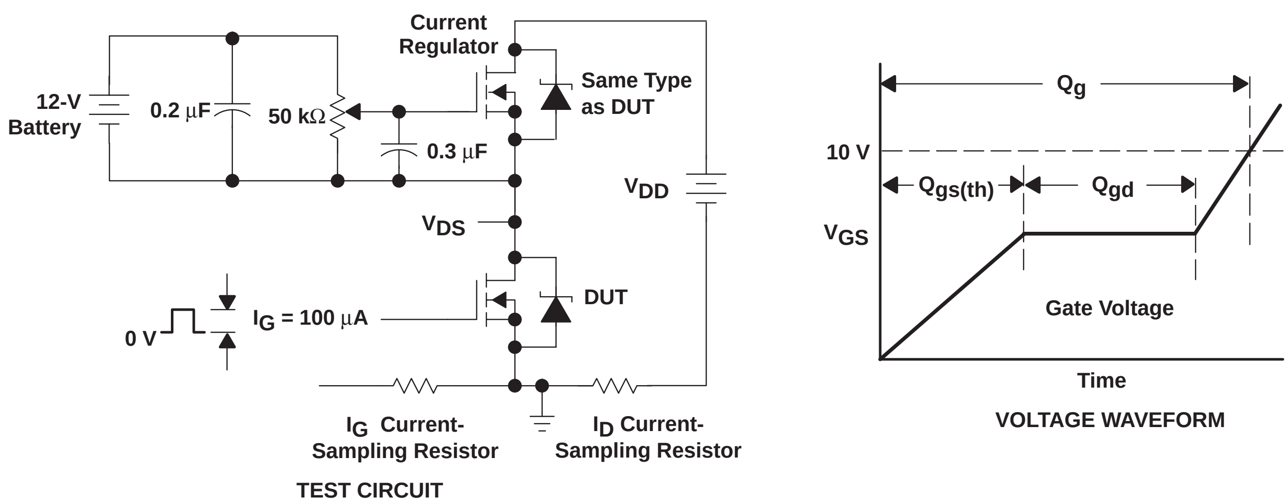
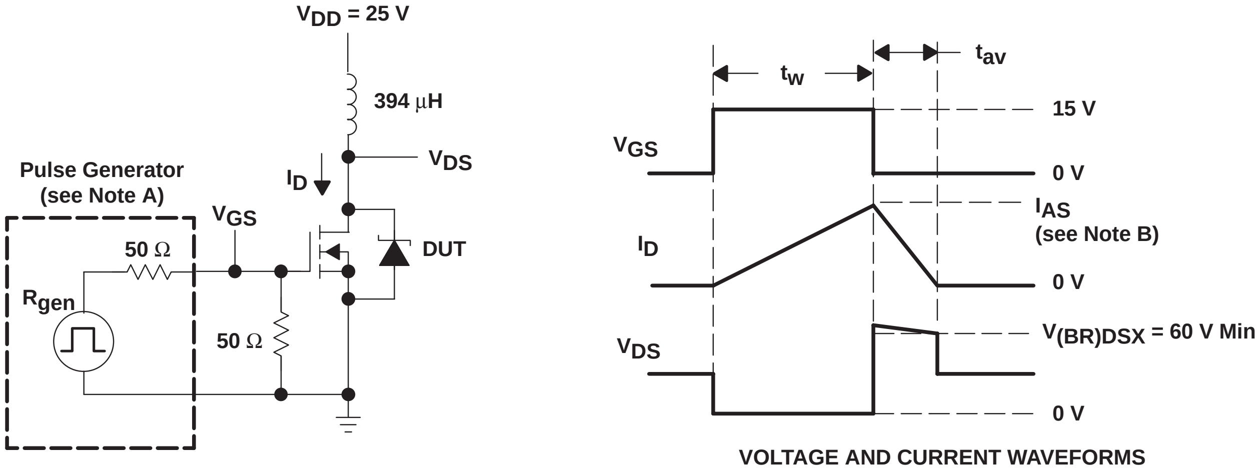


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



VOLTAGE AND CURRENT WAVEFORMS

TEST CIRCUIT

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 8$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21.6$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

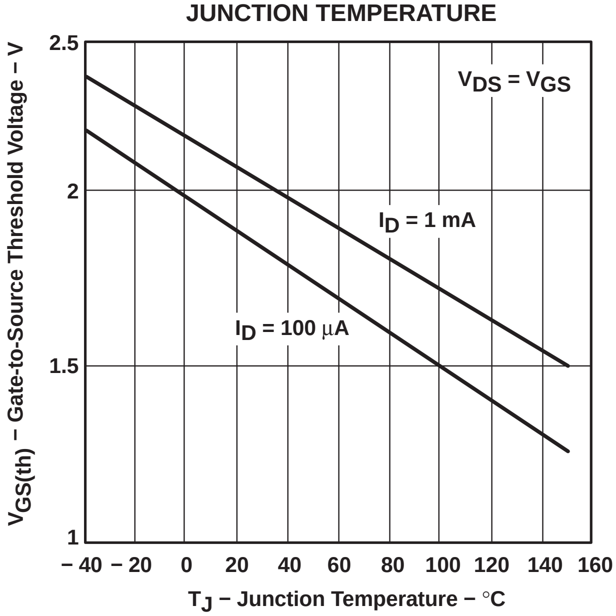


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

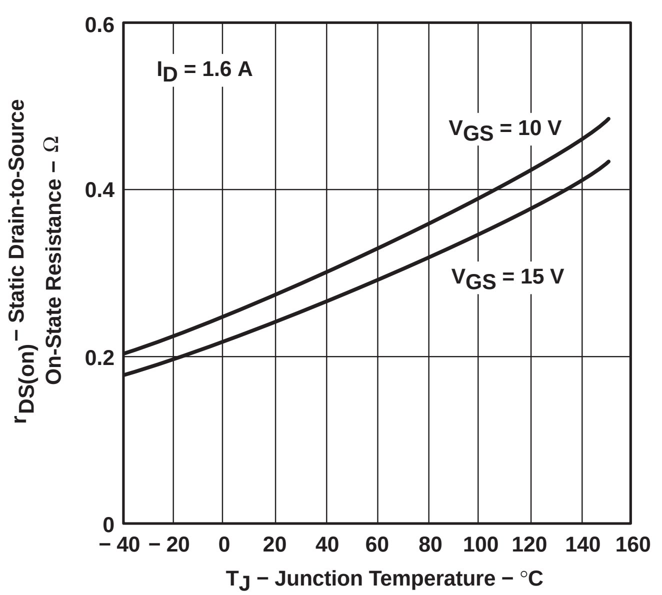


Figure 6

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

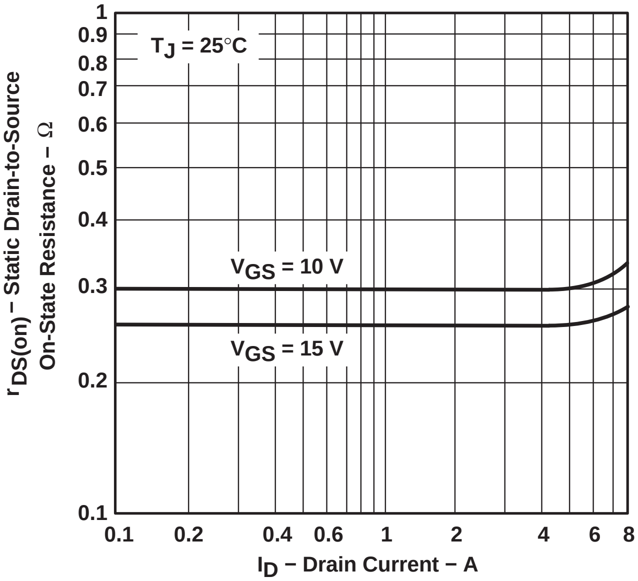


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

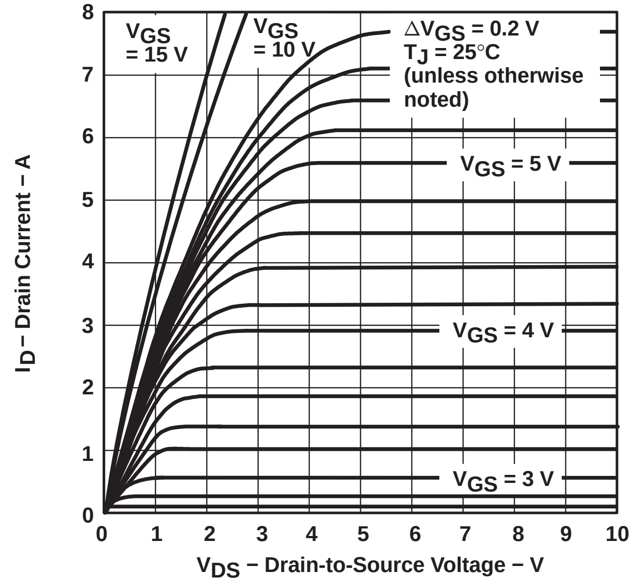


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

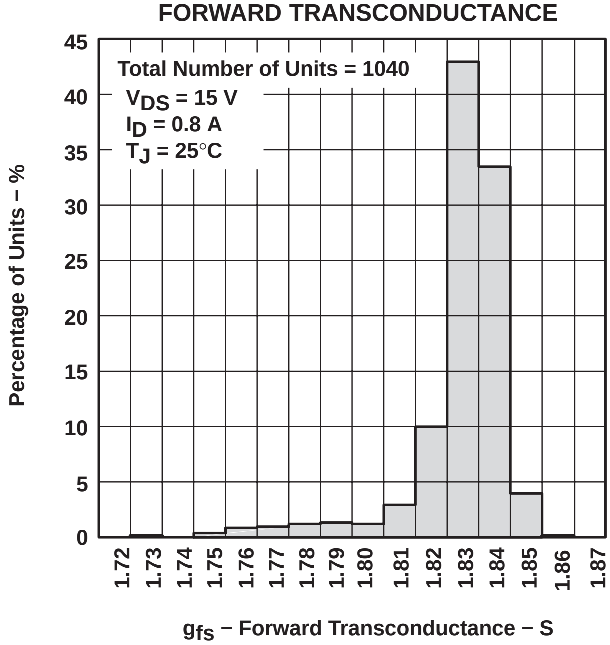


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

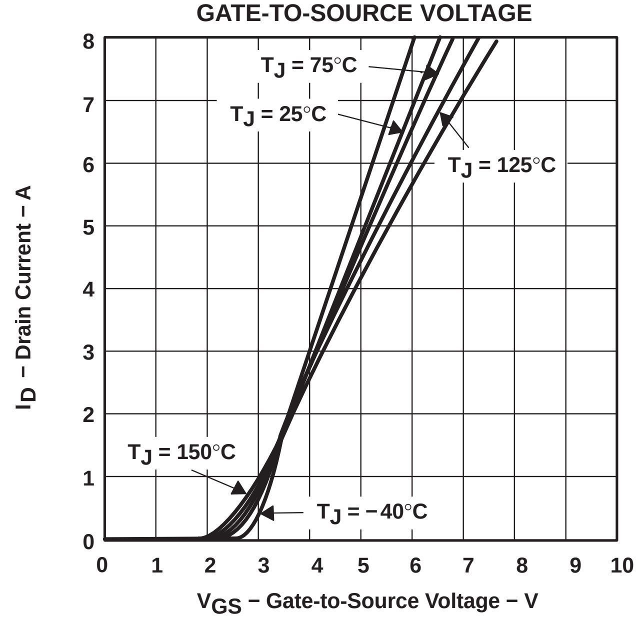


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

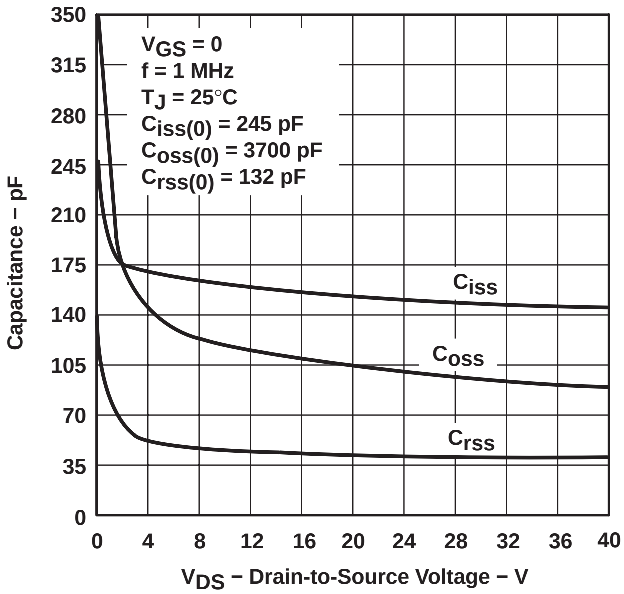


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

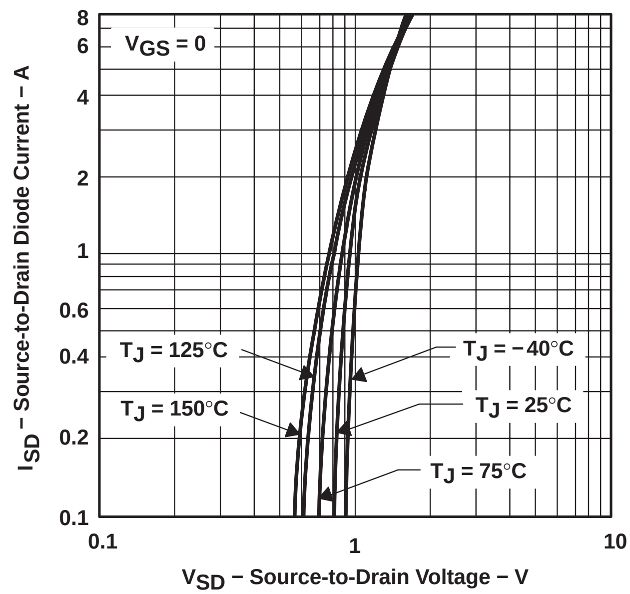


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

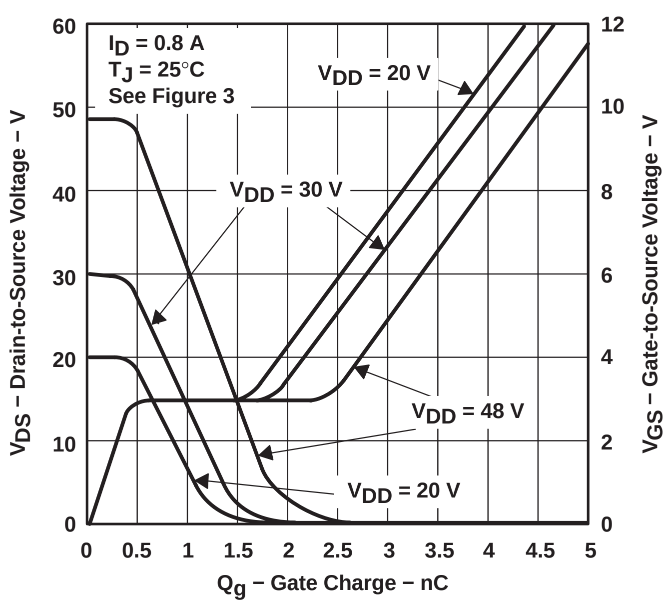


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE di/dt

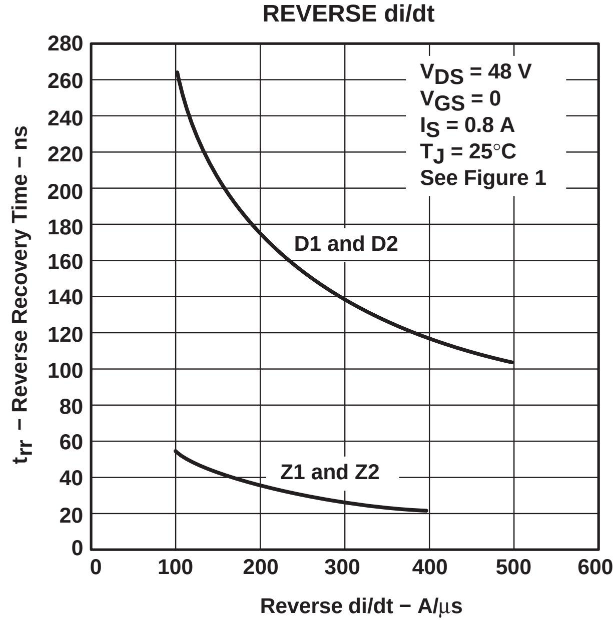
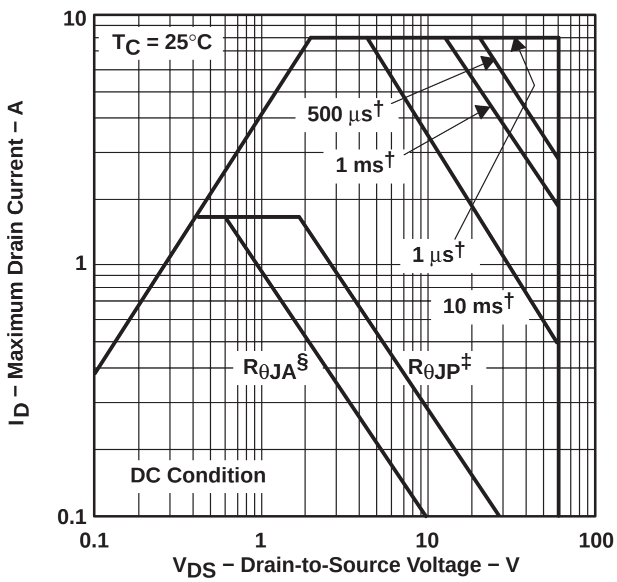


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle
‡ Device mounted in intimate contact with infinite heatsink.
§ Device mounted on FR4 printed circuit board with no heatsink.

Figure 15

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

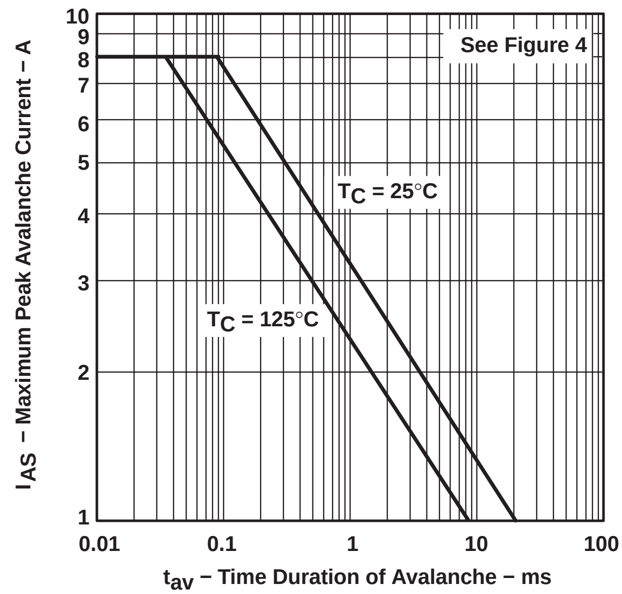
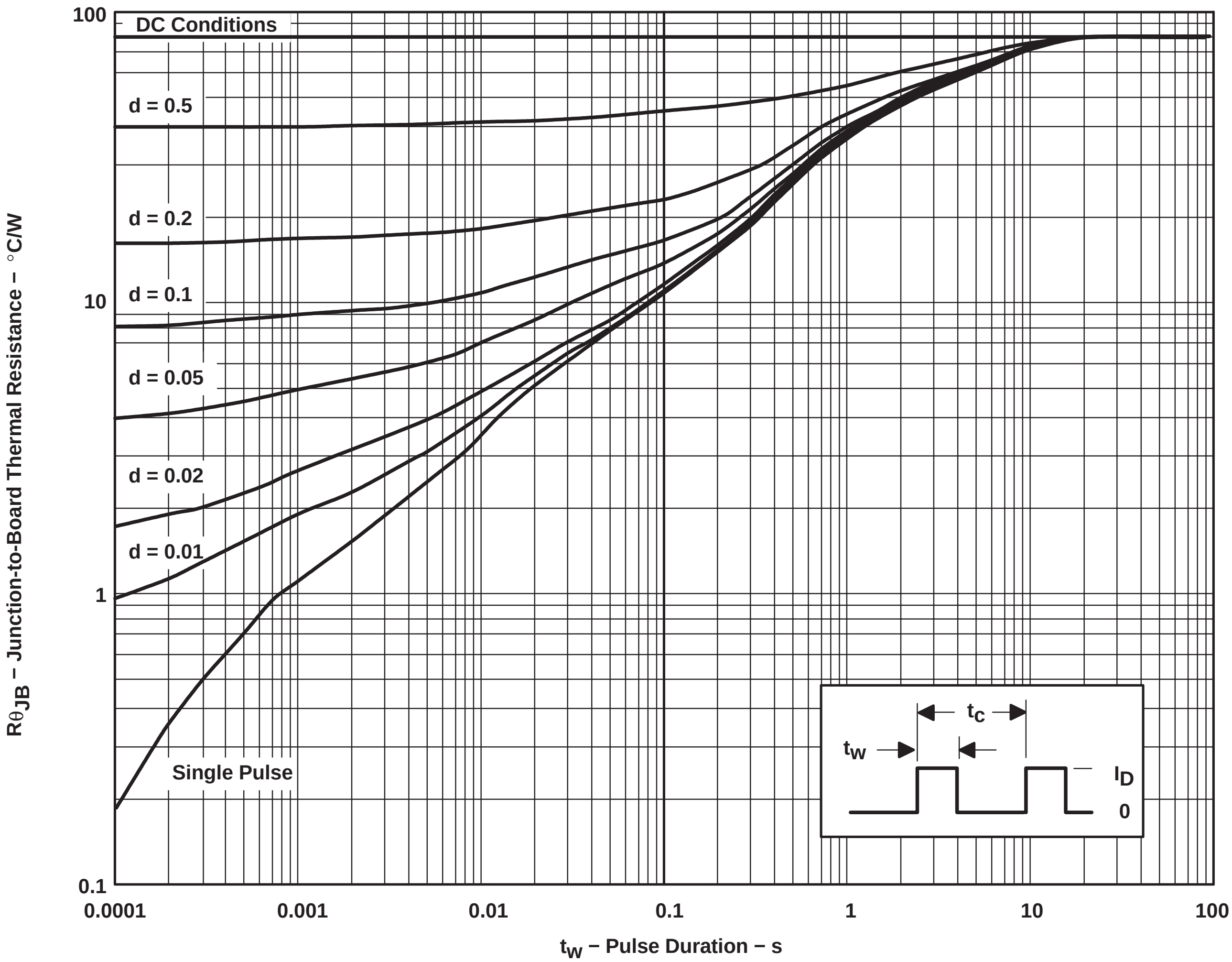


Figure 16

THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink

NOTE A. $Z_{\theta JB}(t) = r(t)R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 17

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPIC5203D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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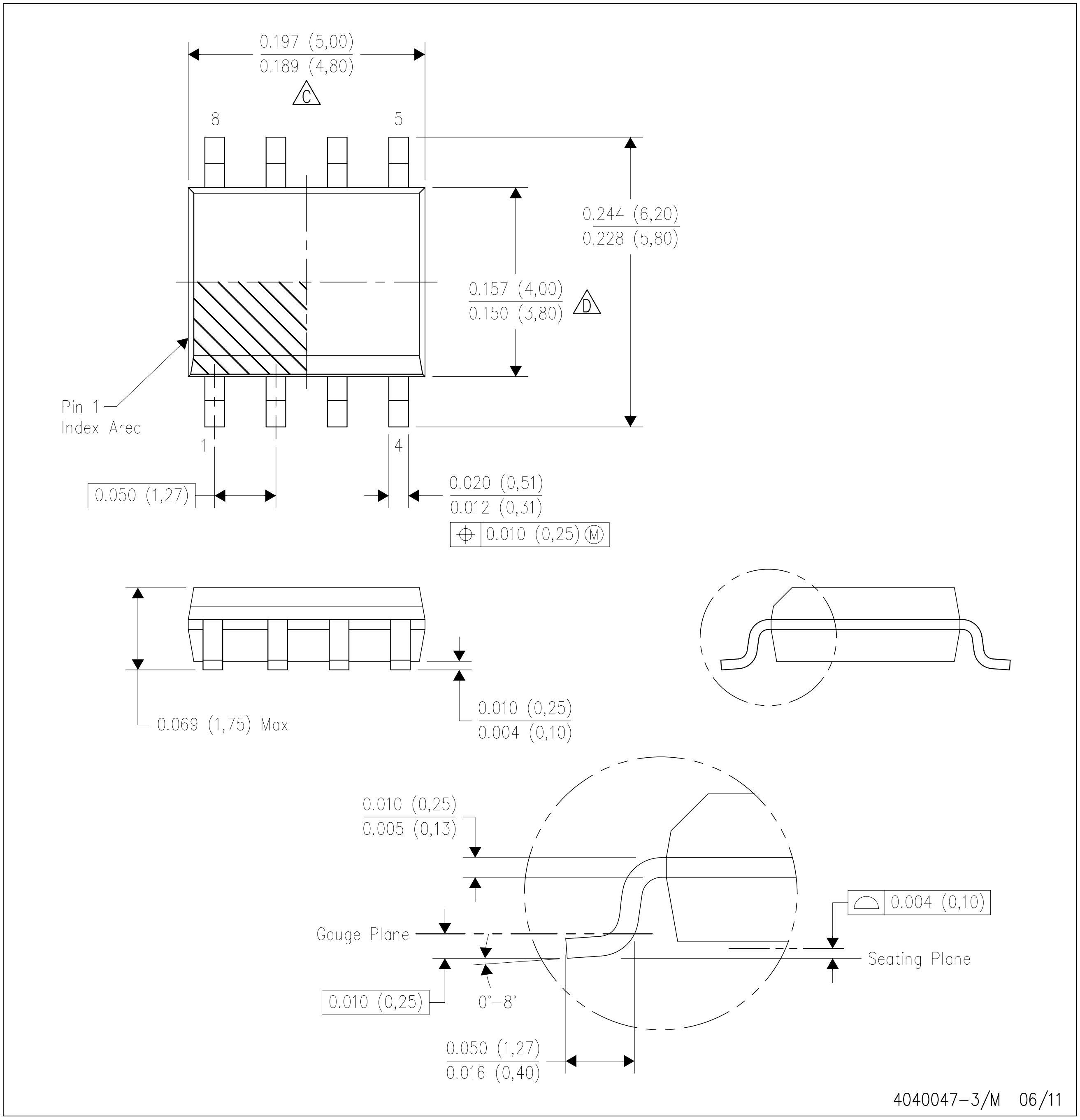
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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