

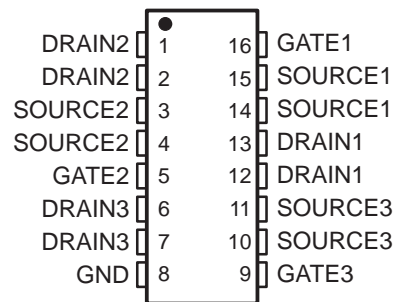
# TPIC5323L

## 3-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS044A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

- Low  $r_{DS(on)}$  . . . 0.6  $\Omega$  Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

**D PACKAGE  
(TOP VIEW)**

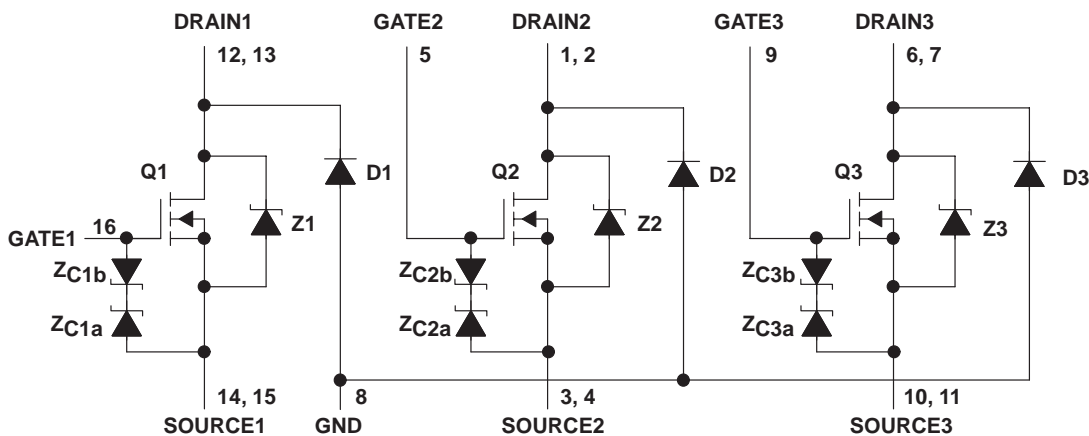


### description

The TPIC5323L is a monolithic gate-protected logic-level power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes ( $Z_{CXa}$  and  $Z_{CXb}$ ) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k $\Omega$  resistor.

The TPIC5323L is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### schematic



NOTE A: For correct operation, no terminal can be taken below GND.

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### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, $V_{DS}$	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, $V_{GS}$	-9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1 A
Pulsed drain current, each output, $I_{max}$ , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	$\pm 50$ mA
Pulsed gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	$\pm 500$ mA
Single-pulse avalanche energy, $E_{AS}$ , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	22.5 mJ
Continuous total power dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	1.09 W
Operating virtual junction temperature range, $T_J$	$-40^\circ\text{C}$ to $150^\circ\text{C}$
Operating case temperature range, $T_C$	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



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### electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$ ,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$ , See Figure 5	$V_{DS} = V_{GS}$	1.5	1.8	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250 \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250 \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, D3)	Drain-to-GND current = $250 \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1 \text{ A}$ , See Notes 2 and 3	$V_{GS} = 5 \text{ V}$ ,		0.6	0.7	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1 \text{ A}$ , $V_{GS} = 0$ (Z1, Z2, Z3), See Notes 2 and 3 and Figure 12			0.9	1.1	V
$V_F$	Forward on-state voltage, GND-to-drain	$I_D = 1 \text{ A}$ (D1, D2, D3), See Notes 2 and 3			4		V
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10		
$I_{GSSF}$	Forward-gate current, drain short circuited to source	$V_{GS} = 15 \text{ V}$ ,	$V_{DS} = 0$		20	200	nA
$I_{GSSR}$	Reverse-gate current, drain short circuited to source	$V_{SG} = 5 \text{ V}$ ,	$V_{DS} = 0$		10	100	nA
$I_{lkg}$	Leakage current, drain-to-GND	$V_{DGND} = 48 \text{ V}$	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 1 \text{ A}$ , See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.6	0.65		$\Omega$
			$T_C = 125^\circ\text{C}$	0.85	0.9		
$g_{fs}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ , See Notes 2 and 3 and Figure 9	$I_D = 500 \text{ mA}$ ,	0.89	1.06		S
$C_{iss}$	Short-circuit input capacitance, common source			107	137		pF
$C_{oss}$	Short-circuit output capacitance, common source	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ ,	$V_{GS} = 0$ , See Figure 11	71	89		
$C_{rss}$	Short-circuit reverse transfer capacitance, common source			22	28		

- NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

### source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 500 \text{ mA}$ , $V_{GS} = 0$ , See Figures 1 and 14	$V_{DS} = 48 \text{ V}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , Z1, Z2, and Z3		75		ns
			D1, D2, and D3		190		
$Q_{RR}$	Total diode charge		Z1, Z2, and Z3		0.08		$\mu\text{C}$
			D1, D2, and D3		0.85		



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### resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

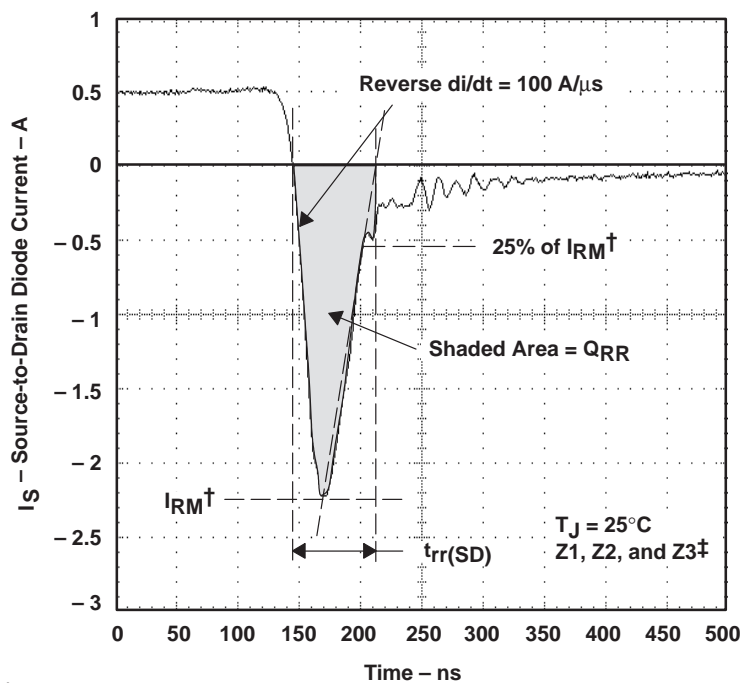
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$ , $R_L = 50\ \Omega$ , $t_{r1} = 10\text{ ns}$ , $t_{f1} = 10\text{ ns}$ , See Figure 2		34	50	ns
$t_{d(off)}$ Turn-off delay time			50	70	
$t_{r2}$ Rise time			20	30	
$t_{f2}$ Fall time			15	25	
$Q_g$ Total gate charge	$V_{DS} = 48\text{ V}$ , $I_D = 500\text{ mA}$ , $V_{GS} = 5\text{ V}$ , See Figure 3		2	2.45	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.3	0.95	
$Q_{gd}$ Gate-to-drain charge			1.2	1.48	
$L_D$ Internal drain inductance			5		nH
$L_S$ Internal source inductance			5		
$R_g$ Internal gate resistance			0.25		$\Omega$

### thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	See Notes 4 and 7		115		$^\circ\text{C/W}$
$R_{\theta JB}$ Junction-to-board thermal resistance	See Notes 5 and 7		64		
$R_{\theta JP}$ Junction-to-pin thermal resistance	See Notes 6 and 7		33		

- NOTES:
- Package mounted on an FR4 printed-circuit board with no heatsink.
  - Package mounted on a 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board.
  - Package mounted in intimate contact with infinite heatsink.
  - All outputs with equal power

### PARAMETER MEASUREMENT INFORMATION



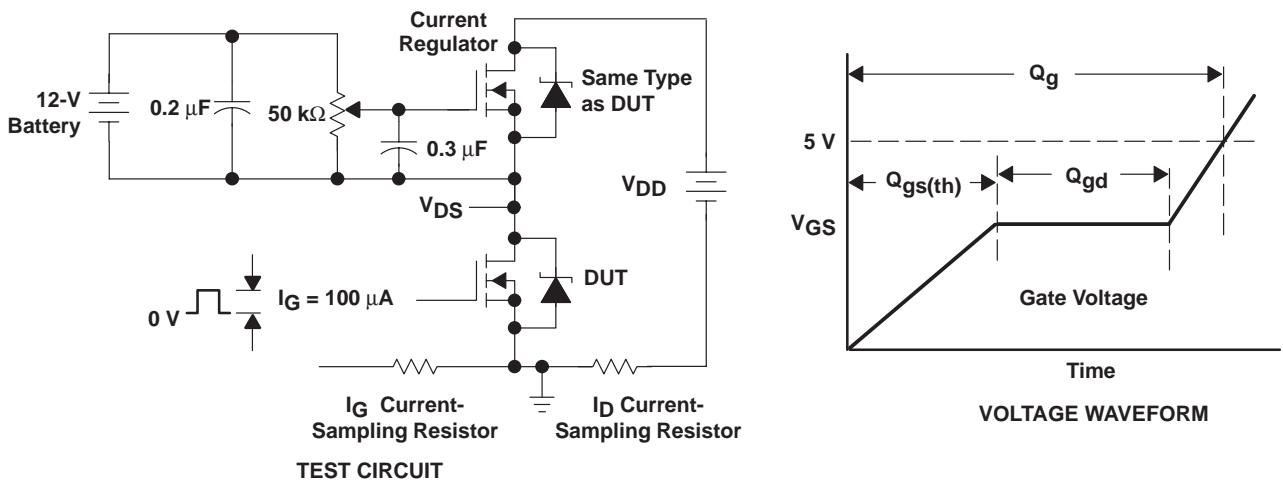
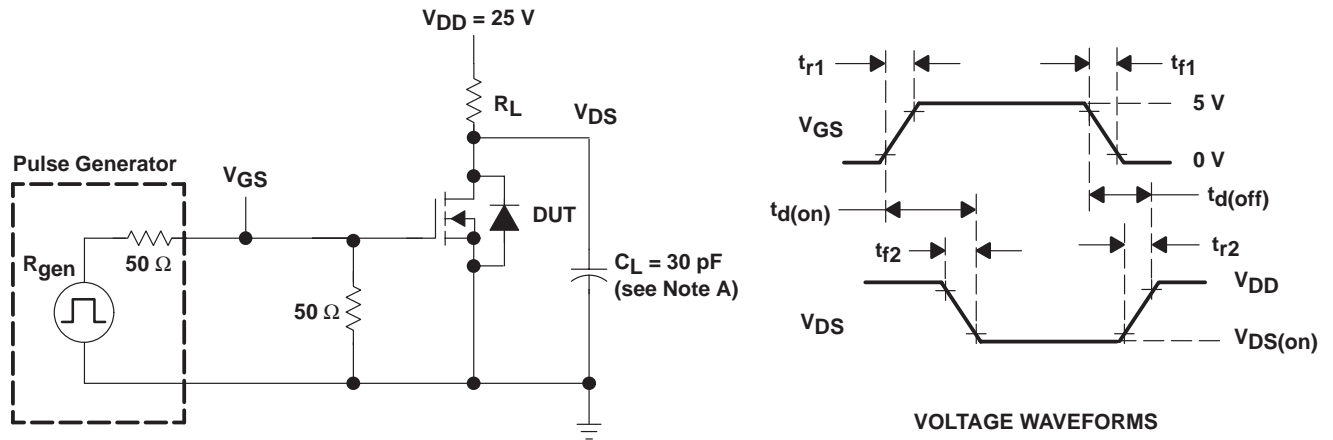
†  $I_{RM}$  = maximum recovery current

‡ The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



PARAMETER MEASUREMENT INFORMATION

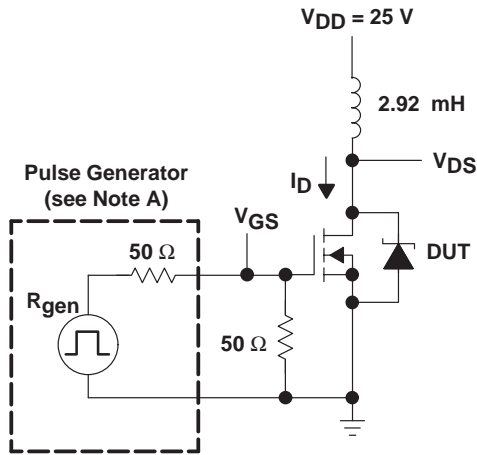


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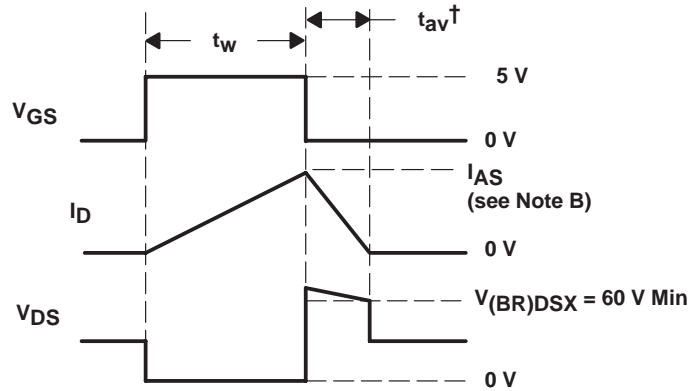
## 3-CHANNEL INDEPENDENT GATE-PROTECTED

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### PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time

NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 3$  A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22.5 \text{ mJ, where } t_{av} = \text{avalanche time.}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

### TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE  
vs  
JUNCTION TEMPERATURE

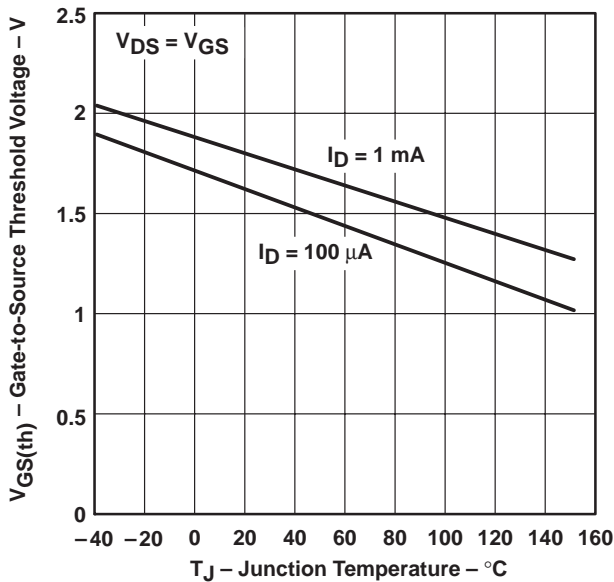


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
JUNCTION TEMPERATURE

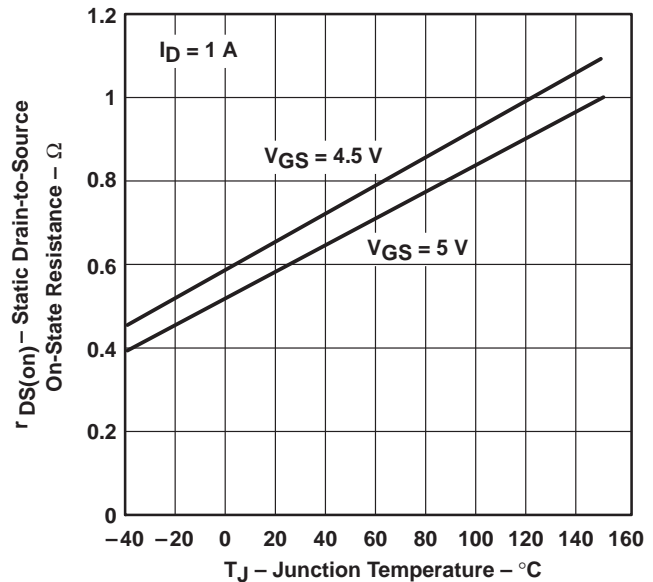


Figure 6



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TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

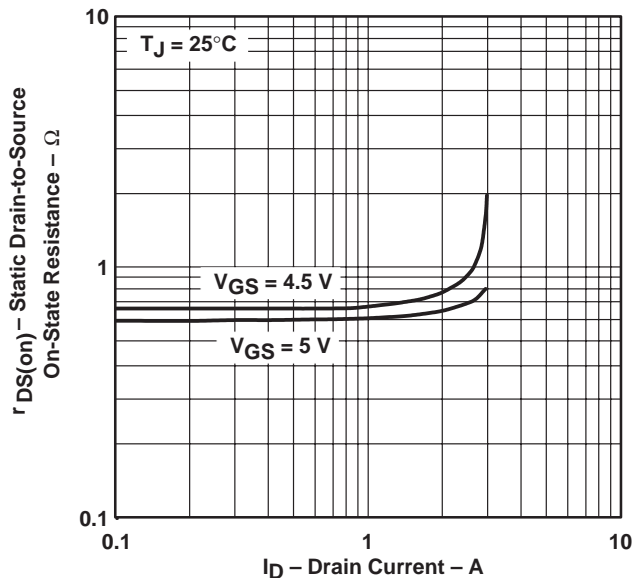


Figure 7

DRAIN CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE

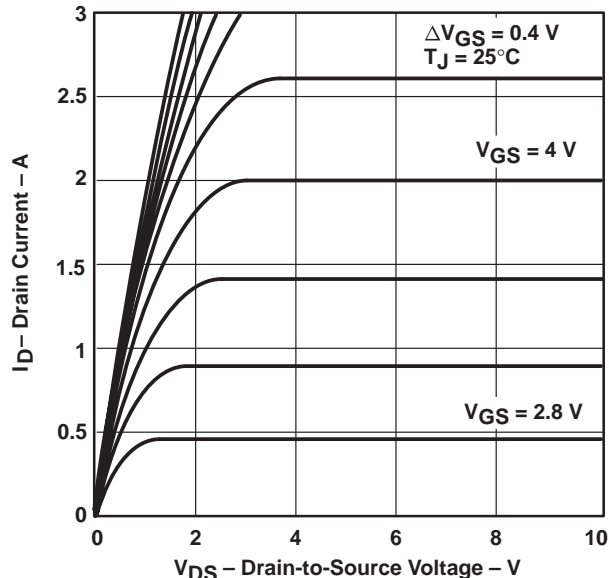


Figure 8

DISTRIBUTION OF  
FORWARD TRANSCONDUCTANCE

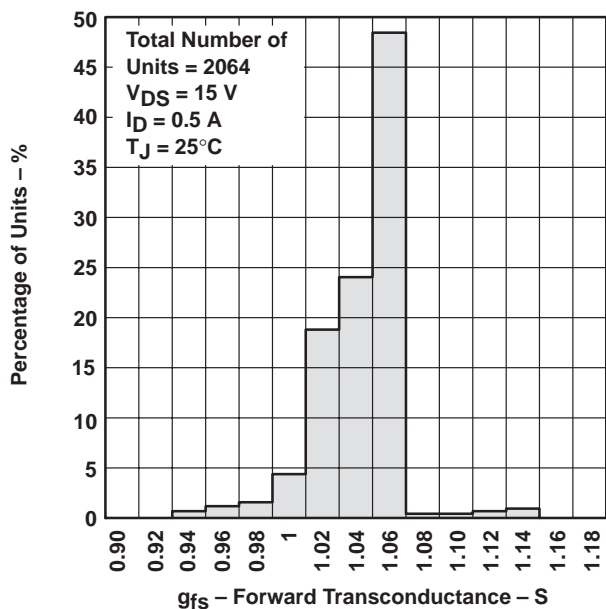


Figure 9

DRAIN CURRENT  
vs  
GATE-TO-SOURCE VOLTAGE

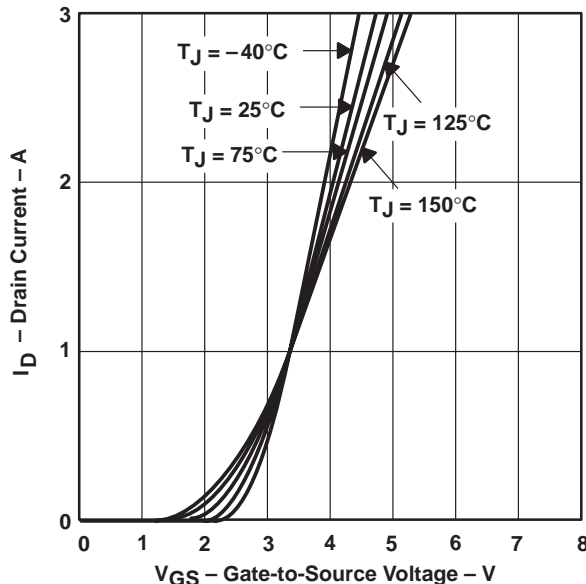


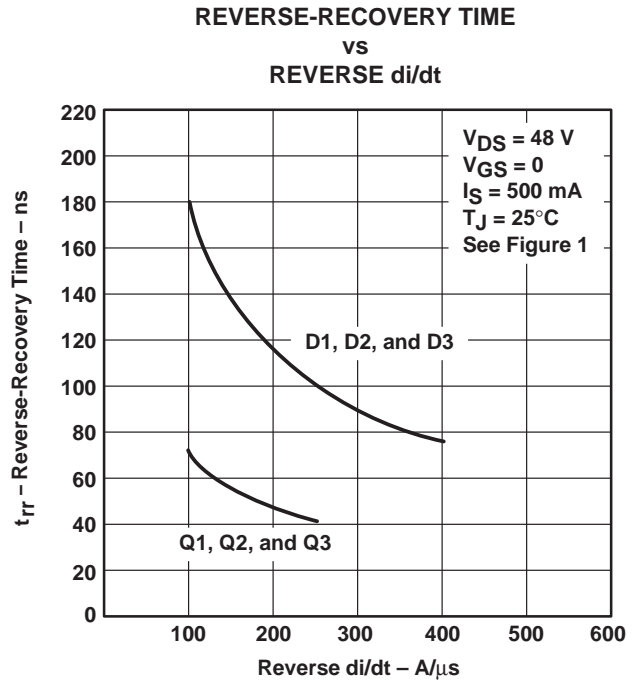
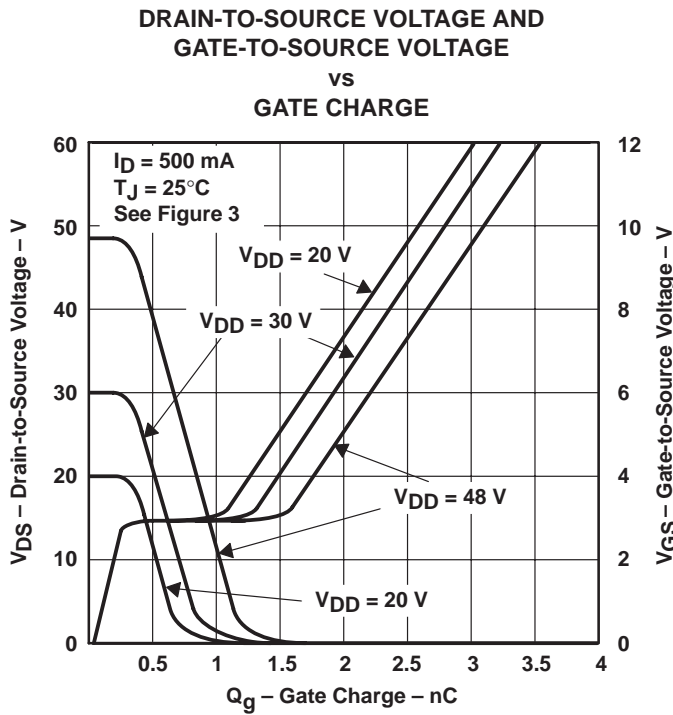
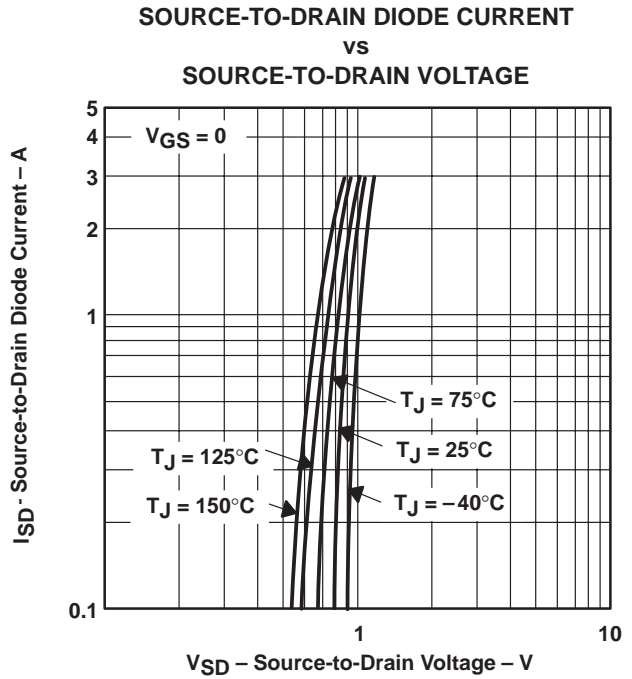
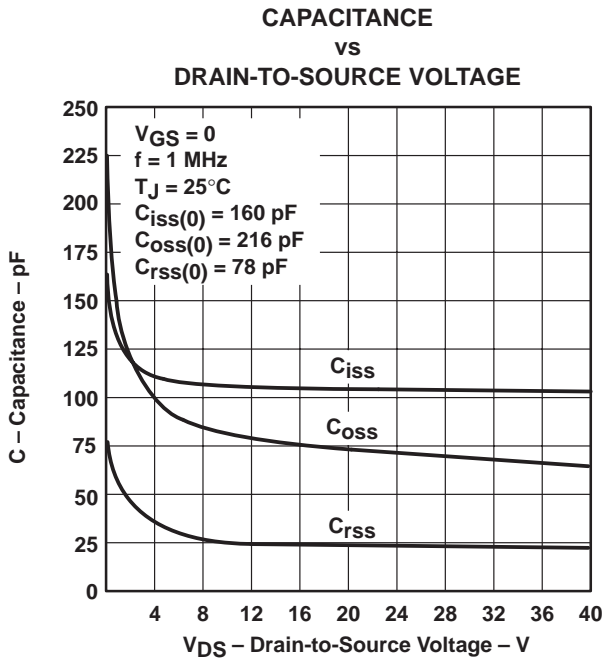
Figure 10

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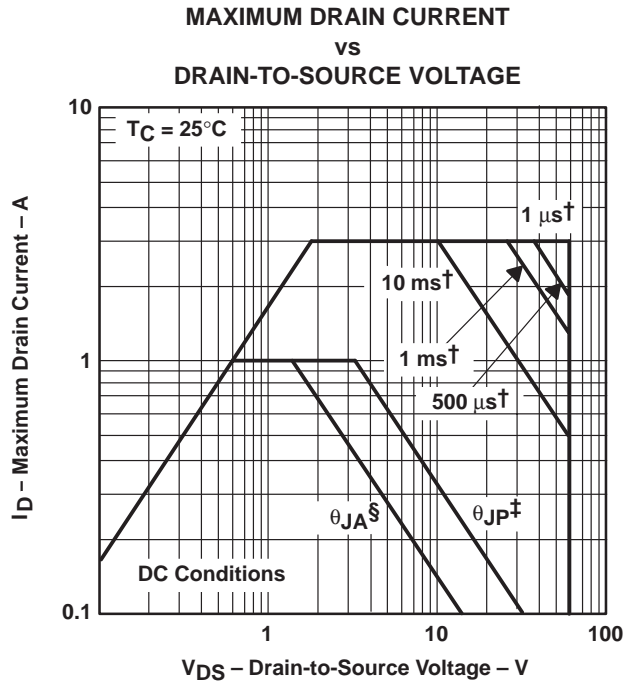
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### TYPICAL CHARACTERISTICS





THERMAL INFORMATION



† Less than 2% duty cycle  
‡ Device mounted in intimate contact with infinite heatsink.  
§ Device mounted on FR4 printed-circuit board with no heatsink.

Figure 15

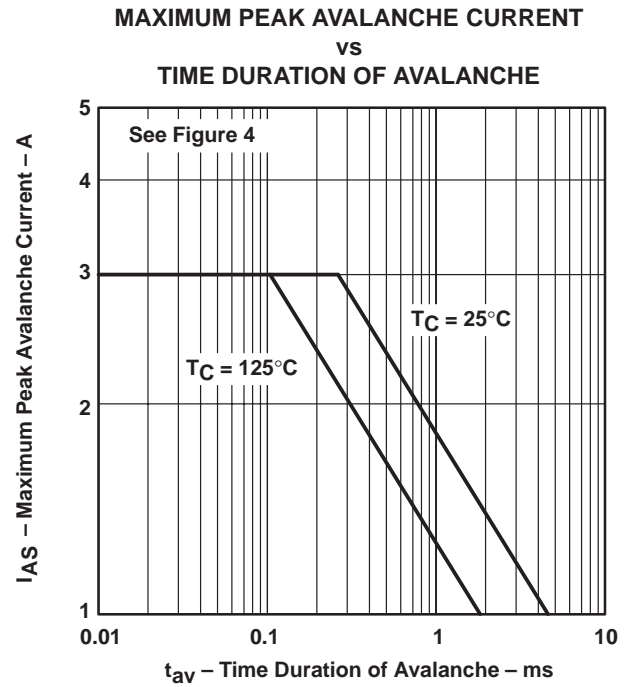


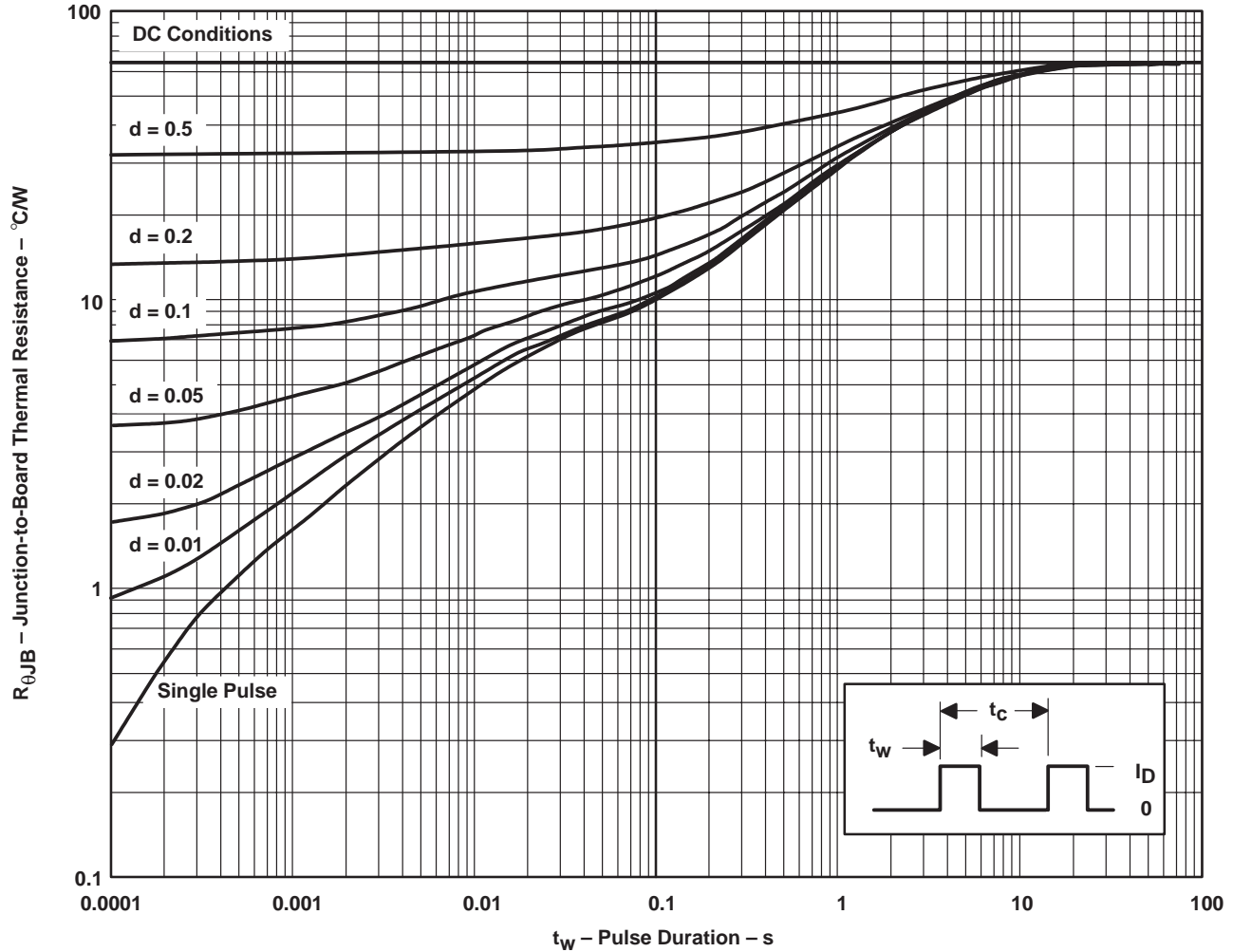
Figure 16

# TPIC5323L 3-CHANNEL INDEPENDENT GATE-PROTECTED

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## THERMAL INFORMATION

### D PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE VS PULSE DURATION



† Device mounted on 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A:  $Z_{\theta B}(t) = r(t) R_{\theta JB}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 17

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC5323LD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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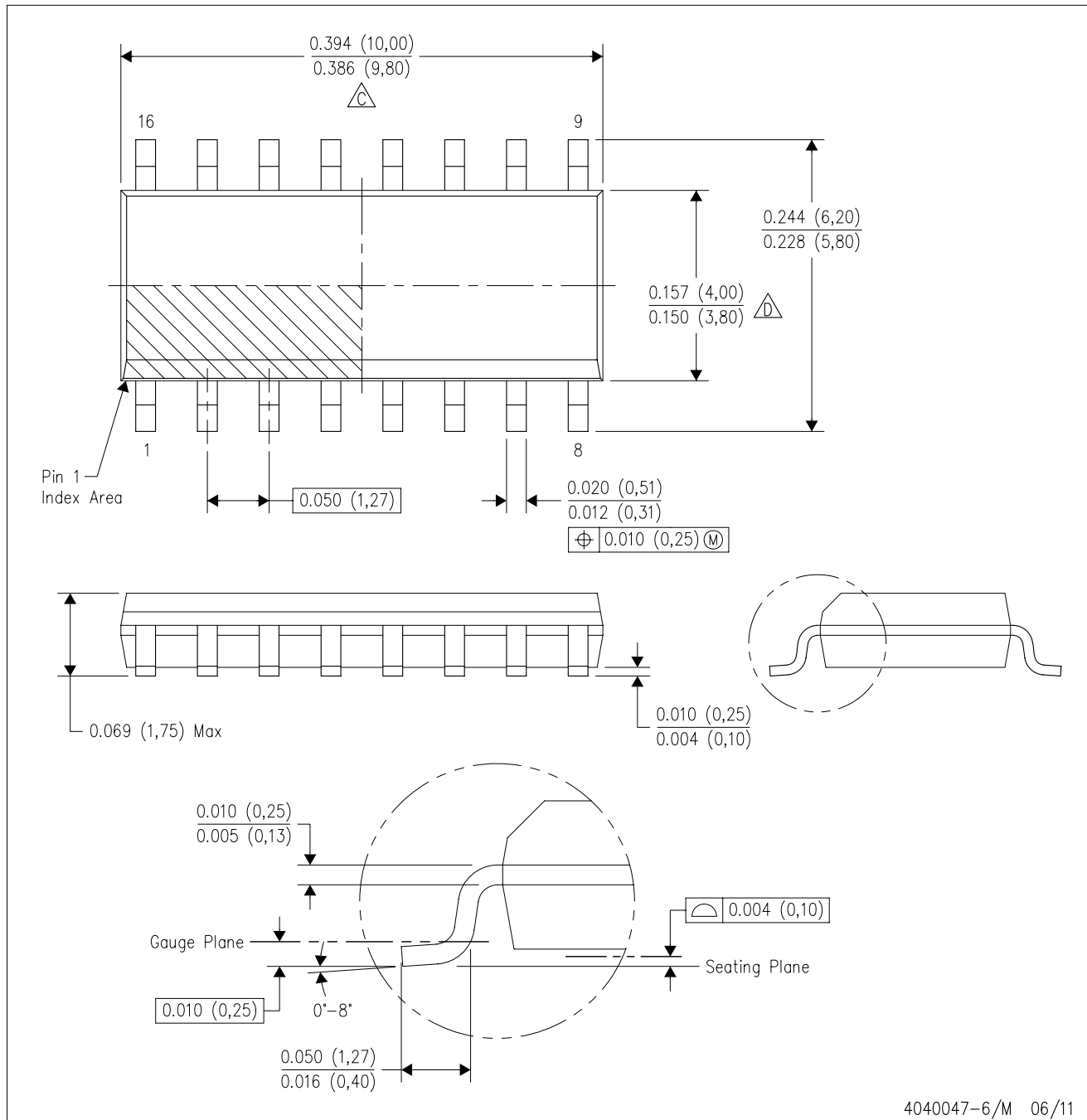
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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