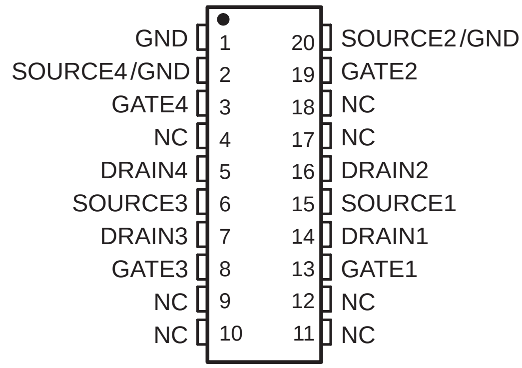
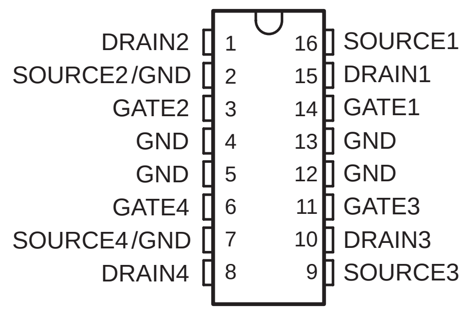
- **Low $r_{DS(on)}$ . . . 0.3 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 10 A Per Channel**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)



NE PACKAGE
(TOP VIEW)



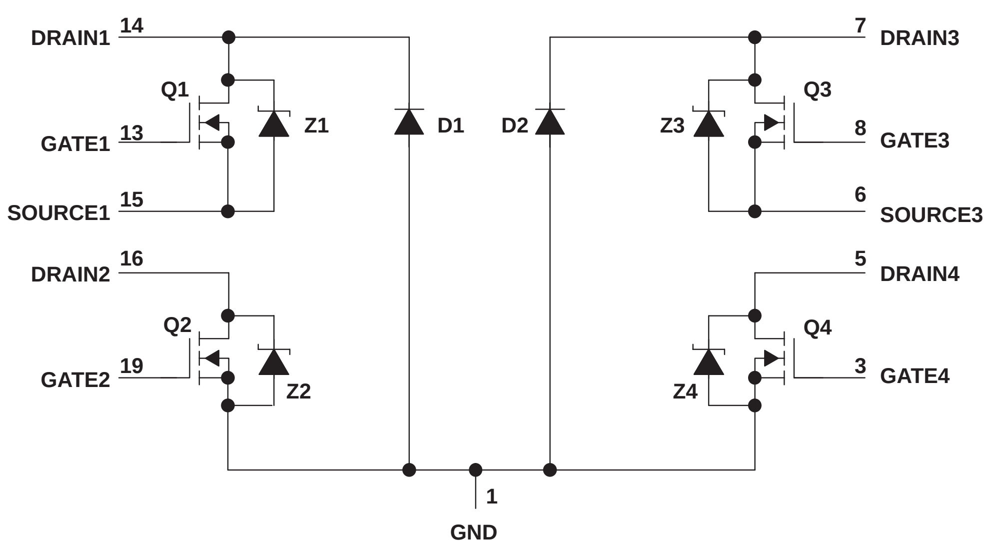
NC − No internal connection

description

The TPIC5404 is a monolithic power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

The TPIC5404 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5404 is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



NOTE A: Pin numbers shown are for the DW package.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	±20
Continuous drain current, each output, T_C = 25°C: DW package	1.7 A
NE package	2 A
Continuous source-to-drain diode current (NE package)	2 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 15)	10 A
Single-pulse avalanche energy, T_C = 25°C (see Figures 4 and 16)	21 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, $V_{DS} = V_{GS}$		1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 2 A, V_{GS} = 10 V, See Notes 2 and 3			0.6	0.7	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 2 A (D1, D2), See Notes 2 and 3			7.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3			1	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_R = 48 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.3	0.35	Ω
			T_C = 125°C		0.41	0.5	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 1 A, See Notes 2 and 3		1.6	1.9		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz			220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤ 5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z1 and Z3), See Figure 1		120		ns
Q_{RR}	Total diode charge			0.12		µC
$t_{rr(SD)}$	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 100 A/µs, (Z2 and Z4), See Figure 1		280		ns
Q_{RR}	Total diode charge			0.9		µC

GND-to-drain diode characteristics, T_C = 25°C (see schematic, D1 and D2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_F = 1 A, V_{DS} = 48 V, di/dt = 100 A/µs, See Figure 1		260		ns
Q_{RR}	Total diode charge			2.2		µC

resistive-load switching characteristics, T_C = 25°C

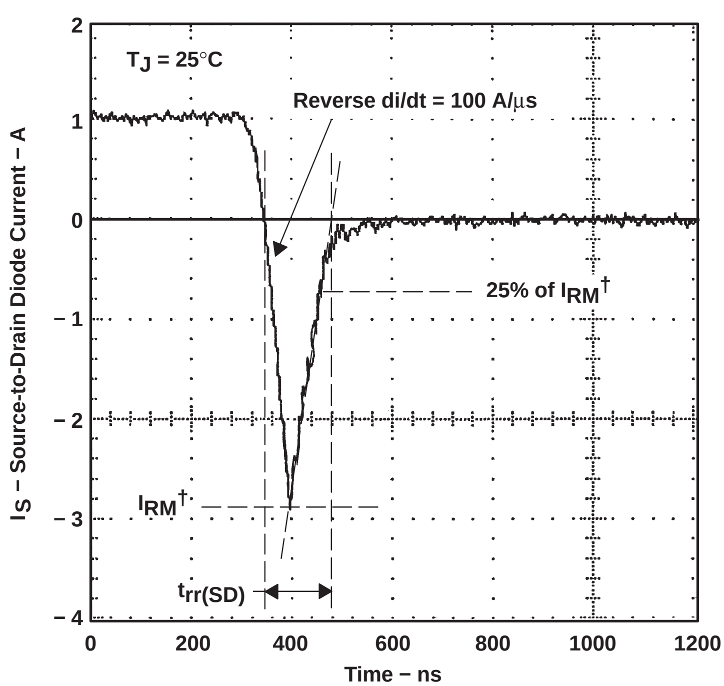
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{r1} = 10 ns, t_{f1} = 10 ns, See Figure 2		32	65	ns
$t_{d(off)}$	Turn-off delay time			40	80	
t_{r2}	Rise time			15	30	
t_{f2}	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		6.6	8	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.8	1	
Q_{gd}	Gate-to-drain charge			2.6	3.2	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	All outputs with equal power, See Note 4		90		°C/W
		NE package			60		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package			30		°C/W
		NE package			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION

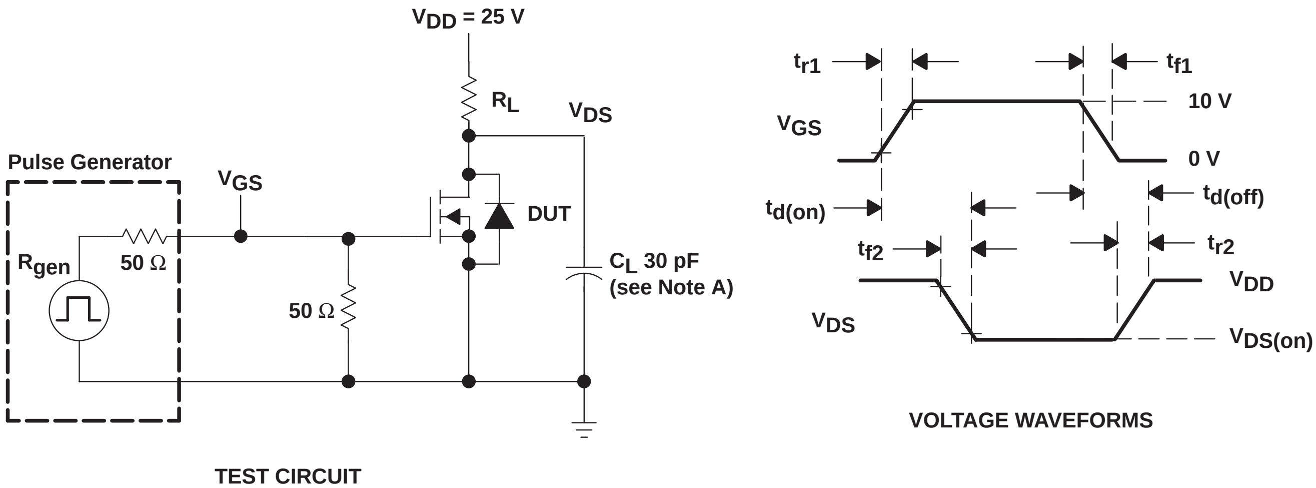


† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

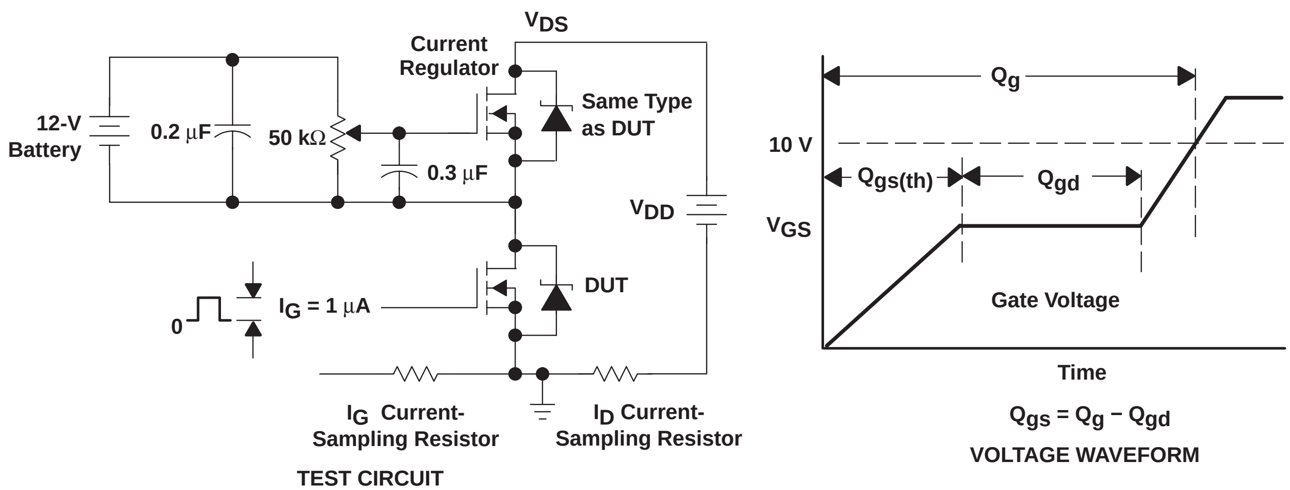
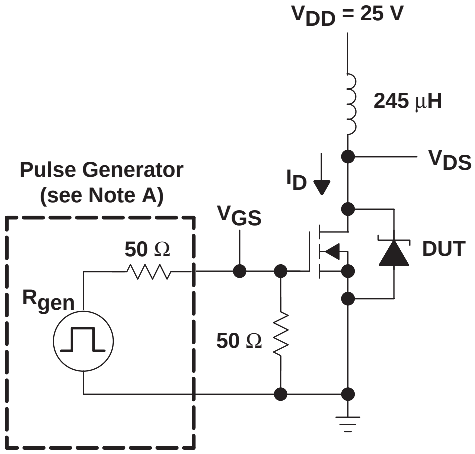
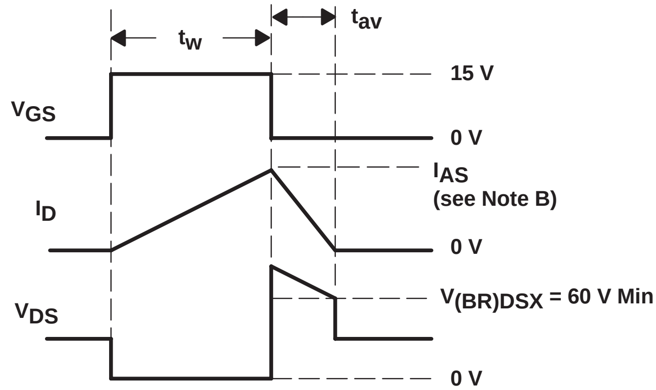


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 10$ A, where t_{av} = avalanche time.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21$ mJ

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

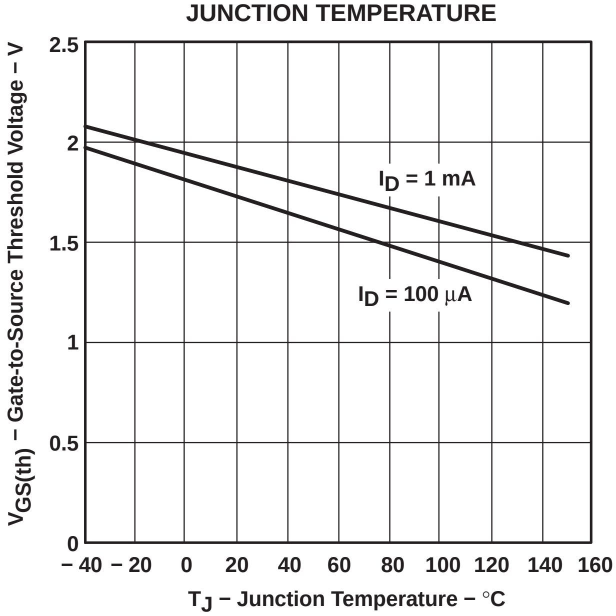


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

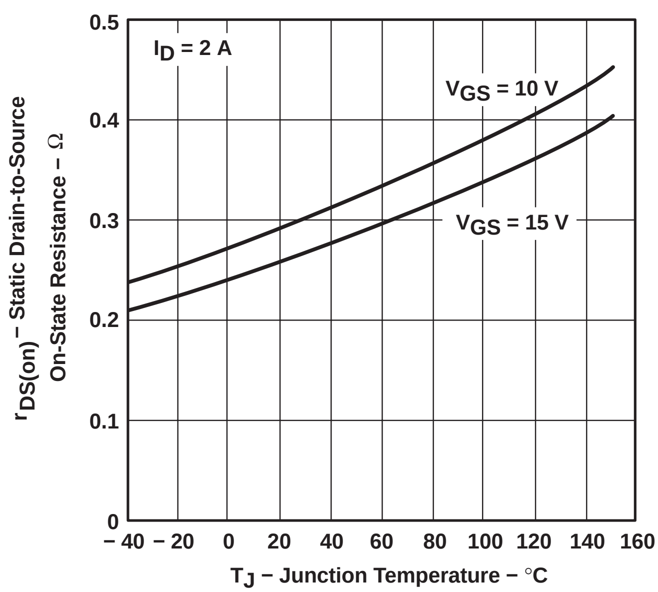


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

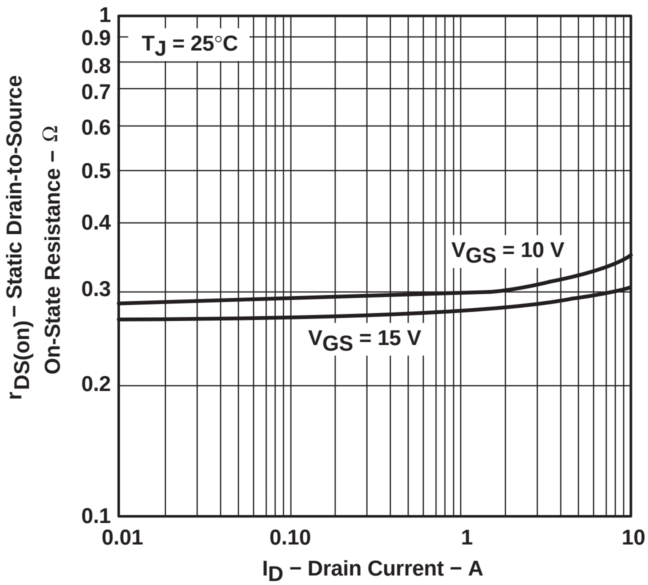


Figure 7

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

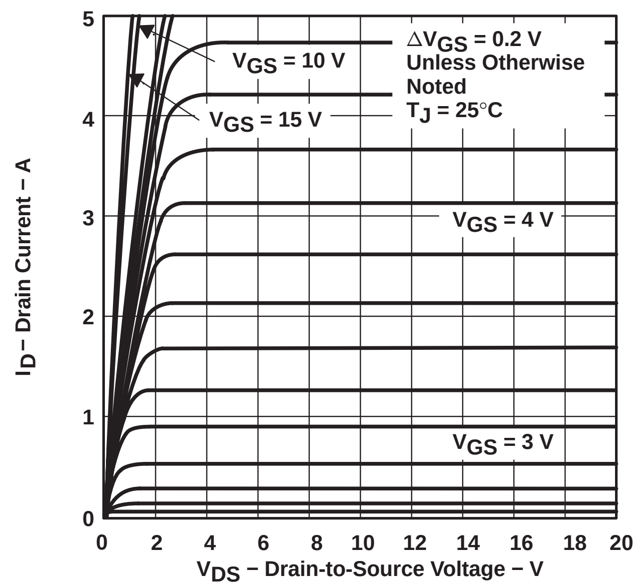


Figure 8

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

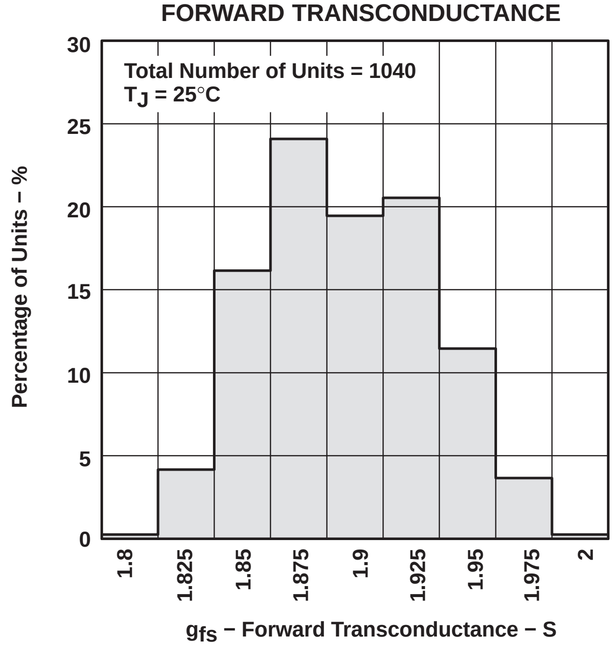


Figure 9

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

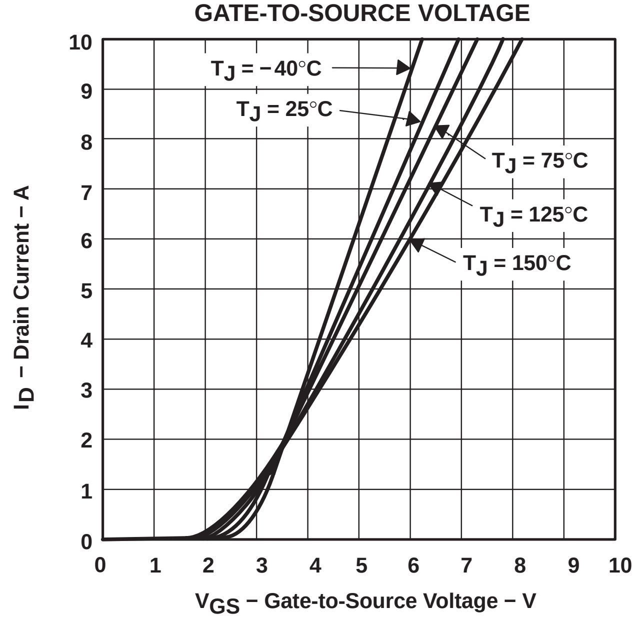


Figure 10

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

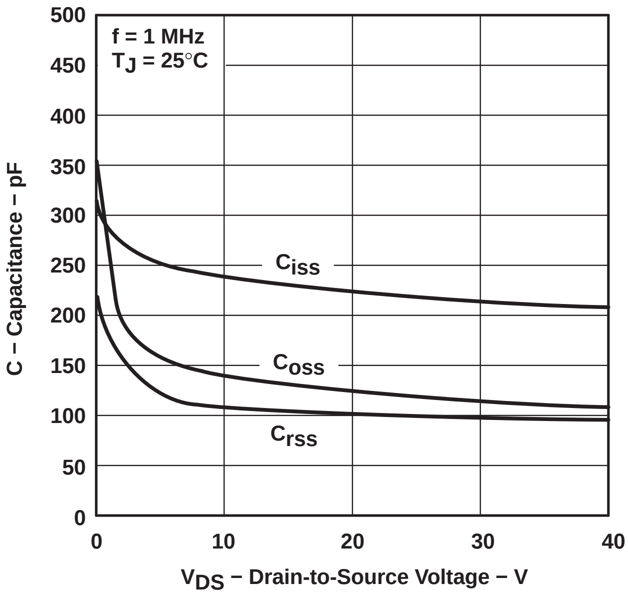


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

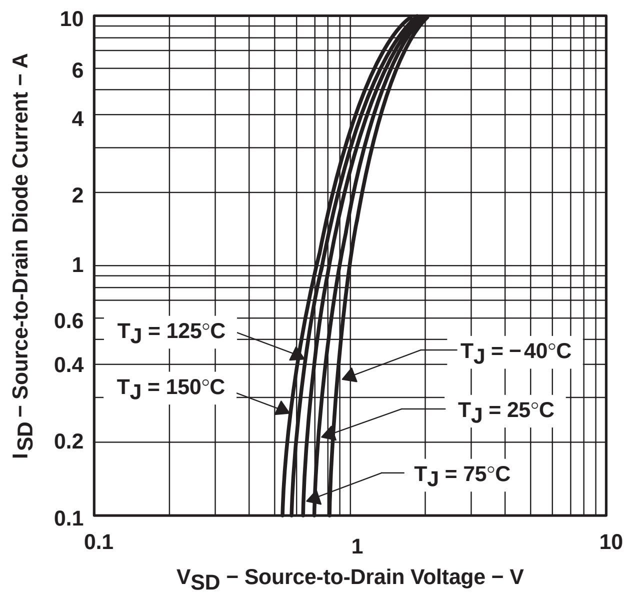


Figure 12

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

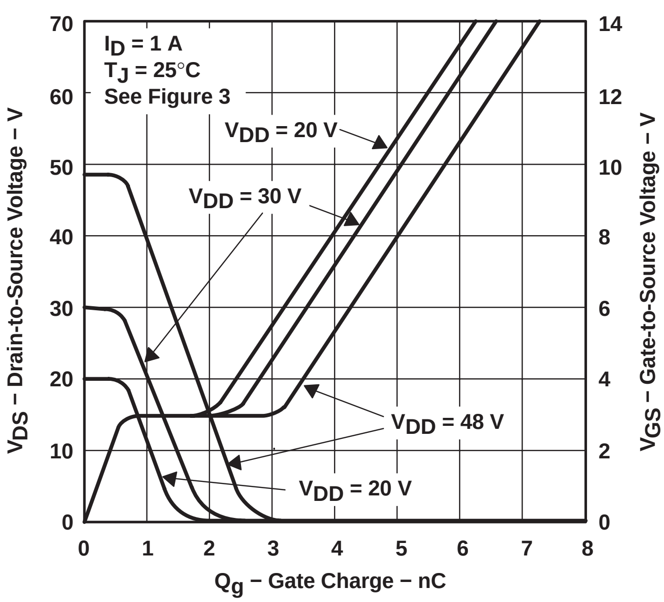


Figure 13

REVERSE-RECOVERY TIME vs REVERSE di/dt

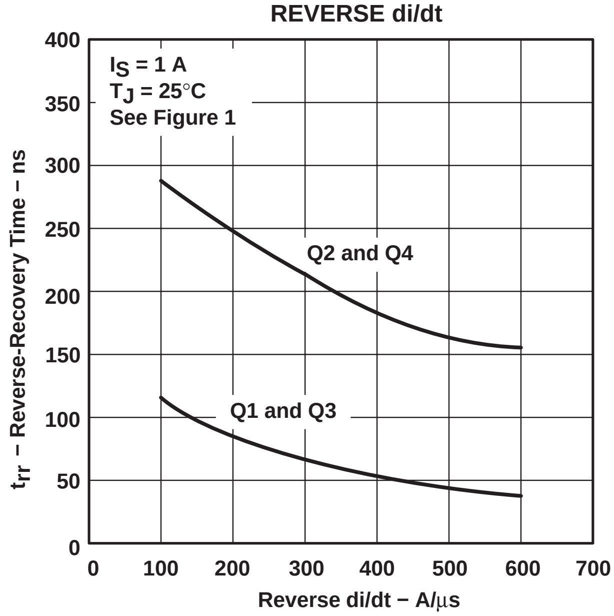
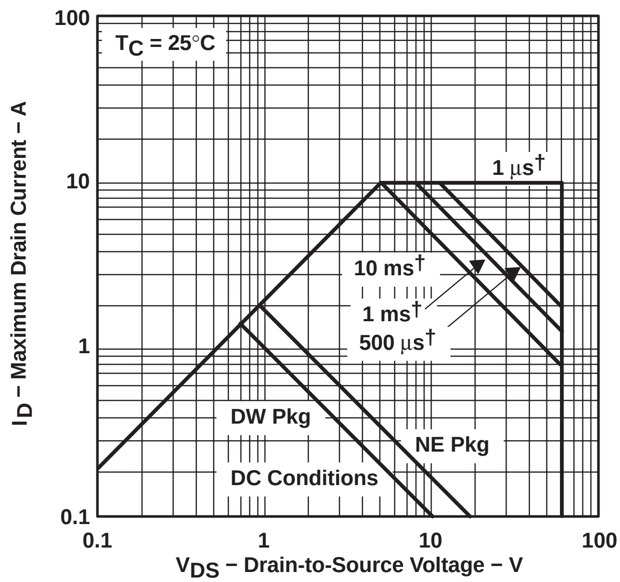


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

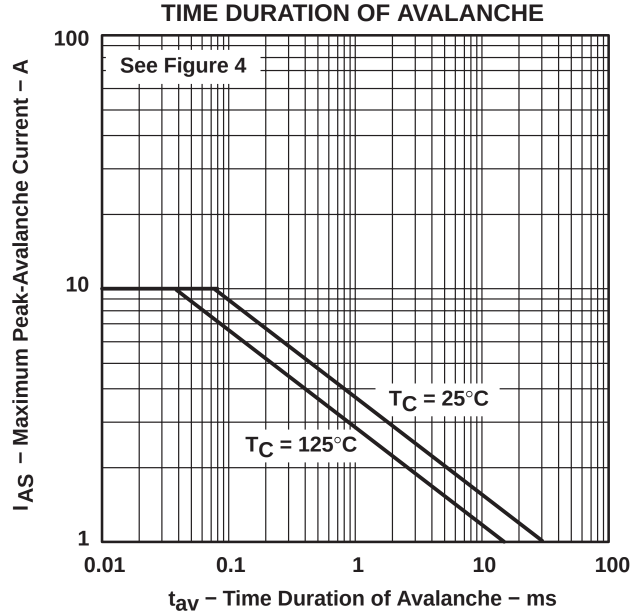
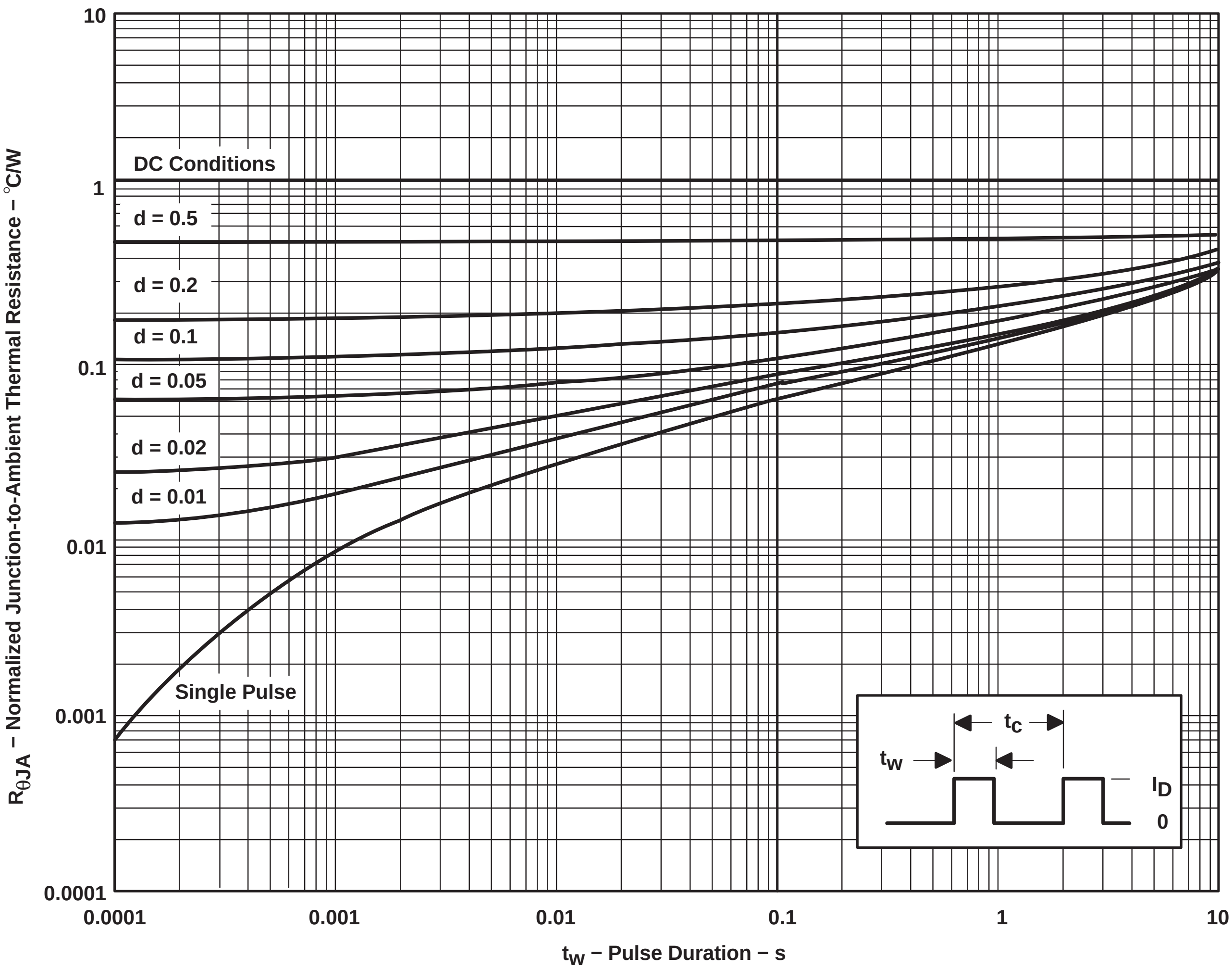


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



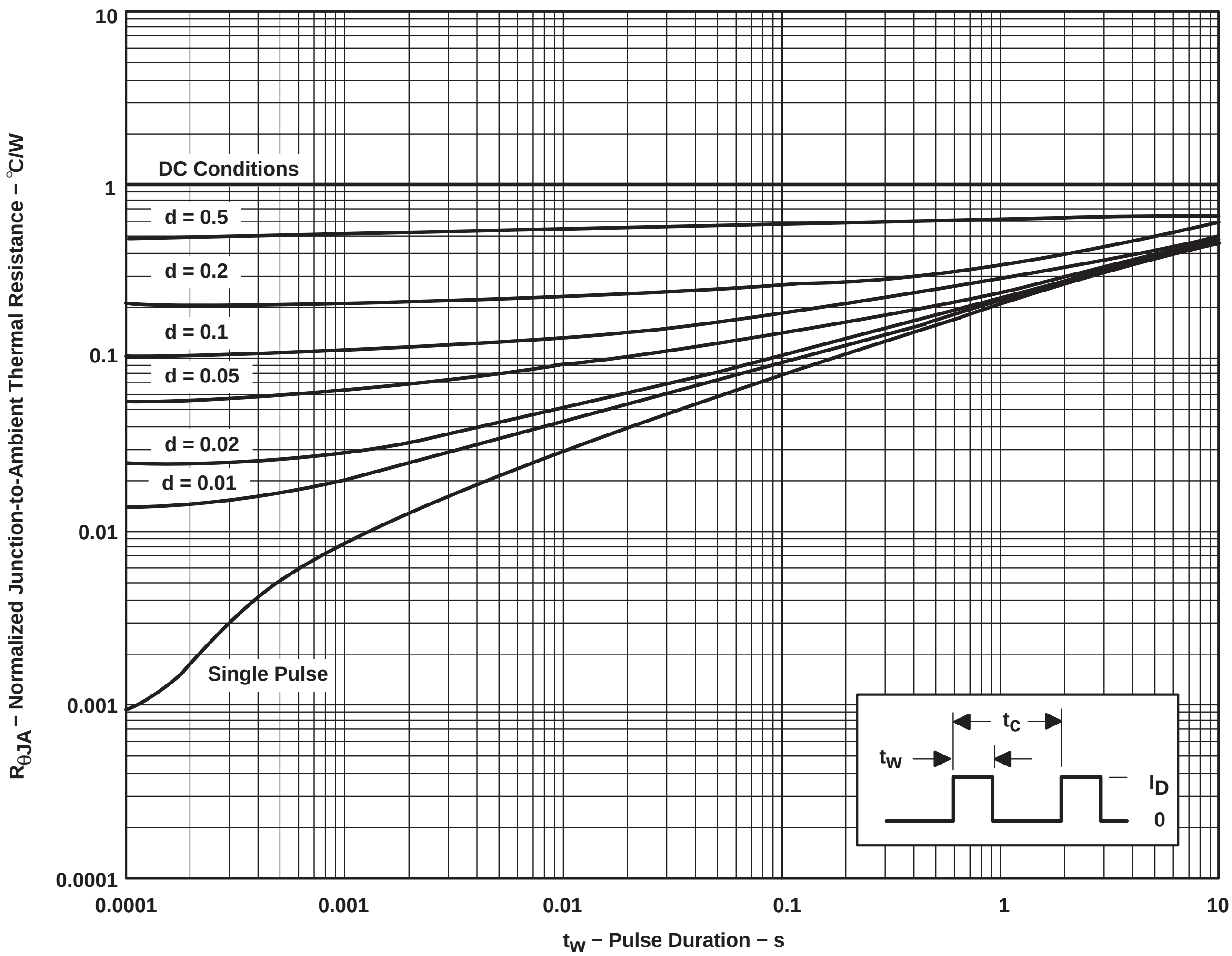
† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\,R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPIC5404DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
TPIC5404NE	OBSOLETE	PDIP	NE	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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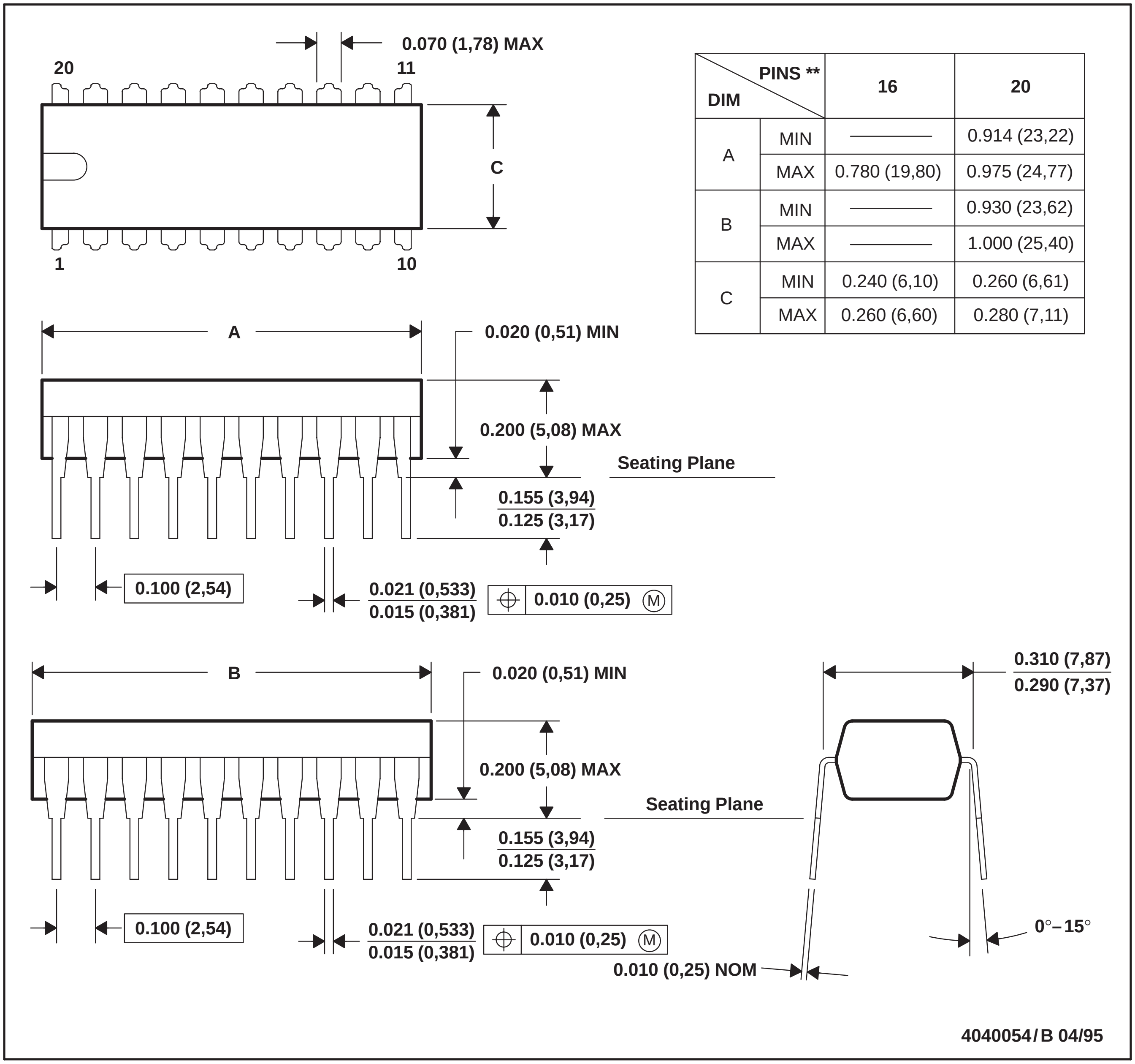
NE (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

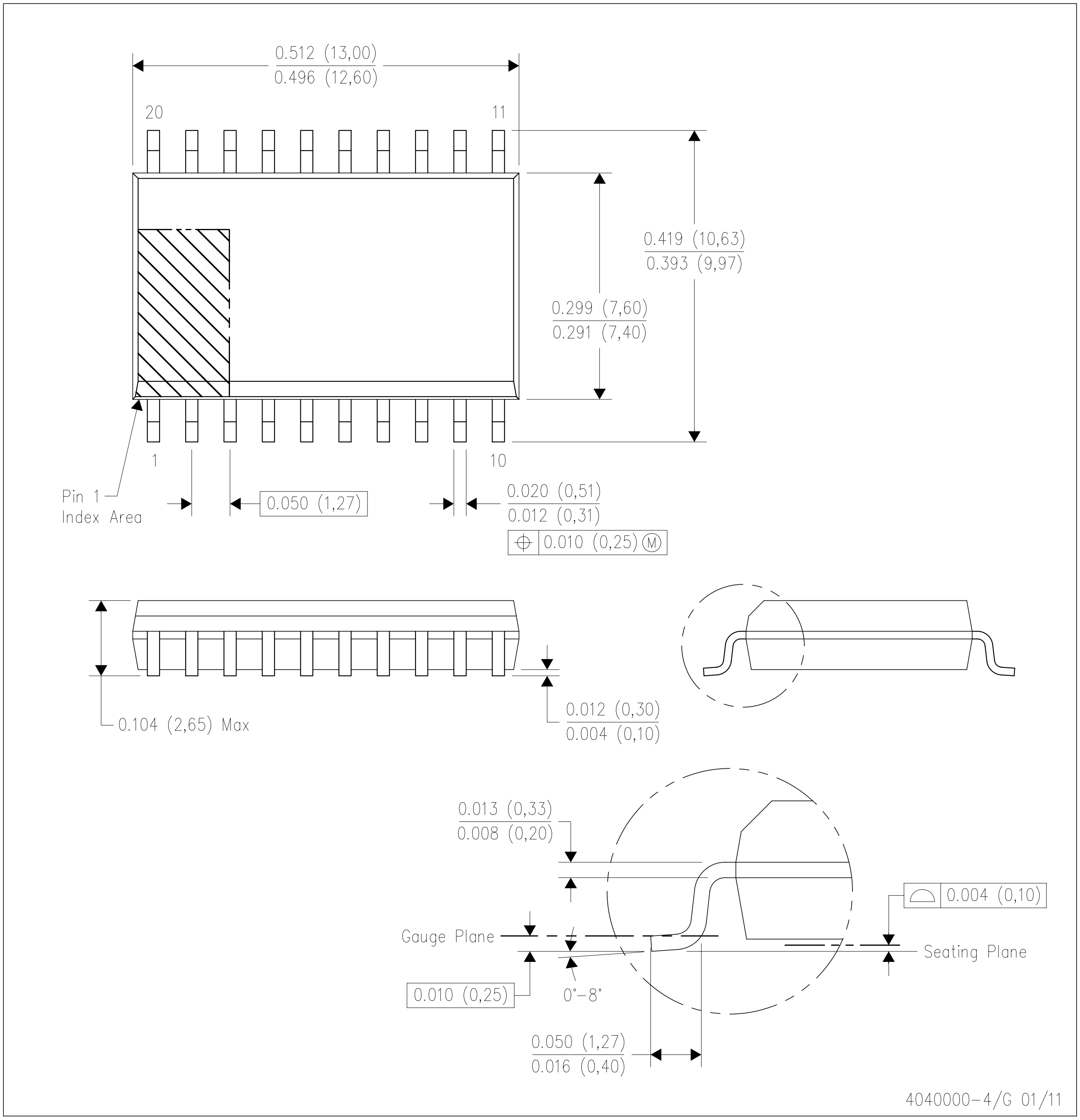
20 PIN SHOWN



DIM \ PINS **		16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.