

# TPIC5404 H-BRIDGE POWER DMOS ARRAY

SLIS023B – MARCH 1994 – REVISED SEPTEMBER 1995

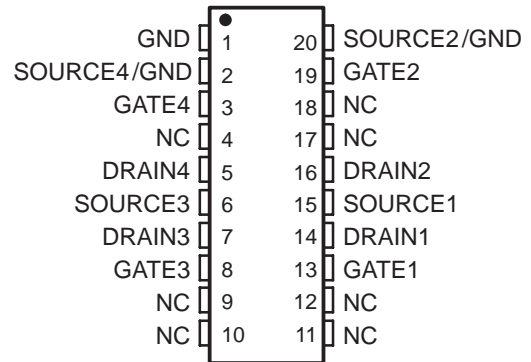
- Low  $r_{DS(on)}$  . . . 0.3  $\Omega$  Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 10 A Per Channel
- Fast Commutation Speed

## description

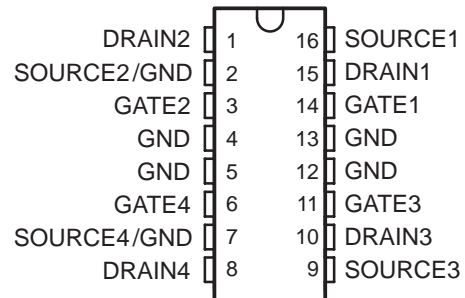
The TPIC5404 is a monolithic power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

The TPIC5404 is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5404 is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

DW PACKAGE  
(TOP VIEW)

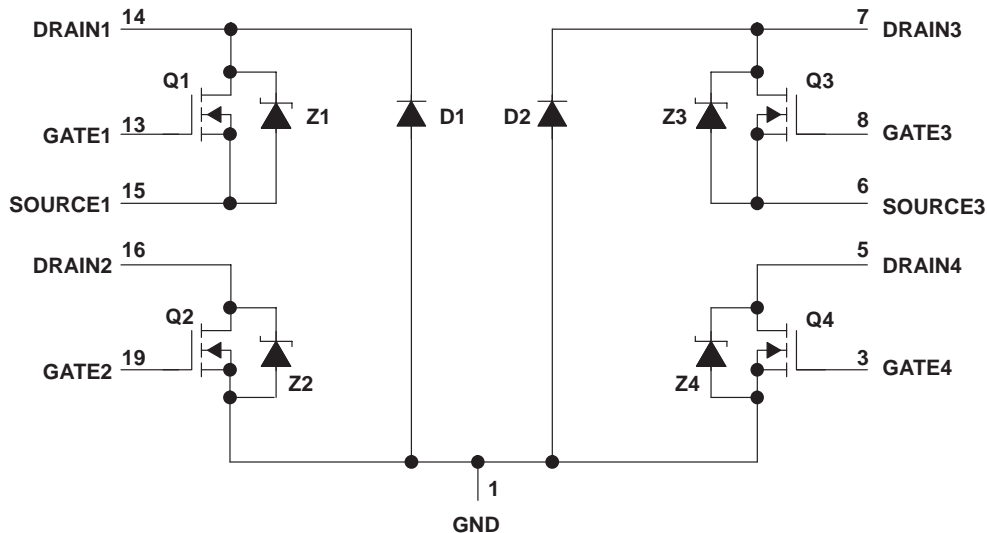


NE PACKAGE  
(TOP VIEW)



NC – No internal connection

## schematic



NOTE A: Pin numbers shown are for the DW package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# TPIC5404

## H-BRIDGE POWER DMOS ARRAY

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### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

|  |  |
|--|--|
| Drain-to-source voltage, $V_{DS}$ .....  | 60 V                                       |
| Source-to-GND voltage (Q1, Q3) .....   | 100 V                                      |
| Drain-to-GND voltage (Q1, Q3) .....  | 100 V                                      |
| Drain-to-GND voltage (Q2, Q4) .....  | 60 V                                       |
| Gate-to-source voltage range, $V_{GS}$ .....   | $\pm 20$                                   |
| Continuous drain current, each output, $T_C = 25^\circ\text{C}$ : DW package .....           | 1.7 A                                      |
| NE package .....   | 2 A  |
| Continuous source-to-drain diode current (NE package) .....                                  | 2 A  |
| Pulsed drain current, each output, $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15) ..... | 10 A                                       |
| Single-pulse avalanche energy, $T_C = 25^\circ\text{C}$ (see Figures 4 and 16) .....         | 21 mJ                                      |
| Continuous total power dissipation .....   | See Dissipation Rating Table               |
| Operating virtual junction temperature range, $T_J$ .....                                    | $-40^\circ\text{C}$ to $150^\circ\text{C}$ |
| Operating case temperature range, $T_C$ .....  | $-40^\circ\text{C}$ to $125^\circ\text{C}$ |
| Storage temperature range, $T_{stg}$ .....   | $-65^\circ\text{C}$ to $150^\circ\text{C}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....                           | $260^\circ\text{C}$                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

| PACKAGE | $T_C \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$<br>POWER RATING |
|---------|---|---|---|
| DW      | 1389 mW                                     | 11.1 mW/ $^\circ\text{C}$                         | 279 mW                                    |
| NE      | 2075 mW                                     | 16.6 mW/ $^\circ\text{C}$                         | 415 mW                                    |

**electrical characteristics,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

| PARAMETER     |   | TEST CONDITIONS  | MIN                       | TYP  | MAX  | UNIT          |
|---------------|---|--|---------------------------|------|------|---------------|
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage                         | $I_D = 250 \mu\text{A}$ , $V_{GS} = 0$   | 60                        |      |      | V             |
| $V_{GS(th)}$  | Gate-to-source threshold voltage                          | $I_D = 1 \text{ mA}$ , $V_{DS} = V_{GS}$   | 1.5                       | 1.85 | 2.2  | V             |
| $V_{(BR)}$    | Reverse drain-to-GND breakdown voltage (across D1, D2)    | Drain-to-GND current = $250 \mu\text{A}$   | 100                       |      |      | V             |
| $V_{DS(on)}$  | Drain-to-source on-state voltage                          | $I_D = 2 \text{ A}$ ,<br>See Notes 2 and 3 $V_{GS} = 10 \text{ V}$ ,                           |                           | 0.6  | 0.7  | V             |
| $V_F$         | Forward on-state voltage, GND-to-drain                    | $I_D = 2 \text{ A}$ (D1, D2),<br>See Notes 2 and 3   |                           | 7.5  |      | V             |
| $V_{F(SD)}$   | Forward on-state voltage, source-to-drain                 | $I_S = 2 \text{ A}$ ,<br>$V_{GS} = 0$ (Z1, Z2, Z3, Z4),<br>See Notes 2 and 3                   |                           | 1    | 1.2  | V             |
| $I_{DSS}$     | Zero-gate-voltage drain current                           | $V_{DS} = 48 \text{ V}$ ,<br>$V_{GS} = 0$  | $T_C = 25^\circ\text{C}$  | 0.05 | 1    | $\mu\text{A}$ |
|               |   |  | $T_C = 125^\circ\text{C}$ | 0.5  | 10   |               |
| $I_{GSSF}$    | Forward gate current, drain short circuited to source     | $V_{GS} = 16 \text{ V}$ , $V_{DS} = 0$   |                           | 10   | 100  | nA            |
| $I_{GSSR}$    | Reverse gate current, drain short circuited to source     | $V_{SG} = 16 \text{ V}$ , $V_{DS} = 0$   |                           | 10   | 100  | nA            |
| $I_{lkg}$     | Leakage current, drain-to-GND                             | $V_R = 48 \text{ V}$   | $T_C = 25^\circ\text{C}$  | 0.05 | 1    | $\mu\text{A}$ |
|               |   |  | $T_C = 125^\circ\text{C}$ | 0.5  | 10   |               |
| $r_{DS(on)}$  | Static drain-to-source on-state resistance                | $V_{GS} = 10 \text{ V}$ ,<br>$I_D = 2 \text{ A}$ ,<br>See Notes 2 and 3<br>and Figures 6 and 7 | $T_C = 25^\circ\text{C}$  | 0.3  | 0.35 | $\Omega$      |
|               |   |  | $T_C = 125^\circ\text{C}$ | 0.41 | 0.5  |               |
| $g_{fs}$      | Forward transconductance                                  | $V_{DS} = 15 \text{ V}$ ,<br>See Notes 2 and 3 $I_D = 1 \text{ A}$ ,                           | 1.6                       | 1.9  |      | S             |
| $C_{iss}$     | Short-circuit input capacitance, common source            | $V_{DS} = 25 \text{ V}$ ,<br>$f = 1 \text{ MHz}$ $V_{GS} = 0$ ,                                |                           | 220  | 275  | pF            |
| $C_{oss}$     | Short-circuit output capacitance, common source           |  |                           | 120  | 150  |               |
| $C_{rss}$     | Short-circuit reverse-transfer capacitance, common source |  |                           | 100  | 125  |               |

- NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum, pulse duration  $\leq 5 \text{ ms}$ .  
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

**source-to-drain diode characteristics,  $T_C = 25^\circ\text{C}$**

| PARAMETER    |                       | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT          |
|--------------|-----------------------|--|-----|------|-----|---------------|
| $t_{rr(SD)}$ | Reverse-recovery time | $I_S = 1 \text{ A}$ , $V_{GS} = 0$ , $V_{DS} = 48 \text{ V}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>See Figure 1 (Z1 and Z3), |     | 120  |     | ns            |
| $Q_{RR}$     | Total diode charge    |  |     | 0.12 |     | $\mu\text{C}$ |
| $t_{rr(SD)}$ | Reverse-recovery time | $I_S = 1 \text{ A}$ , $V_{GS} = 0$ , $V_{DS} = 48 \text{ V}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>See Figure 1 (Z2 and Z4), |     | 280  |     | ns            |
| $Q_{RR}$     | Total diode charge    |  |     | 0.9  |     | $\mu\text{C}$ |

**GND-to-drain diode characteristics,  $T_C = 25^\circ\text{C}$  (see schematic, D1 and D2)**

| PARAMETER |                       | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|-----------|-----------------------|--|-----|-----|-----|---------------|
| $t_{rr}$  | Reverse-recovery time | $I_F = 1 \text{ A}$ , $V_{DS} = 48 \text{ V}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>See Figure 1 |     | 260 |     | ns            |
| $Q_{RR}$  | Total diode charge    |  |     | 2.2 |     | $\mu\text{C}$ |



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## resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

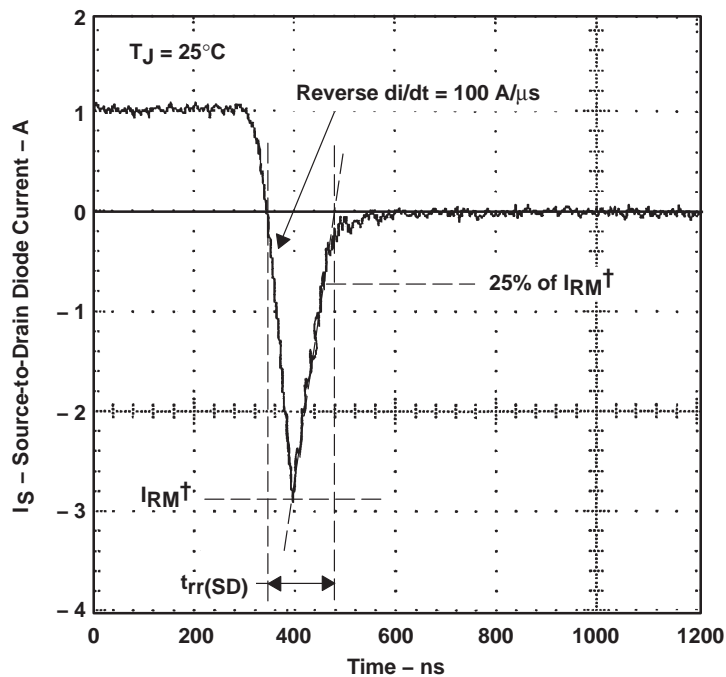
| PARAMETER    |                                 | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT     |
|--------------|---------------------------------|--|-----|------|-----|----------|
| $t_{d(on)}$  | Turn-on delay time              | $V_{DD} = 25\text{ V},$<br>$R_L = 25\ \Omega,$<br>$t_{r1} = 10\text{ ns},$<br>See Figure 2 |     | 32   | 65  | ns       |
| $t_{d(off)}$ | Turn-off delay time             |  |     | 40   | 80  |          |
| $t_{r2}$     | Rise time                       |  |     | 15   | 30  |          |
| $t_{f2}$     | Fall time                       |  |     | 25   | 50  |          |
| $Q_g$        | Total gate charge               | $V_{DS} = 48\text{ V},$<br>See Figure 3<br>$I_D = 1\text{ A},$<br>$V_{GS} = 10\text{ V},$  |     | 6.6  | 8   | nC       |
| $Q_{gs(th)}$ | Threshold gate-to-source charge |  |     | 0.8  | 1   |          |
| $Q_{gd}$     | Gate-to-drain charge            |  |     | 2.6  | 3.2 |          |
| $L_D$        | Internal drain inductance       |  |     | 5    |     | nH       |
| $L_S$        | Internal source inductance      |  |     | 5    |     |          |
| $R_g$        | Internal gate resistance        |  |     | 0.25 |     | $\Omega$ |

## thermal resistance

| PARAMETER       |  | TEST CONDITIONS | MIN | TYP | MAX | UNIT               |
|-----------------|--|-----------------|-----|-----|-----|--------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | DW package      |     | 90  |     | $^\circ\text{C/W}$ |
|                 |  | NE package      |     | 60  |     |                    |
| $R_{\theta JP}$ | Junction-to-pin thermal resistance     | DW package      |     | 30  |     | $^\circ\text{C/W}$ |
|                 |  | NE package      |     | 25  |     |                    |

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

## PARAMETER MEASUREMENT INFORMATION

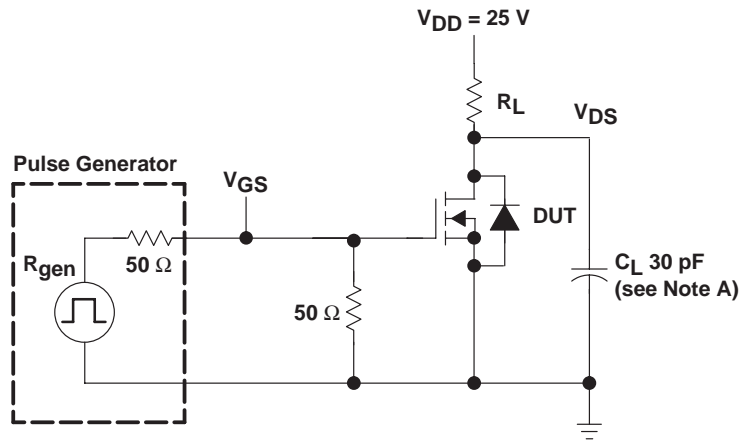


†  $I_{RM}$  = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

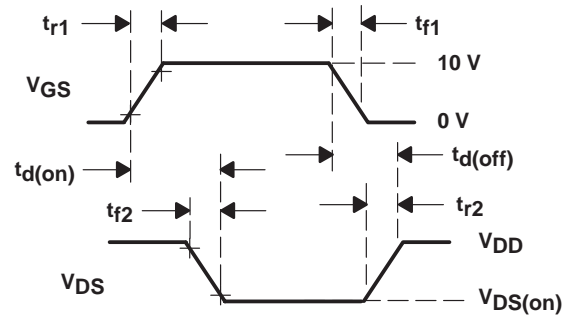


PARAMETER MEASUREMENT INFORMATION



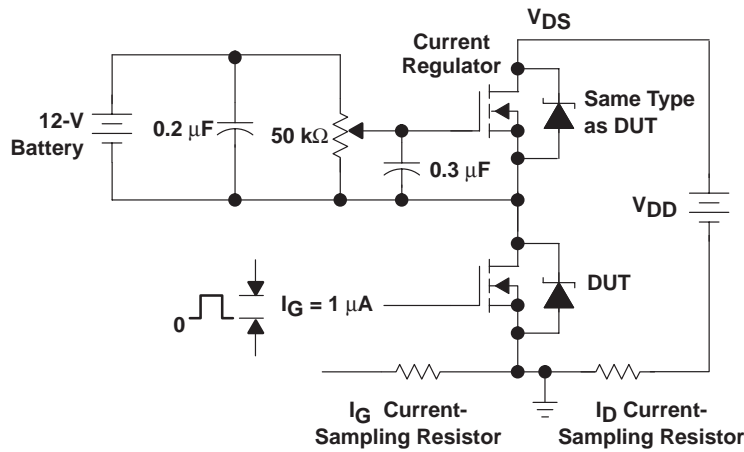
TEST CIRCUIT

NOTE A:  $C_L$  includes probe and jig capacitance.

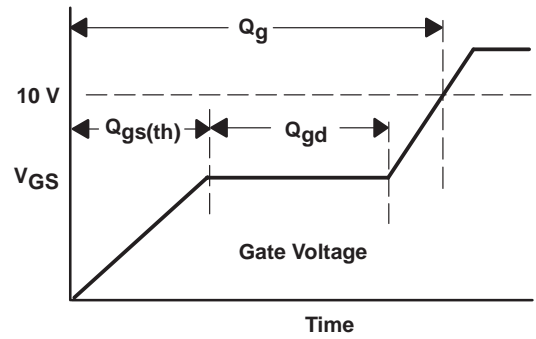


VOLTAGE WAVEFORMS

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT



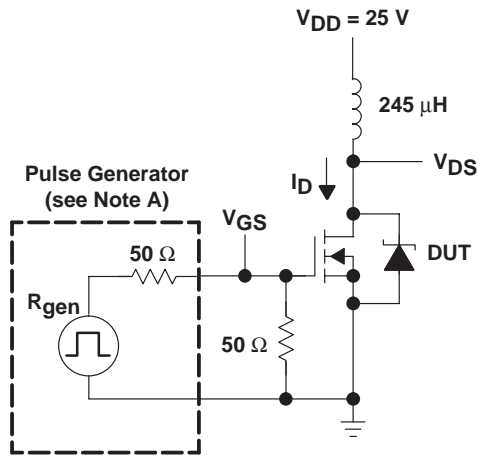
$Q_{gs} = Q_g - Q_{gd}$   
VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

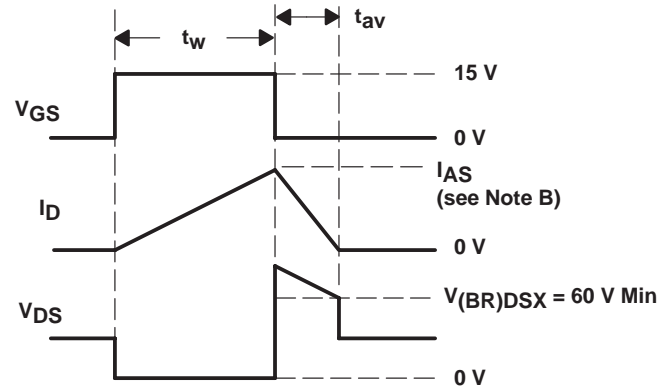
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## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 10$  A, where  $t_{av}$  = avalanche time.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 21 \text{ mJ}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

## TYPICAL CHARACTERISTICS

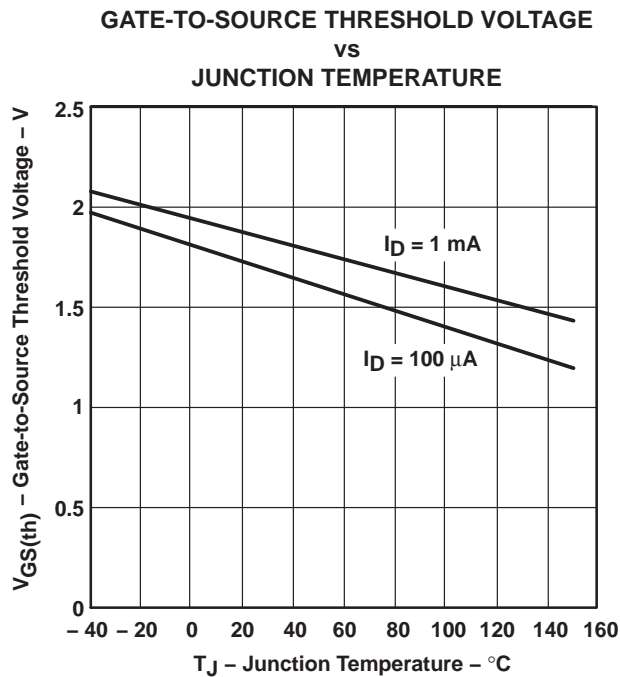


Figure 5

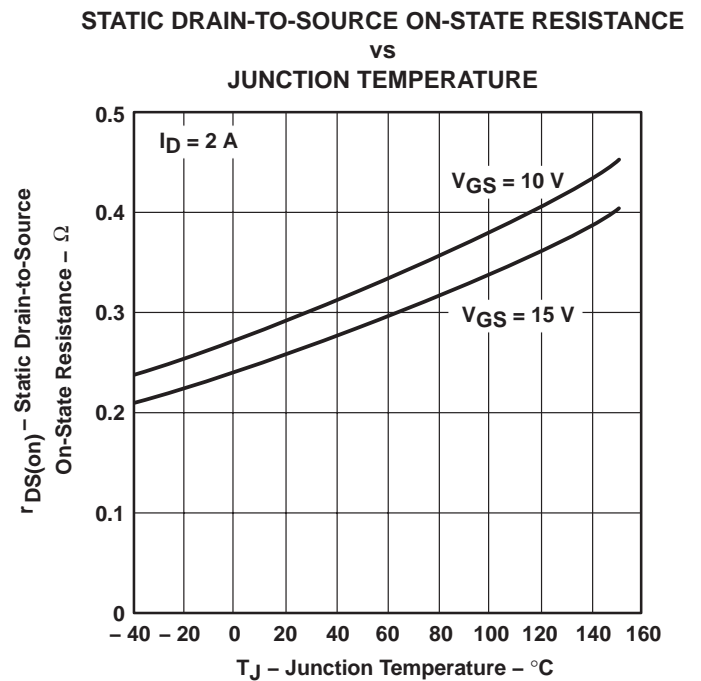


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

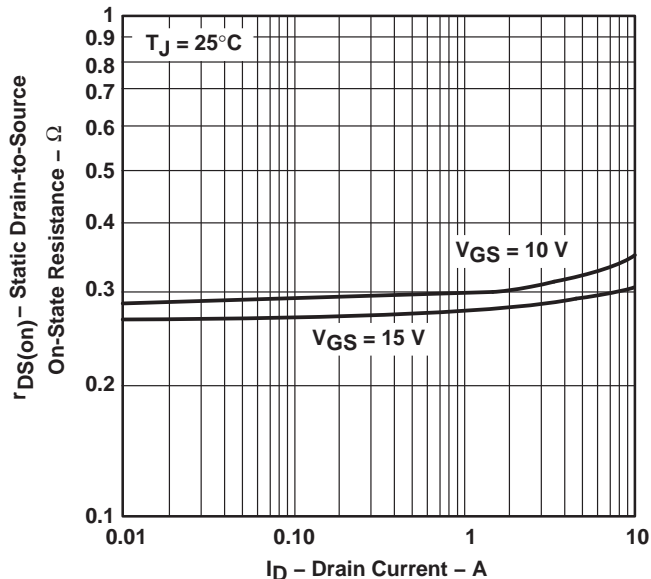


Figure 7

DRAIN CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE

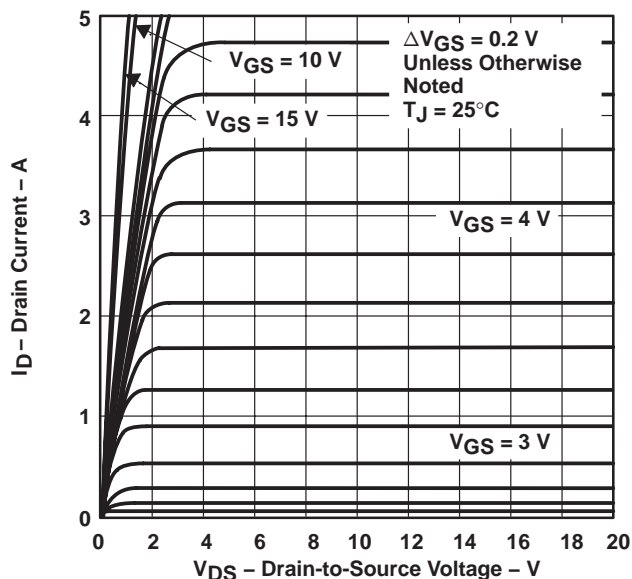


Figure 8

DISTRIBUTION OF  
FORWARD TRANSCONDUCTANCE

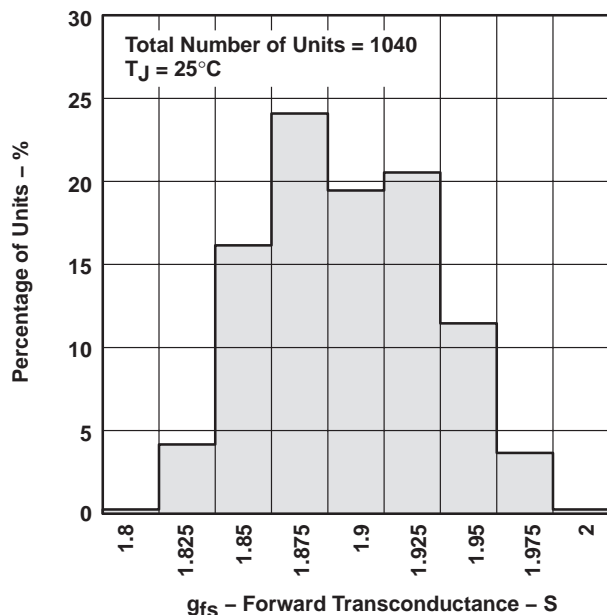


Figure 9

DRAIN CURRENT  
vs  
GATE-TO-SOURCE VOLTAGE

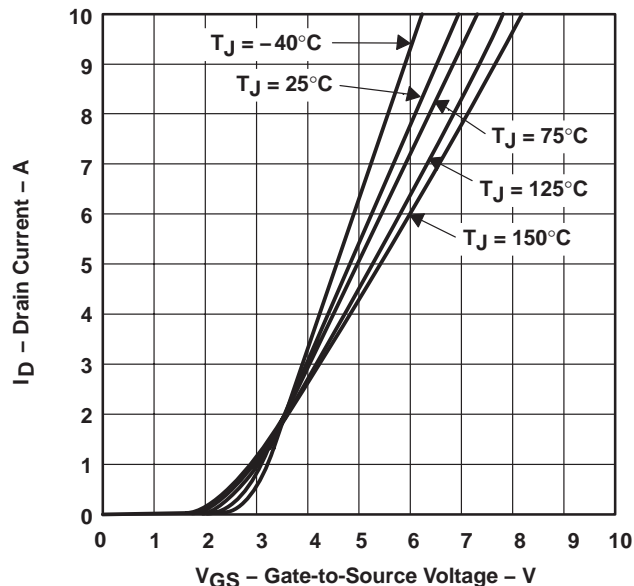


Figure 10

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## TYPICAL CHARACTERISTICS

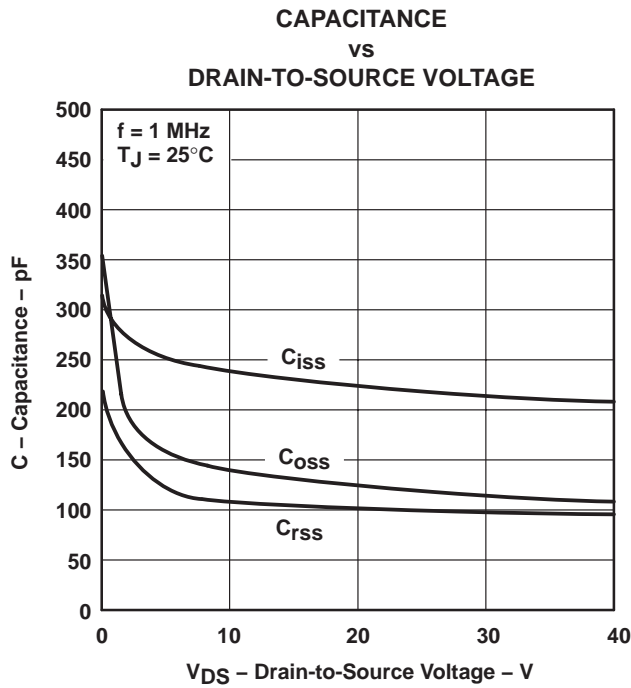


Figure 11

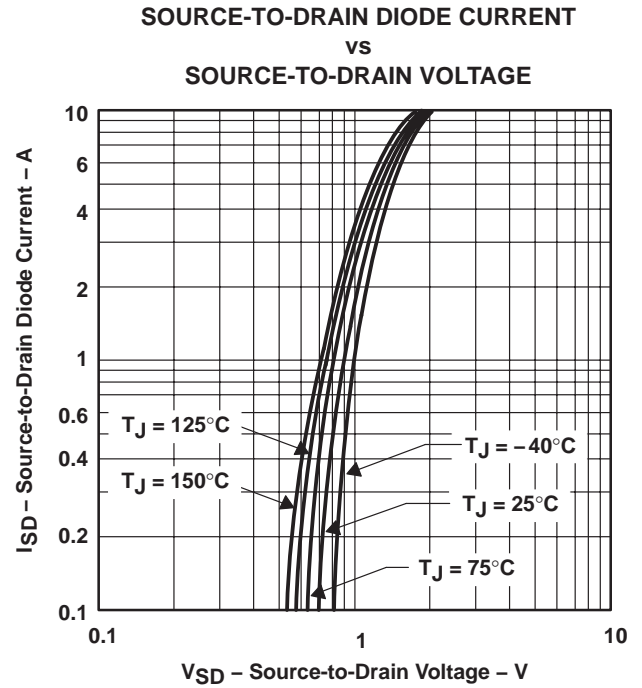


Figure 12

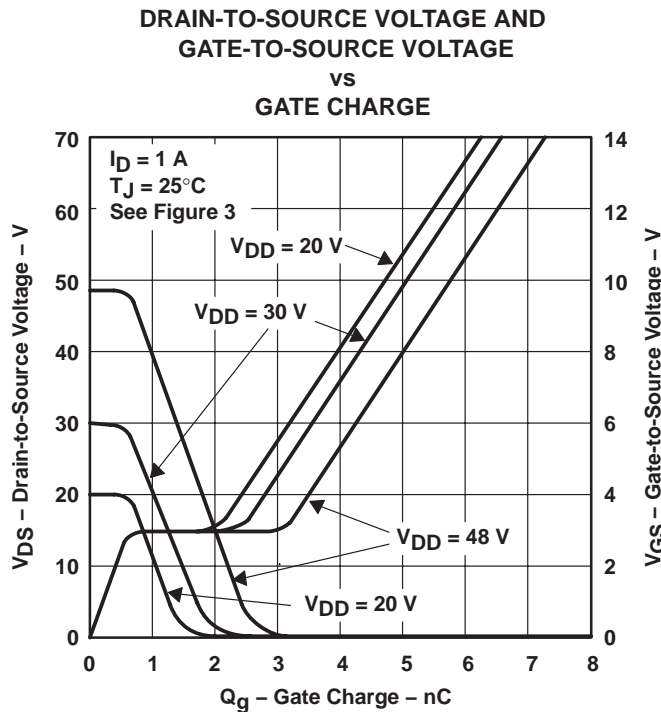


Figure 13

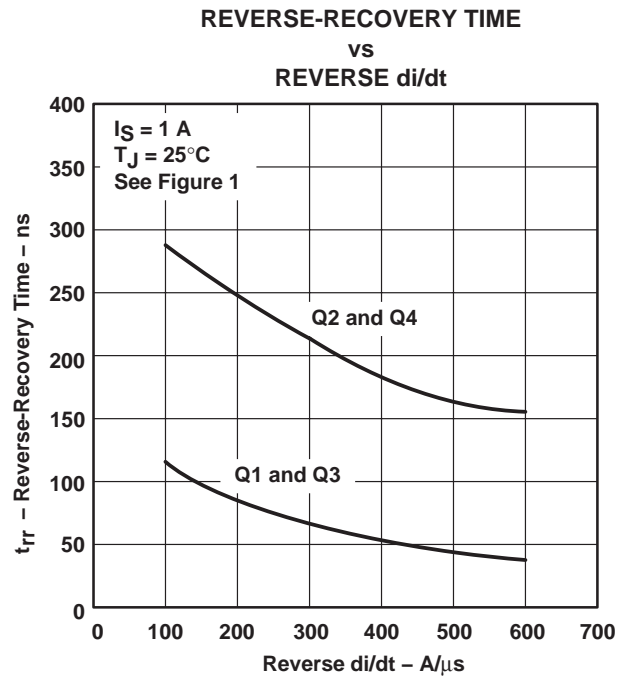
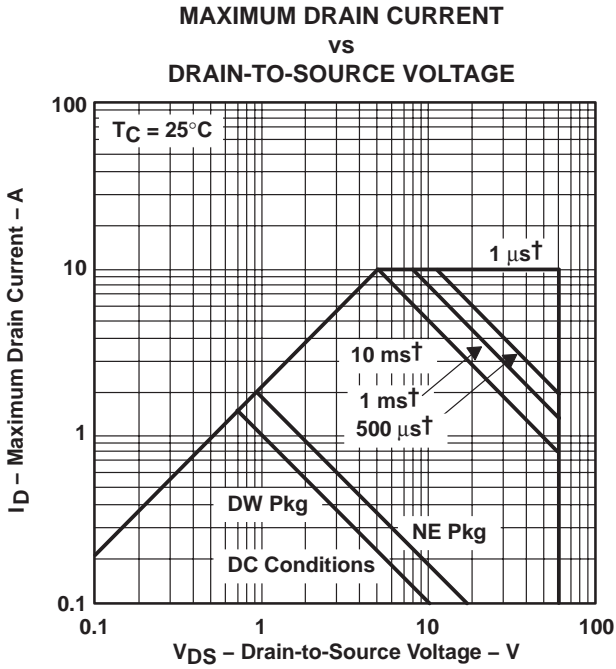


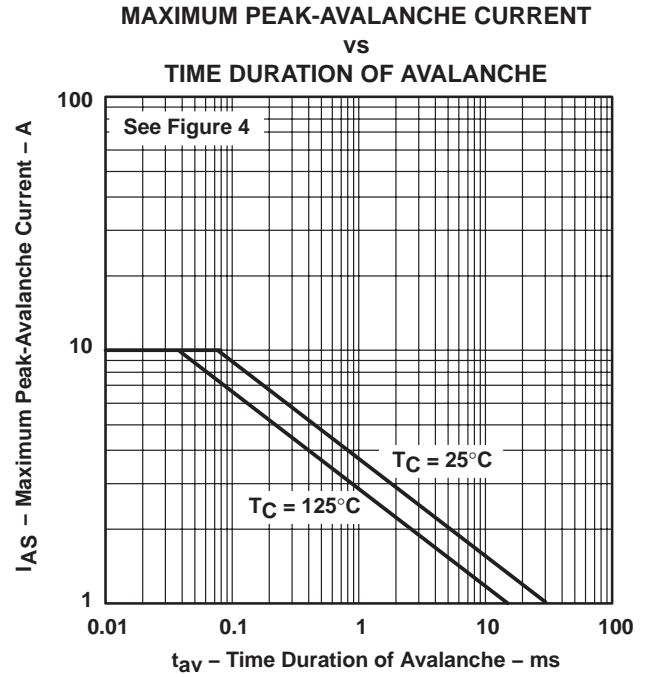
Figure 14



THERMAL INFORMATION



† Less than 0.1 duty cycle

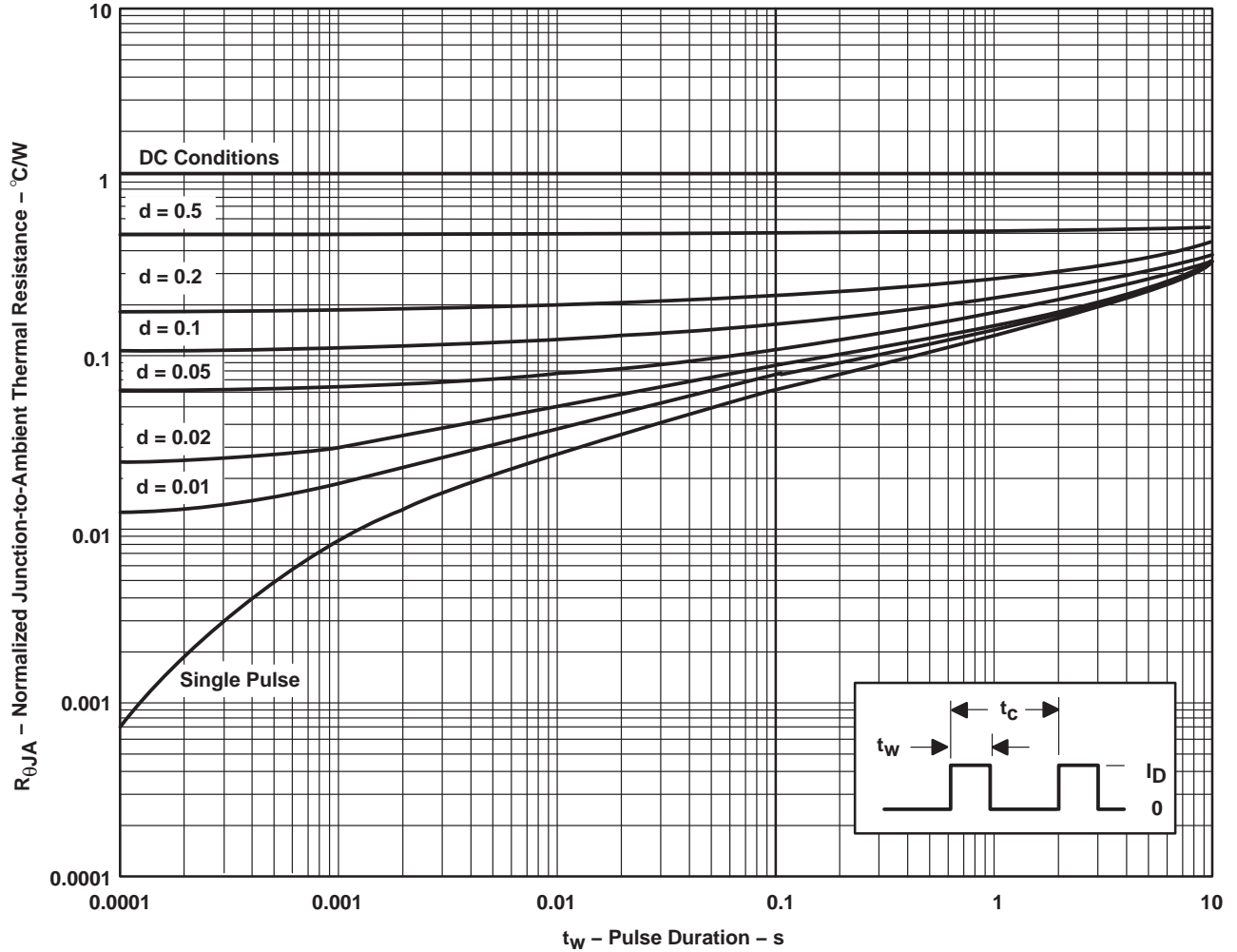


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## THERMAL INFORMATION

NE PACKAGE†  
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE  
VS  
PULSE DURATION



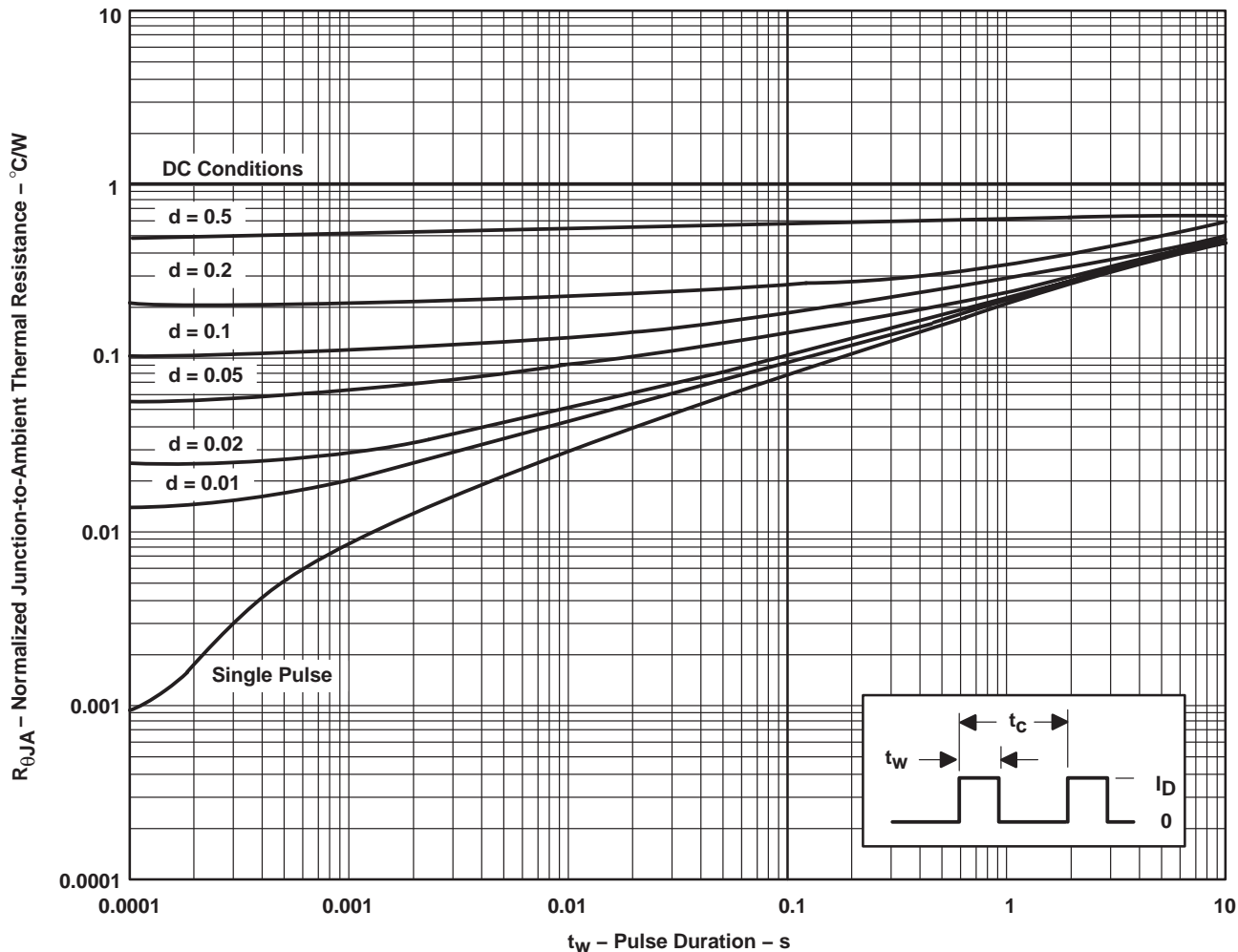
† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 17

THERMAL INFORMATION

DW PACKAGE†  
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE  
VS  
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 18

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPIC5404DW       | OBSOLETE              | SOIC         | DW              | 20   |             | TBD                     | Call TI          | Call TI                      |
| TPIC5404NE       | OBSOLETE              | PDIP         | NE              | 16   |             | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

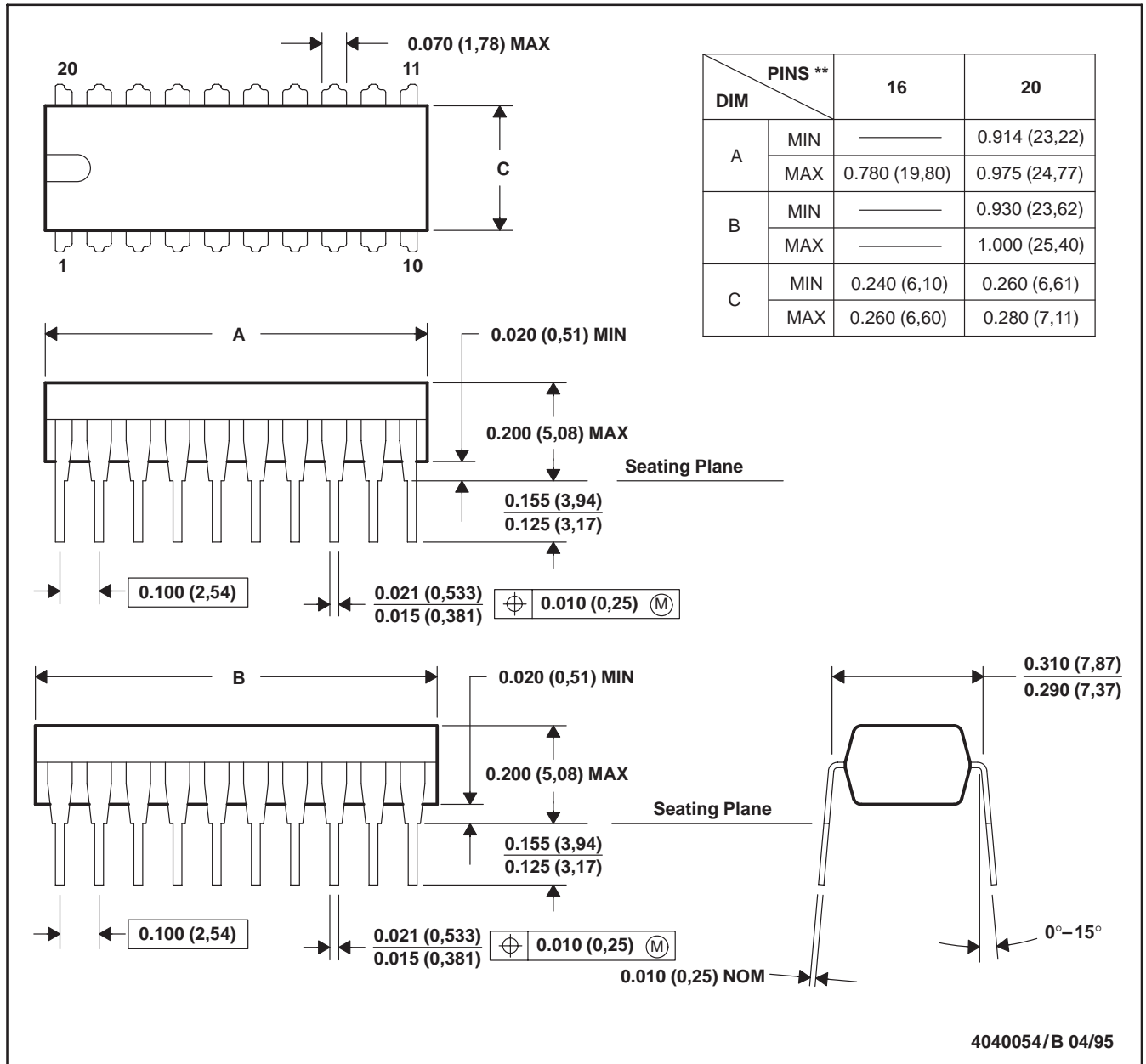
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NE (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (16 pin only)

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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| Data Converters             | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     |
| DLP® Products               | <a href="http://www.dlp.com">www.dlp.com</a>                       |
| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             |
| Logic                       | <a href="http://logic.ti.com">logic.ti.com</a>                     |
| Power Mgmt                  | <a href="http://power.ti.com">power.ti.com</a>                     |
| Microcontrollers            | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> |
| RFID                        | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>               |
| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

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|                               |  |
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