# 42-V/300-mA Wide-Input Ultra-low Quiescent Current Low-Dropout Linear Regulator with Power-Good Indicator

## Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, $T_A$: −40°C to +125°C
  - Junction Temperature, $T_J$: −40°C to +150°C
- Input Voltage: 3 V to 42 V
- Output Voltage:
  - Fixed 5 V and 3.3 V
- ±2% Output Accuracy Over Line Regulation, Load Regulation, and Operating Temperature Range
- Low Current Consumption:
  - 400-nA Shutdown Current
  - 3-μA Typical Quiescent Current
- 300-mA Maximum Output Current
- Low Dropout Voltage: 720 mV Maximum at 200 mA Load Current
- Integrated Power-Good Indicator
  - Adjustable Power-Good Delay Time
  - Open-Drain Output
- Stable with 1-μF to 200-μF Output Capacitor with ESR Range from 0.001 Ω to 10 Ω
- Integrated Protection:
  - Over-Current Protection
  - Over-Temperature Protection
- Package Option:
  - EMSOP8

## Applications

- Automotive Clusters and Infotainment
- Automotive Headlights and Interior Lighting
- Automotive Domain Control
- Automotive BCM and Door Handler

## Description

The TPL8034Q series supports operating with 3 V to 42 V (45-V maximum transient voltage). Operating with as low as 3 V allows the TPL8034Q to work well during cold-crank and start-stop conditions.

The TPL8034Q products are 3-μA ultra-low quiescent low dropout voltage linear regulators with 300-mA maximum output current capability.

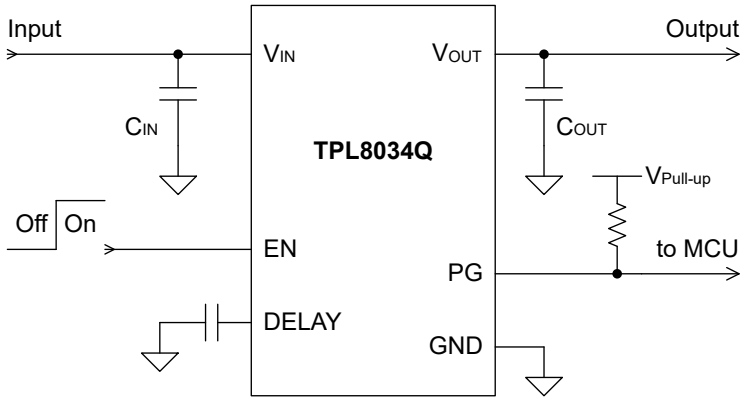
The TPL8034Q series integrates an open-drain output power good indicator. The power-good delay time is adjusted with an external capacitor.

With the above features, the TPL8034Q products are the optimal solutions for powering the MCU, CAN/LIN transceivers in the always-on applications, and the battery-connected applications in the automotive systems.

The TPL8034Q series provides fixed 5-V and 3.3-V output voltage options. What's more, the TPL8034Q supports a wide range of output capacitors from 1 μF to 200 μF with an ESR range from 0.001 Ω to 10 Ω. The TPL8034Q series integrates over-current protection and over-temperature protection.

The TPL8034Q series operates in the ambient temperature range from −40°C to +125°C. Additionally, the TPL8034Q series provides a thermal-enhanced EMSOP8 package to enable sustained operation despite significant dissipation.

## Typical Application Circuit



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## Product Family Table

| Order Number | Output Voltage (V) | Package |
|---|---|---|
| TPL803433Q-EV1R-S | 3.3 V | EMSOP8 |
| TPL803450Q-EV1R-S | 5.0 V | EMSOP8 |

## Revision History

| Date | Revision | Notes |
|---|---|---|
| 2023-06-17 | Rev.Pre.0 | Preliminary datasheet. |
| 2023-07-30 | Rev.Pre.1 | 1. Updated Thermal Information.<br>2. Updated Electrical Characteristics Table. |
| 2023-09-02 | Rev.Pre.2 | Updated test waveforms. |
| 2024-09-27 | Rev.A.0 | Initial released. |

## Pin Configuration and Functions

EMSOP8 Package

Top View

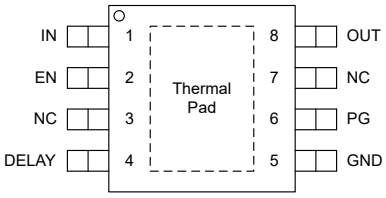



**Table 1. Pin Functions: TPL8034Q**

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 4 | DELAY | O | Power-good delay adjustment pin. Connecting a capacitor from the DELAY pin to GND to set the PG delay time. |
| 2 | EN | I | Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. |
| 5 | GND | - | Ground reference pin. Connect the GND pin to the PCB ground plane directly. |
| 1 | IN | I | Input voltage pin. |
| 3, 7 | NC | - | No connection. |
| 8 | OUT | O | Regulated output voltage pin. |
| 6 | PG | O | Power-good indication pin. The PG pin is an open-drain output and must be connected to $V_{OUT}$ or pull-up voltage through an external resistor. |

(1) Thermal Pad **MUST** be connected to PCB ground plane directly.

# Specifications

## Absolute Maximum Ratings

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| EN, IN | | −0.3 | 45 | V |
| OUT, DELAY, PG | | −0.3 | 6 | V |
| $T_J$ | Junction Temperature Range | −40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | −65 | 150 | °C |
| $T_L$ | Lead Temperature (Soldering 10 sec) | | 260 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

## ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|---|---|---|---|---|
| HBM | Human Body Model ESD | AEC Q100-002 | ±2 | kV |
| CDM | Charged Device Model ESD | AEC Q100-011 | ±1 | kV |

## Recommended Operating Conditions

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| IN | | 3 | 42 | V |
| EN | | 0 | $V_{IN}$ | V |
| $C_{OUT}$ | Output Capacitor Requirements | 1 | 200 | μF |
| ESR | Output Capacitor ESR Requirements | 0.001 | 10 | Ω |
| $C_{DELAY}$ | DELAY Capacitor | 0.1 | 100 | nF |
| $T_A$ | Ambient Temperature Range | −40 | 125 | °C |
| $T_J$ | Junction Temperature Range | −40 | 150 | °C |

## Thermal Information

| Package Type | $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC,top}$ | $\theta_{JC,bottom}$ | Unit |
|---|---|---|---|---|---|
| EMSOP8 | 45.6 | 43.3 | 95.2 | 12.8 | °C/W |

## Electrical Characteristics

All test conditions: $V_{IN}$ = 13.5 V, $V_{EN}$ = 2 V, $C_{IN}$ = $C_{OUT}$ = 10 μF, $I_{OUT}$ = 0.1 mA. $T_A$ = −40°C to +125°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Input Voltage and Current** | | | | | | |
| $V_{IN}$ | Input Supply Voltage Range (1) | | $V_{IN, MIN}$ | | 42 | V |
| UVLO | $V_{IN}$ Under-Voltage Lockout Threshold | $V_{IN}$ rising, $V_{EN}$ = 2 V, $I_{OUT}$ = 200 mA | | 2.6 | 2.8 | V |
| | Hysteresis | | | 260 | | mV |
| $I_{SD}$ | Shutdown Current | $V_{EN}$ = 0 V | | 0.4 | 2 | μA |
| $I_Q$ | Quiescent Current | $I_{OUT}$ = 0 mA | | 3 | 5.5 | μA |
| | | $I_{OUT}$ = 0.1 mA | | 4 | 6.5 | μA |
| **Enable Input Voltage and Current** | | | | | | |
| $V_{IH, EN}$ | EN Logic Input High (Enable) | | 1.4 | | $V_{IN}$ | V |
| $V_{IL, EN}$ | EN Logic Input Low (Disable) | | 0 | | 0.7 | V |
| $I_{EN}$ | EN Pin Leakage Current | $V_{EN}$ = 2 V to 42 V | −200 | | 200 | nA |
| **Regulated Output Voltage and Current** | | | | | | |
| $V_{OUT}$ | Output Accuracy | $V_{IN}$ = 6 V to 42 V, $I_{OUT}$ = 1 mA to 300 mA | −2% | | 2% | |
| $\Delta V_{OUT}$ | Line Regulation | $V_{IN}$ = 6 V to 42 V, $I_{OUT}$ = 10 mA | | 0.1 | | mV |
| | Load Regulation | $I_{OUT}$ = 1 mA to 300 mA | | 5 | | mV |
| $V_{DO}$ | Dropout Voltage (2) | $I_{OUT}$ = 100 mA, $V_{OUT}$ = 3.3 V | | 280 | 450 | mV |
| | | $I_{OUT}$ = 200 mA, $V_{OUT}$ = 3.3 V | | 580 | 900 | mV |
| | | $I_{OUT}$ = 100 mA, $V_{OUT}$ = 5 V | | 220 | 360 | mV |
| | | $I_{OUT}$ = 200 mA, $V_{OUT}$ = 5 V | | 440 | 720 | mV |
| $I_{OUT}$ | Output Current Range | $V_{OUT}$ in regulation | 0 | | 300 | mA |
| $I_{CL}$ | Output Current Limit | $V_{OUT}$ is forced to 0.9×$V_{OUT, NOM}$ | 320 | 500 | 900 | mA |
| $t_{SU}$ | Start-Up Time (3) | | | 2 | | ms |
| PSRR | Power Supply Rejection Ratio (3) | $I_{OUT}$ = 10 mA, f = 1 kHz | | 65 | | dB |
| | | $I_{OUT}$ = 10 mA, f = 100 kHz | | 50 | | dB |
| | | $I_{OUT}$ = 10 mA, f = 1 MHz | | 40 | | dB |
| **Temperature Range** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold (3) | | | 175 | | °C |
| | Thermal Shutdown Hysteresis (3) | | | 20 | | °C |
| **Power Good and Delay** | | | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PG, TH}$ | Power-Good Threshold | $V_{OUT}$ increasing | 86% | 90% | 94% | ×$V_{OUT}$ |
| | Hysteresis (3) | | | 2% | | ×$V_{OUT}$ |
| $V_{PG, OL}$ | Power Good Output Low Level | | | | 0.4 | V |
| $I_{PG}$ | PG Pin Leakage Current | $V_{PG}$ = 5 V | | | 1 | μA |
| $V_{DELAY, TH}$ | DELAY Threshold | $V_{DELAY}$ rising to $V_{PG}$ = HIGH | 0.8 | 1 | 1.2 | V |
| $I_{DELAY, CHG}$ | $C_{DELAY}$ Charging Current | $V_{DELAY}$ = 0 V | 1 | 2 | 3 | μA |
| $I_{DELAY, DIS}$ | $C_{DELAY}$ Discharging Current (3) | $V_{DELAY}$ = 1 V | | 200 | | mA |
| $t_{DELAY}$ | Delay Time from $V_{OUT}$ = $V_{PG, TH}$ to PG = HIGH (3) (4) | $V_{OUT}$ = 5 V, $C_{DELAY}$ = 100 nF | | 50 | | ms |
| | | $V_{OUT}$ = 5 V, $C_{DELAY}$ = 0 | | 300 | | μs |
| $t_{DEG}$ | PG Deglitch Time (3) | If $V_{OUT}$ only drops for a short period, keep the PG voltage unchanged | | 200 | | μs |

(1) $V_{IN, MIN}$ = 3 V or $V_{OUT, NOM}$ + 1 V, whichever is greater.

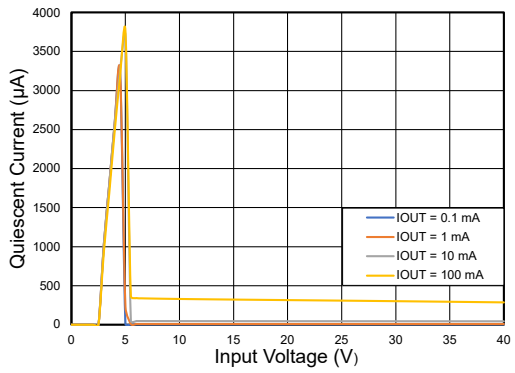
(2) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured when the output voltage has dropped 100 mV from the nominal value. In dropout, the output voltage will be equal to ($V_{IN}$ – $V_{DO}$).

(3) Not tested during production.

(4) $t_{DELAY}$ = ($C_{DELAY}$×$V_{DELAY, TH}$)/ $I_{DELAY, CHG}$

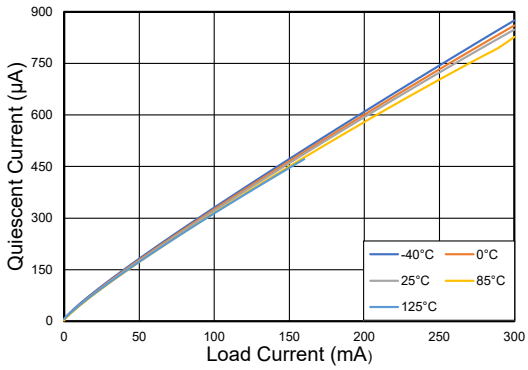
## Typical Performance Characteristics

All test conditions: $V_{IN}$ = 13.5 V, $V_{EN}$ = 2 V, $C_{IN}$ = $C_{OUT}$ = 10 µF, $I_{OUT}$ = 0.1 mA. $T_A$ = −40°C to +125°C, unless otherwise noted.



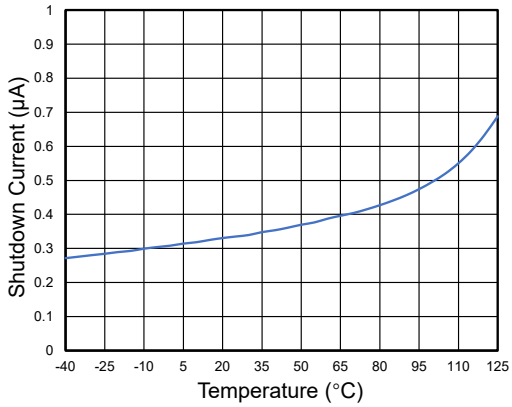

$V_{OUT}$ = 5 V

**Figure 1. Quiescent Current vs Input Voltage**



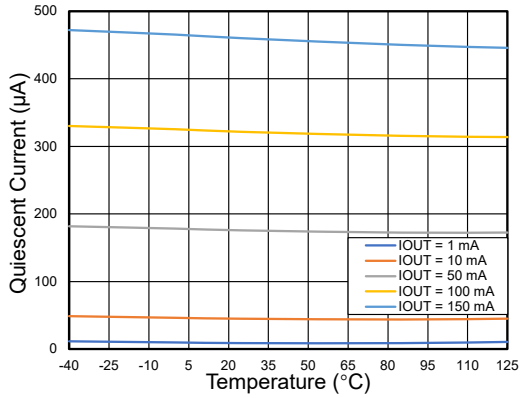

$V_{OUT}$ = 5 V

**Figure 2. Quiescent Current vs Load Current**



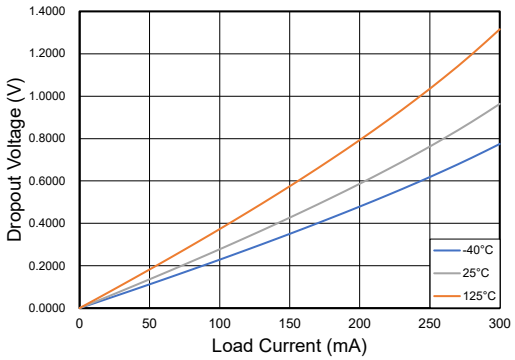

$V_{EN}$ = 0 V

**Figure 3. Shutdown Current vs Ambient Temperature**



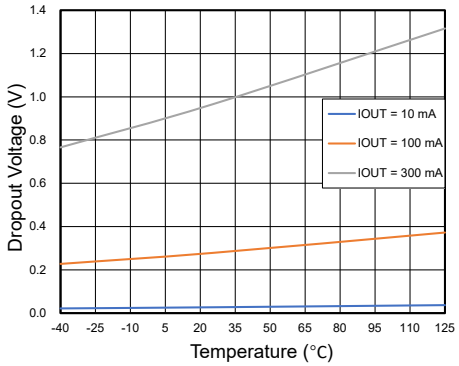

$V_{OUT}$ = 5 V

**Figure 4. Quiescent Current vs Ambient Temperature**



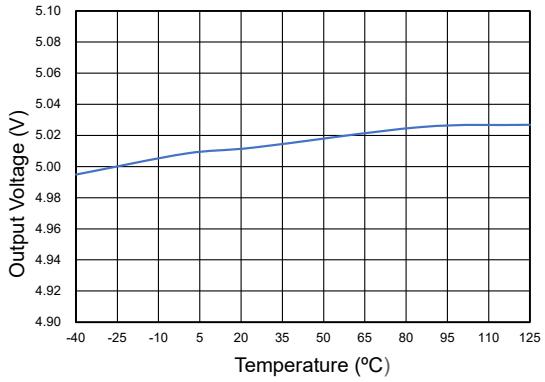

$V_{OUT}$ = 3.3 V

**Figure 5. Dropout Voltage vs Load Current**



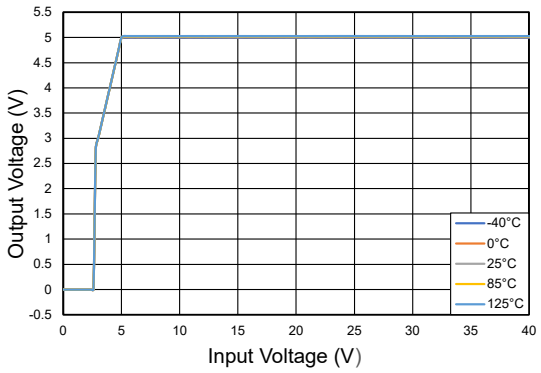

$V_{OUT}$ = 3.3 V

**Figure 6. Dropout Voltage vs Ambient Temperature**



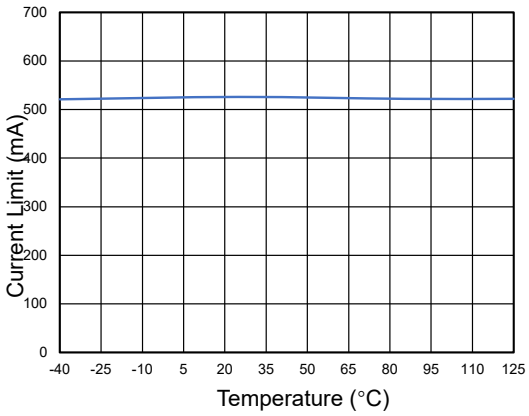

$V_{OUT}$ = 5 V

**Figure 7. Output Voltage vs Ambient Temperature**



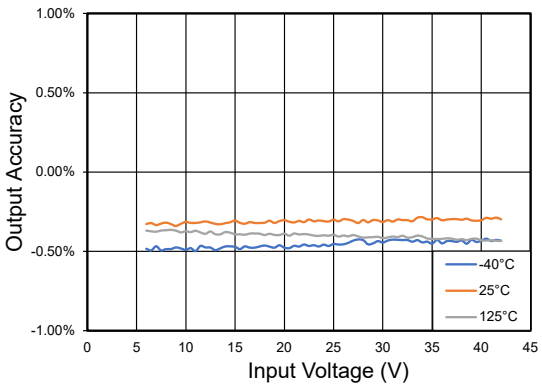

$V_{OUT}$ = 5 V, $I_{OUT}$ = 1 mA

**Figure 8. Output Voltage vs Input Voltage**



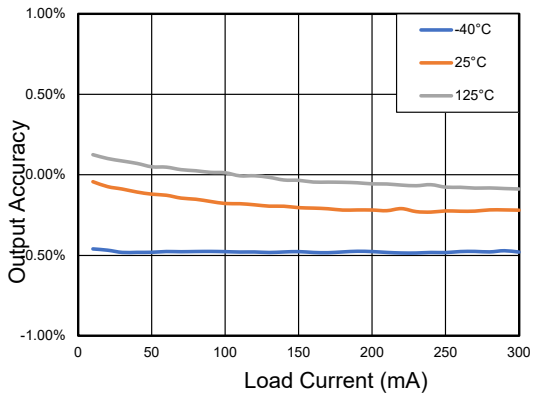

$V_{OUT}$ = 5 V, force $V_{OUT}$ = 0.9×$V_{OUT, NOM}$

**Figure 9. Output Current Limit vs Ambient Temperature**



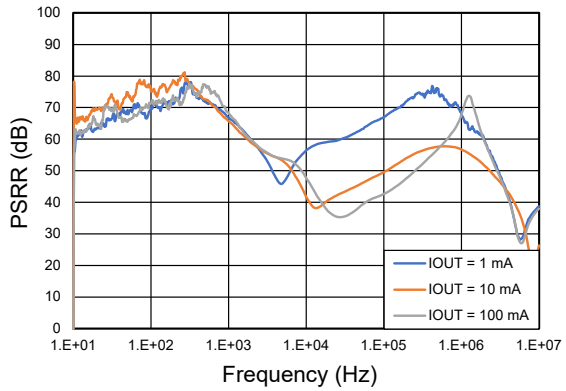

$V_{OUT}$ = 5 V

**Figure 10. Line Regulation**



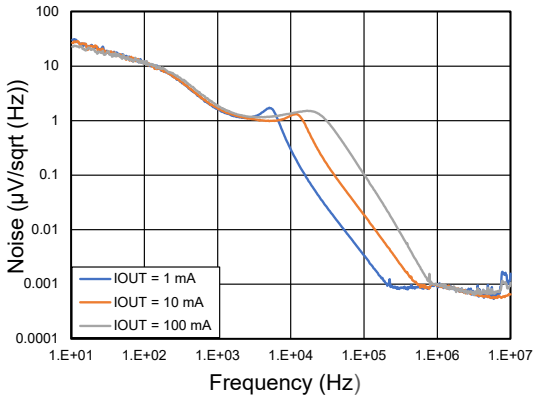

$V_{OUT}$ = 5 V

**Figure 11. Load Regulation**




$V_{OUT}$ = 5 V

**Figure 12. PSRR**




$V_{OUT}$ = 5 V

**Figure 13. Noise**

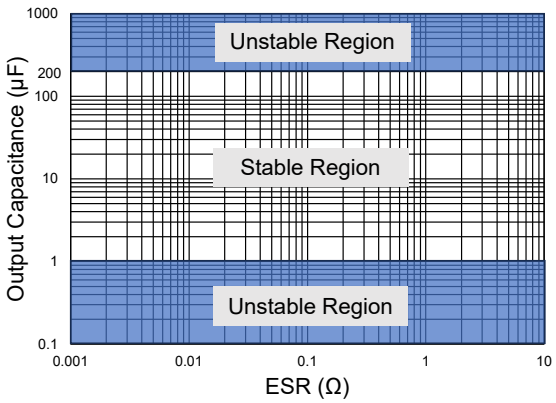
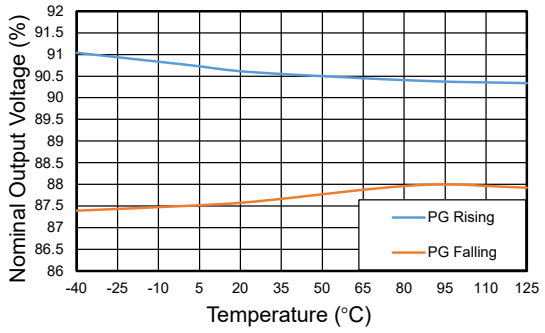
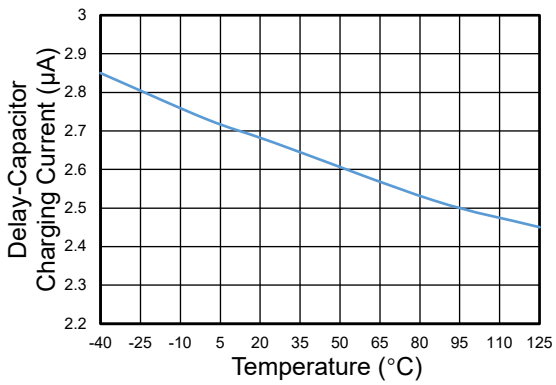



**Figure 14. Output Capacitance vs ESR stability**



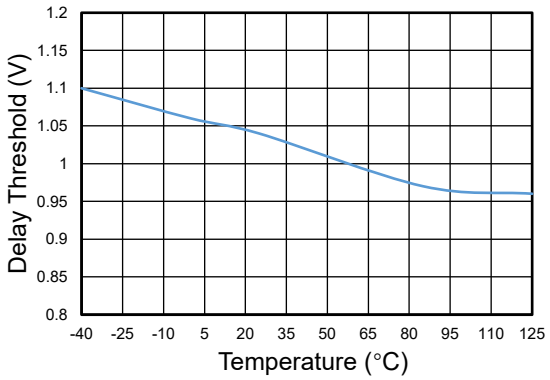

$V_{OUT}$ = 5 V

**Figure 15. Power-Good Threshold Voltage vs Temperature**



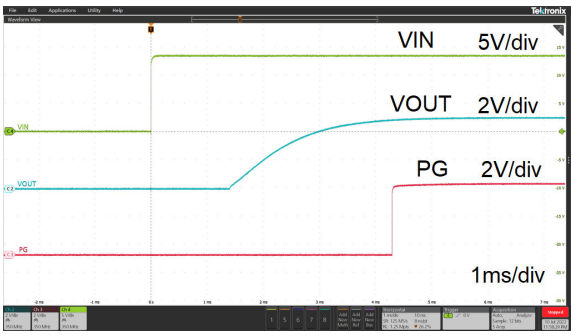

$V_{OUT}$ = 5 V

**Figure 16. Delay Charging Current**



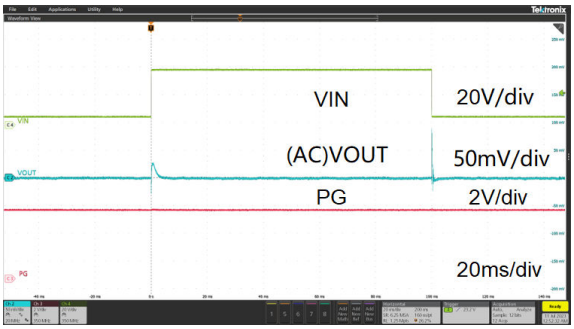

$V_{OUT}$ = 5 V

**Figure 17. Delay Charging Threshold**



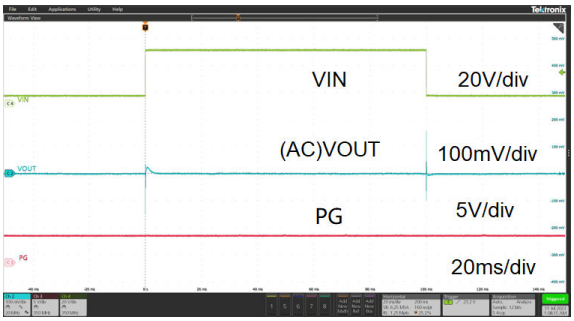

$C_{OUT}$ = 10 μF, $V_{IN}$ = 0 V to 13.5 V, $V_{OUT}$ = 0 V to 5 V, $I_{OUT}$ = 0.1mA

**Figure 18. Startup Waveform**



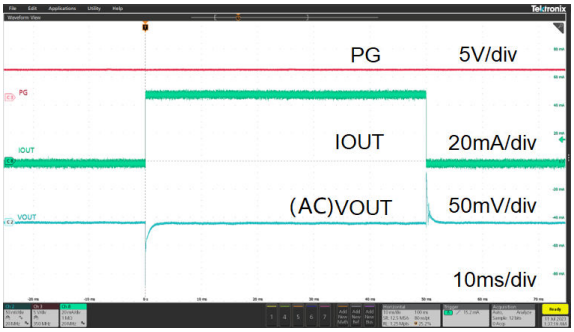

$V_{IN}$ = 6 to 40 V (1 V/µs), $V_{OUT}$ = 5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 1 mA

**Figure 19. Line Transient**



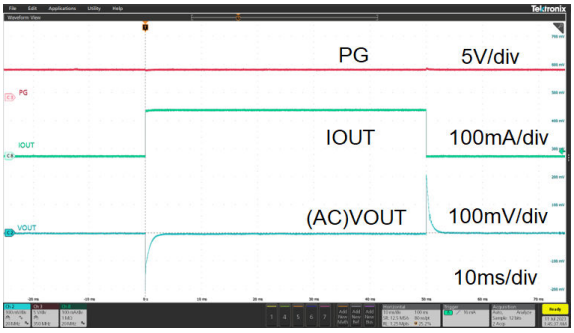

$V_{IN}$ = 6 to 40 V (1 V/µs), $V_{OUT}$ = 5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 10 mA

**Figure 20. Line Transient**




$V_{IN}$ = 13.5 V, $V_{OUT}$ = 5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 1 mA to 50 mA

**Figure 21. Load Transient**




$V_{IN}$ = 13.5 V, $V_{OUT}$ = 5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 1 mA to 150 mA

**Figure 22. Load Transient**

# Detailed Description

## Overview

The TPL8034Q series supports the operating range from 3 V to 42 V (45-V maximum transient voltage). Operating as low as 3 V allows the TPL8034Q to work well during cold-crank and start-stop conditions.

The TPL8034Q products are 3-μA ultra-low quiescent low dropout voltage linear regulators with 300-mA maximum output current capability.

The TPL8034Q series integrates an open-drain output power good indicator. The power-good delay time is adjusted with an external capacitor.

With the above features, the TPL8034Q products are the optimal solutions for powering the MCU, CAN/LIN transceivers in the always-on applications, and battery-connected applications in automotive systems.

The TPL8034Q series provides fixed 5-V and 3.3-V output voltage options. The TPL8034Q supports a wide range of output capacitors from 1 μF to 200 μF with an ESR range from 0.001 Ω to 10 Ω. Also, the TPL8034Q series integrates over-current protection and over-temperature protection.

## Functional Block Diagram

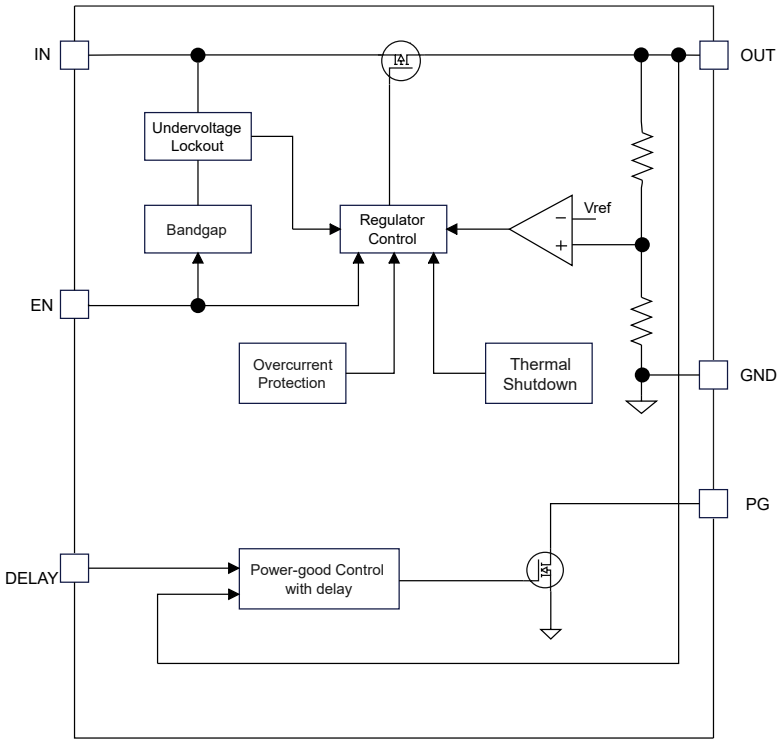



**Figure 23. Functional Block Diagram**

## Feature Description

### Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

### Under-Voltage Lockout (UVLO)

The TPL8034Q series uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

### Regulated Output Voltage (OUT)

The TPL8034Q series is available in fixed voltage versions of 5 V and 3.3 V. When the input voltage is higher than $V_{OUT, NOM}$ + $V_{DO}$, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT, NOM}$ + $V_{DO}$, the output pin tracks the input voltage minus the dropout voltage based on the load current.

### Power-Good (PG)

The TPL8034Q series integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used, or leave the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold $V_{PG, TH}$. When the output voltage is higher than $V_{PG, TH}$, the PG pin turns to a high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

### Power-Good Delay Time (DELAY)

The TPL8034Q series uses an external capacitor to set the delay time before the PG pin turns to HIGH. There is a constant current charging the capacitor after the output voltage rises above $V_{PG, TH}$, and there is a constant current discharging the capacitor after the output voltage falls below $V_{PG, TH}$. The power-good delay time can be calculated using Equation 1

$$t_{DELAY} = \frac{C_{DELAY} \times V_{DELAY,\ TH}}{I_{DELAY,\ CHG}} \quad (1)$$

Where:

- the typical value of $V_{DELAY, TH}$ is 1 V.
- the typical value of $I_{DELAY, CHG}$ is 2 μA.
- $C_{DELAY}$ is the external capacitor at the DELAY pin.

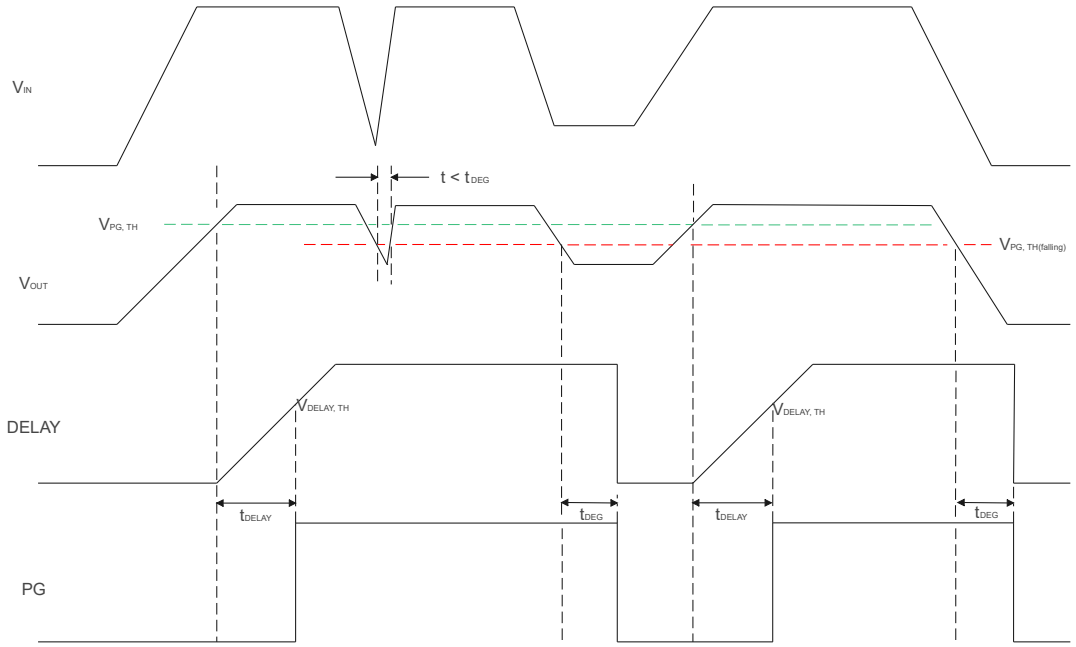



**Figure 24. Power-Good Delay Time**

### Over-Current Protection

The TPL8034Q series integrates an internal current limit that helps to protect the regulator during fault conditions, e.g., the output is shorted to ground, or the output is forced below $V_{OUT, NOM}$. The output voltage is not regulated when the device is in current limit, and $V_{OUT} = I_{CL} \times R_{LOAD}$.

### Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown ($T_{SD}$) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table, continuously operating above the junction temperature range reduces the lifetime of the device.

# Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

The TPL8034Q series products are 42-V 3-μA ultra-low quiescent low dropout voltage linear regulators with 300-mA maximum output current capability. The following application schematic shows a typical usage of the TPL8034Q series.

## Typical Application

Figure 25 shows the typical application schematic of the TPL8034Q series.

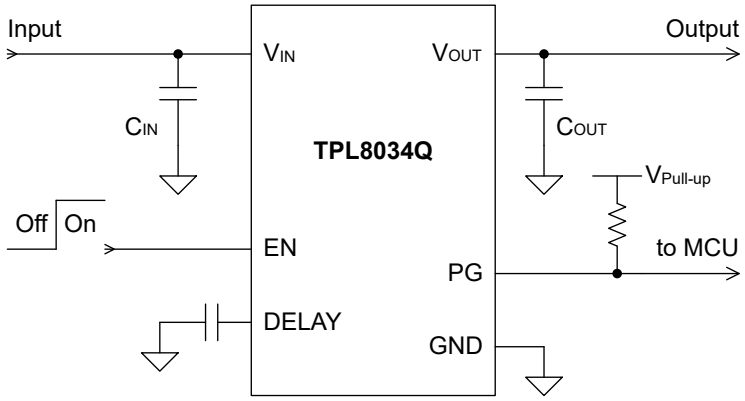



**Figure 25. Typical Application Circuit**

### Input Capacitor and Output Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. 3PEAK recommends adding a 10-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL8034Q series requires an output capacitor of 1 μF to 200 μF with an ESR range from 0.001 Ω to 10 Ω. 3PEAK recommends selecting an X7R type 10-μF ceramic capacitor with low ESR over temperature.

Both input and output capacitors must be placed as close to the device pins as possible.

### Power Dissipation and Thermal Consideration

During normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using Equation 3. $\theta_{JA}$ is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

# Layout

## Layout Guideline

- Both input and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

## Layout Example

The following figure shows a layout example of TPL8034Q.

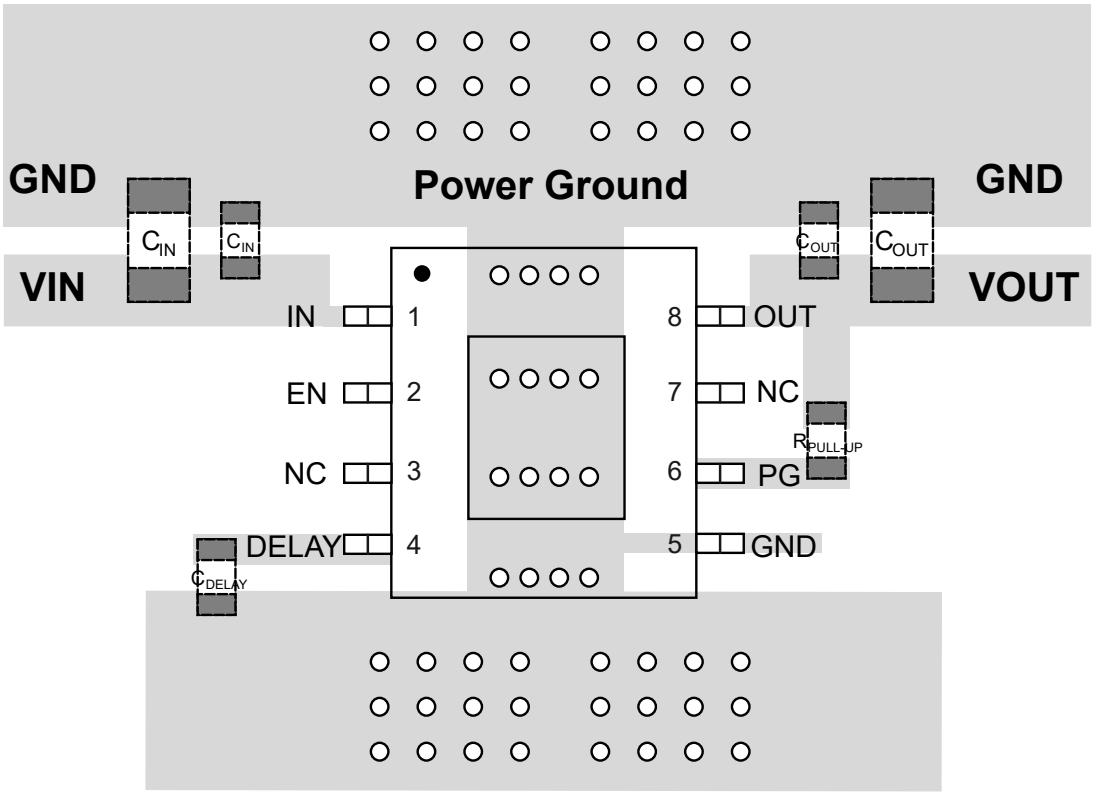
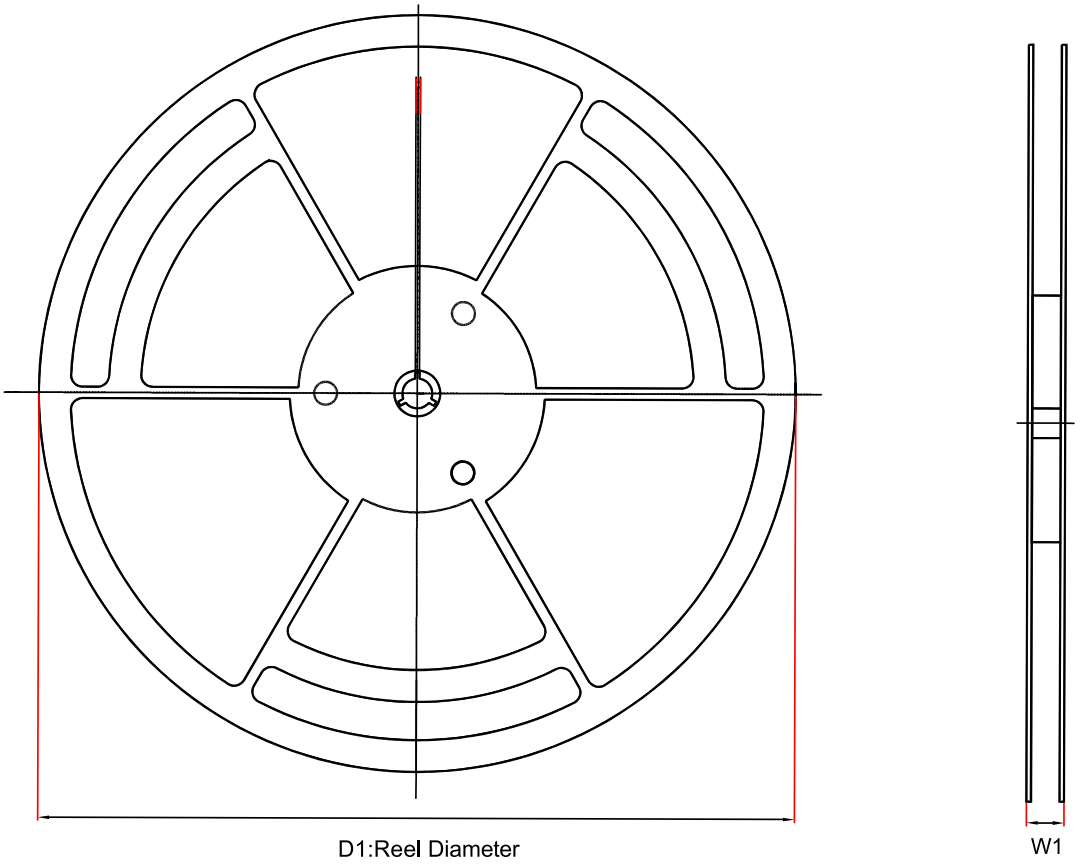
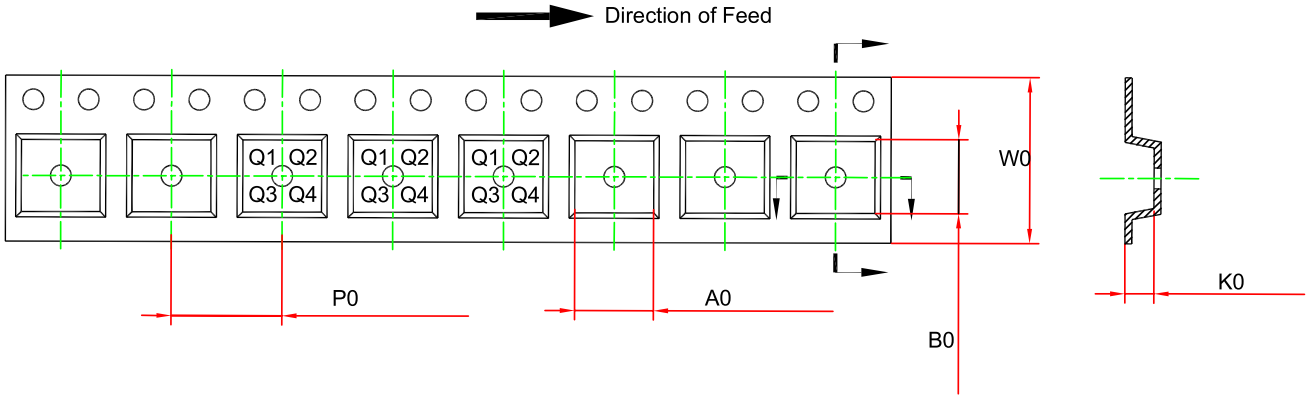



**Figure 26. TPL8034Q Layout Example**

## Tape and Reel Information



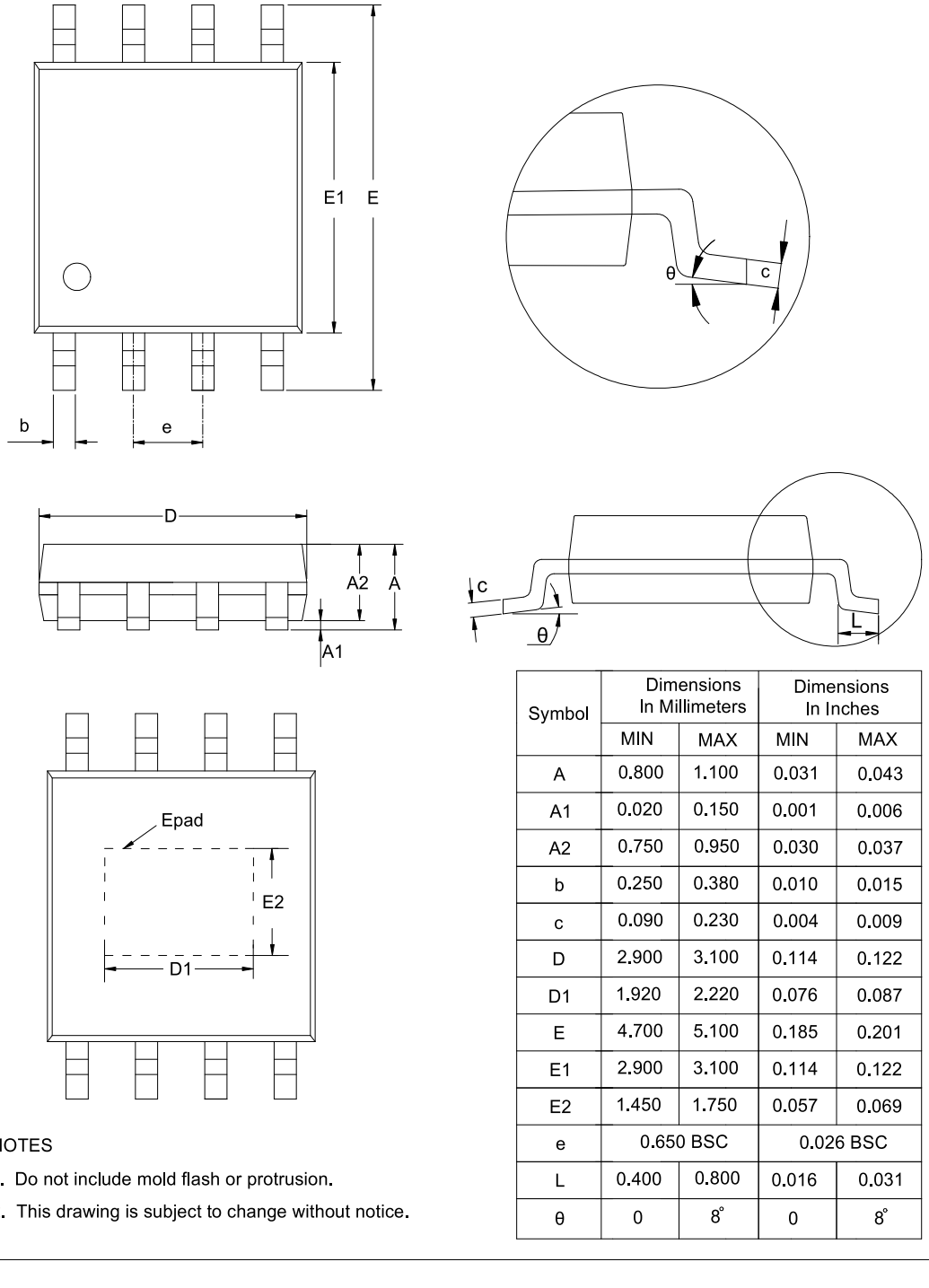




| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| TPL803433Q-EV1R-S | EMSOP8 | 330 | 17.6 | 5.3 | 3.4 | 1.4 | 8 | 12 | Q1 |
| TPL803450Q-EV1R-S | EMSOP8 | 330 | 17.6 | 5.3 | 3.4 | 1.4 | 8 | 12 | Q1 |

## Package Outline Dimensions

### EMSOP8

Package Outline Dimensions EV1(EMSOP-8-B)




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 1.100 | 0.031 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 1.920 | 2.220 | 0.076 | 0.087 |
| E | 4.700 | 5.100 | 0.185 | 0.201 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| E2 | 1.450 | 1.750 | 0.057 | 0.069 |
| e | 0.650 BSC | | 0.026 BSC | |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0 | 8° | 0 | 8° |

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

## Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|---|---|---|---|---|---|---|
| TPL803433Q-EV1R-S | −40 to 125°C | EMSOP8 | L3433 | MSL2 | 3,000 | Green |
| TPL803450Q-EV1R-S | −40 to 125°C | EMSOP8 | L3450 | MSL2 | 3,000 | Green |

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

# IMPORTANT NOTICE AND DISCLAIMER



**Performance Information.** Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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