Features

- Input Voltage Range:
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5V
- Output Voltage Options:
  - Fixed Output Voltage: 0.8 V to 3.95 V
  - Adjustable Output Voltage: 0.8 V to 5.2 V
- ±1% Output Accuracy Over Line, Load Regulation, and Operating Temperature Range With BIAS
- 3A Maximum Output Current
- Low Dropout Voltage: 145 mV typ at 3 A
- High PSRR:
  - 70dB at 1kHz
  - 40dB at 1MHz
- 6 μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Enable and Adjustable Soft-Start Control
- Open-Drain Power-Good (PG) Output
- Stable with a 47 µF or Larger Ceramic Output Capacitor
- Thermal Shutdown and Over-Current Protection
- Operating Junction Temperature: –40°C to +125°C
- Package Options:
  - 3.5×3.5 QFN-20

Applications

- Wireless Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

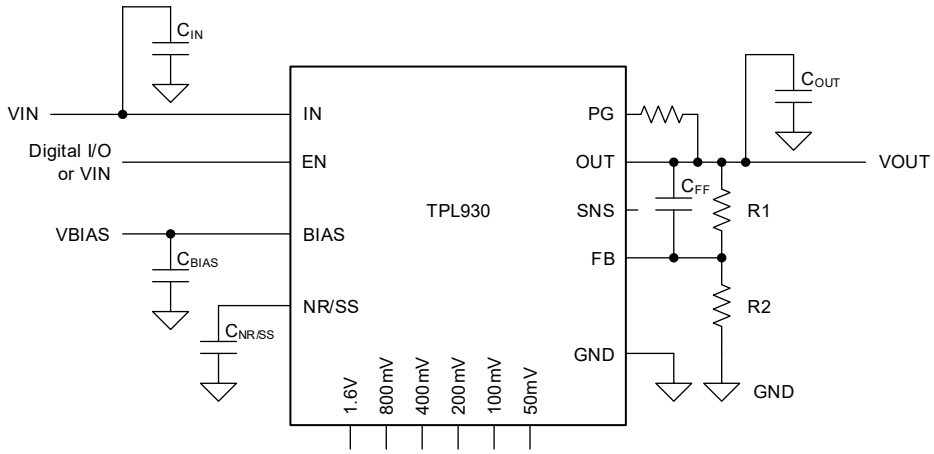
Description

The TPL930 series products are 3-A high-current, 6-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with typically 145-mV ultra-low dropout voltage. The TPL930 series products support both fixed output voltage ranges from 0.8 V to 3.95 V and adjustable output voltage ranges from 0.8 V to 5.2 V with external resistor divider.

Ultra-low noise, high PSRR, and high output current capability makes the TPL930 series products ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensures the TPL930 series products optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD and DSP.

The TPL930 series products provide 3.5×3.5 QFN-20 package with guaranteed operating junction temperature range (T_J) from –40°C to +125°C.

Typical Application Schematic



Product Family Table

Part Number	Output Voltage	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPL930	Adjustable (0.8 V ~ 5.2 V)	TPL930ADJ-QF6R	3.5×3.5 QFN-20	4,000	MSL3	L930A

Table of Contents

Revision History

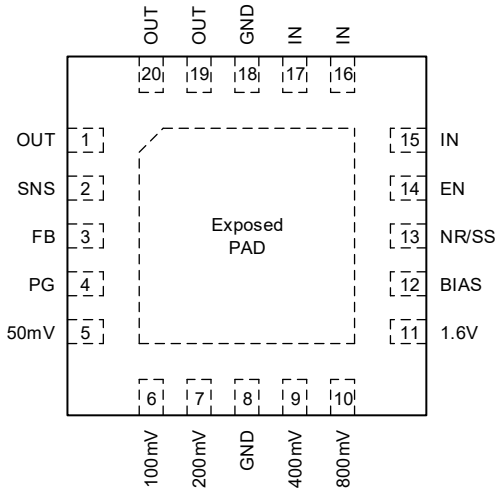
Date	Revision	Notes
2019/04/30	Rev.Pre	Preliminary Version
2020/05/08	Rev.A.0	Initial Release
2021/07/10	Rev.A.1	1. Add Tape and Reel Information in Page 17 2. Update Package Outline Dimension of A, A2, b, D2, E2, and L, in Page 18

Pin Configuration and Functions

TPL930 Series

QFN-20 Package

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	I	Fixed output voltage setting pins. Connecting these pins to ground increases the output voltage. Multiple pins may be simultaneously connected to GND to select the desired output voltage. Leave these pins open when use external resistor divider.
BIAS	12	I	BIAS voltage input pin. A 10-μF capacitor or larger must be connected between this pin and ground. BIAS must be left open or tied to ground when not used.
EN	14	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
FB	3	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
GND	8, 18	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
IN	15, 16, 17	I	Input voltage pin. A 10-μF or larger ceramic capacitor from IN to ground (as close as possible to IN pin) is required to reduce the jitter from previous-stage power supply.
NR/SS	13	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
OUT	1, 19, 20	O	Regulated output voltage pin. A 47-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
PG	4	O	Open-drain power-good output pin. Leave PG pin open when not used.
SNS	2	I	Output voltage sense input pin. Connect this pin to the load side of the output trace only when using fixed output voltage. Leave this pin open when using external resistor divider.

(1) Exposed PAD must be connected to a large-area ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

		MIN	MAX	UNIT
IN, BIAS, EN, PG		–0.3	7	V
OUT, SNS		–0.3	V_{IN} + 0.3	V
NR/SS, FB		–0.3	3.6	V
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V		–0.3	V_{OUT} + 0.3	V
T_J	Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
IN	Input voltage	1.1		6.5	V
BIAS	BIAS voltage	3		6.5	V
EN	Enable voltage	0		6.5	V
OUT	Output voltage	0.8		5.2	V
C_{IN}	Input capacitor	10			μF
C_{OUT}	Output capacitor	47	47//10//10		μF
C_{FF}	Feed-forward capacitor		10		nF
$C_{NR/SS}$	NR/SS capacitor		10		nF
R_{PG}	Power-good pull-up resistor	10		100	kΩ
R_1	High-side resistor of the resistor divider		12.1		kΩ
R_2	Low-side resistor of the resistor divider			160	kΩ
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

PACKAGE	θ_{JA}	$\theta_{JC,bottom}$	UNIT
3.5×3.5 QFN-20	60.6	10.8	°C/W

Electrical Characteristics

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Input Voltage and Current						
V_{IN}	Input supply voltage range		1.1		6.5	V
V_{BIAS}	Bias supply voltage range	V_{IN} = 1.1 V	3		6.5	V
$UVLO_{IN1}$	Input supply UVLO with BIAS	V_{IN} rising with V_{BIAS} = 3 V		0.75	1.0	V
	Hysteresis	V_{BIAS} = 3 V		60		mV
$UVLO_{IN2}$	Input supply UVLO without BIAS	VIN rising		1.3	1.4	V
	Hysteresis			200		mV
$UVLO_{BIAS}$	Bias supply UVLO	V_{BIAS} rising, V_{IN} = 1.1 V		2.7	2.95	V
	Hysteresis	V_{IN} = 1.1 V		180		mV
I_{GND}	GND pin current	V_{IN} = 6.5 V, I_{OUT} = 5 mA		17	30	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		12	25	mA
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, $V_{OUT(NOM)}$ = 0.8 V, I_{OUT} = 3 A		6	20	mA
I_{SD}	Shutdown current	V_{IN} = 6.5 V, V_{EN} = 0.5 V, PG = open		10	25	µA
I_{BIAS}	BIAS pin current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(NOM)}$ = 0.8 V, I_{OUT} = 3 A		3.5	10	mA
Enable and Power Good						
$V_{IH(EN)}$	EN pin high-level input voltage	Device enable	1.1		6.5	V
$V_{IL(EN)}$	EN pin low-level input voltage	Device disable	0		0.4	V
I_{EN}	EN pin current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V	–0.2		0.2	µA
V_{PG}	PG pin threshold	V_{OUT} falling	82%	88%	93%	× VOUT
	Hysteresis			2%		× VOUT
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < V_{PG}, source 1 mA to PG pin			0.4	V
I_{PG}	PG pin leakage current	V_{OUT} > V_{PG}, apply 6.5 V at PG pin			2	µA
Regulated Output Voltage and Current						
V_{FB}	Feedback voltage		0.8 – 1%	0.8	0.8 + 1%	V
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V, stress V_{FB} = 0.8V	–100		100	nA
$V_{NR/SS}$	NR/SS pin voltage			0.8		V
$I_{NR/SS}$	NR/SS pin charging current	V_{IN} = 6.5 V, $V_{NR/SS}$ = GND	4	7.2	9	µA
V_{OUT}	Output voltage range	Fixed	0.8		3.95	V
		Adjustable (resistor tolerances are not included)	0.8		5.2	V
	Accuracy	V_{OUT} = 0.8 V to 5.2 V, I_{OUT} = 5 mA to 3 A (resistor tolerances are not included)	–1%		1%	

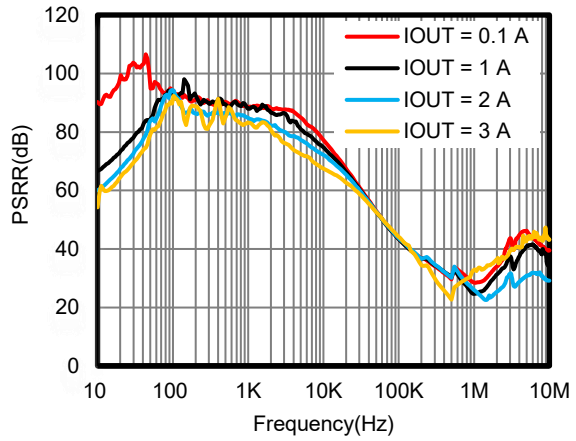
Electrical Characteristics (continued)

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 k Ω to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Regulated Output Voltage and Current							
ΔV_{OUT}	Line regulation	V_{IN} = 1.4 V to 6.5 V, I_{OUT} = 5 mA			0.03		mV/V
	Load regulation	V_{IN} = 1.1 V, V_{BIAS} = 3 V to 6.5 V, I_{OUT} = 5 mA to 3 A			0.7		mV/A
		I_{OUT} = 5 mA to 3 A			0.8		mV/A
V_{DO}	Dropout voltage without BIAS	V_{IN} = 1.4 V, I_{OUT} = 1 A, V_{FB} = 0.8 V – 3%			40	100	mV
		V_{IN} = 1.4 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			80	200	mV
		V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			140	300	mV
		V_{IN} = 5.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			145	300	mV
		V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			145	300	mV
	Dropout voltage with BIAS	V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{FB} = 0.8 V – 3%			40	100	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			80	200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			145	300	mV
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V		3.7	4.5	5.2	A
I_{SC}	Short-circuit current limit	R_{LOAD} ≤ 20 mΩ			0.8		A
PSRR and Noise							
PSRR	Power supply ripple rejection	I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 22 µF	f = 1 kHz, V_{BIAS} = 3 V		70		dB
			f = 1 MHz, V_{BIAS} = 3 V		40		dB
			f = 1 kHz		70		dB
			f = 1 MHz		40		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF			6		µVRMS
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 47 µF || 10µF || 10µF			8		µVRMS
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF			11		µVRMS
Temperature Range							
T_{SD}	Thermal shutdown threshold	Temperature increasing			160		°C
	Hysteresis				20		°C
T_J	Operating junction temperature			–40		125	°C

Typical Performance Characteristics

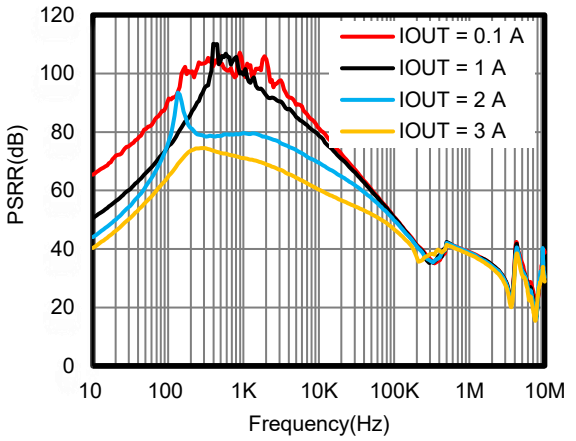
T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 k Ω to OUT, unless otherwise noted.



V_{IN} = 1.1 V, VBIAS = 3 V, V_{OUT} = 0.8 V,

C_{OUT} = 47µF // 10µF // 10µF, $C_{NR/SS}$ =100nF, C_{FF} = open

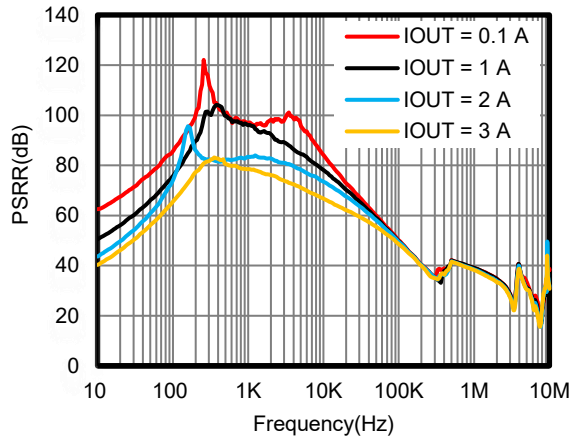
Figure 1 PSRR vs. Frequency and IOUT



V_{IN} = 5.5 V, VBIAS = 3 V, V_{OUT} = 5.2 V,

C_{OUT} = 47µF // 10µF // 10µF, $C_{NR/SS}$ =100nF, C_{FF} = open

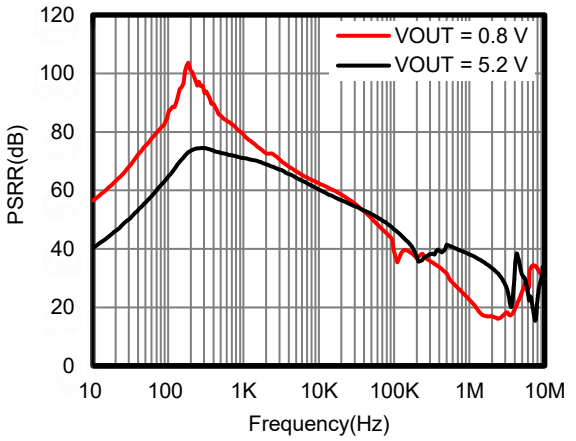
Figure 2 PSRR vs. Frequency and IOUT



V_{IN} = 5.5 V, VBIAS = open, V_{OUT} = 5.2 V,

C_{OUT} = 47µF // 10µF // 10µF, $C_{NR/SS}$ =100nF, C_{FF} = open

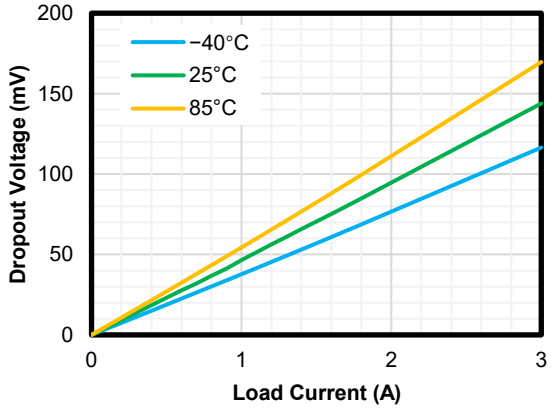
Figure 3 PSRR vs. Frequency and IOUT



V_{IN} = V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, VBIAS = 3V,

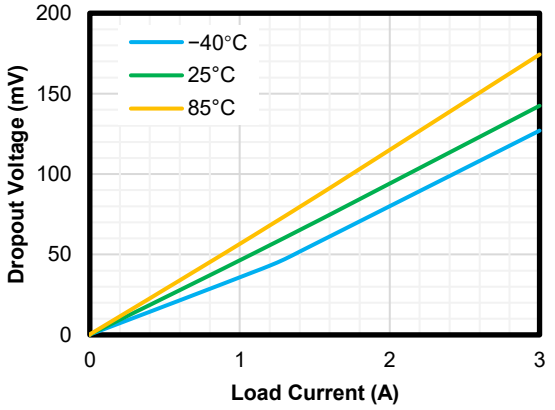
C_{OUT} = 47µF // 10µF // 10µF, $C_{NR/SS}$ =100nF, C_{FF} = open

Figure 4 PSRR vs. Frequency and VOUT



V_{IN} = 1.1 V

Figure 5 Dropout Voltage vs. IOUT

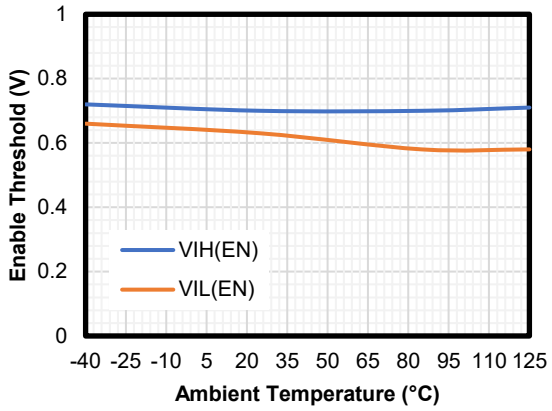


V_{IN} = 5.5 V

Figure 6 Dropout Voltage vs. IOUT

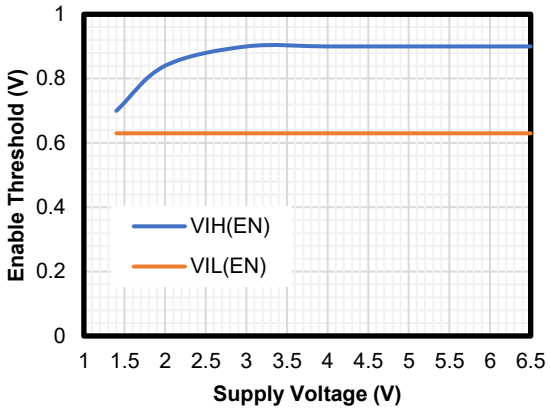
Typical Performance Characteristics (continued)

T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 k Ω to OUT, unless otherwise noted.



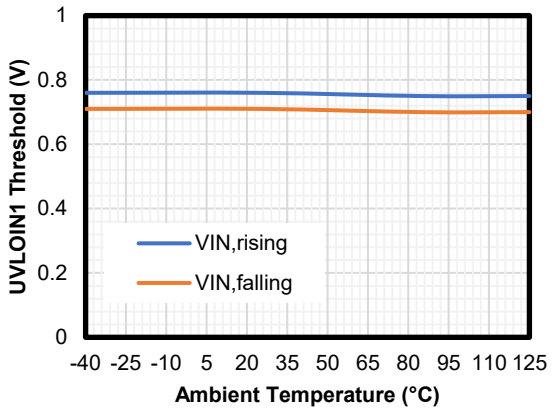
V_{IN} = 1.4 V, VBIAS = open, V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 7 Enable Threshold vs Temperature



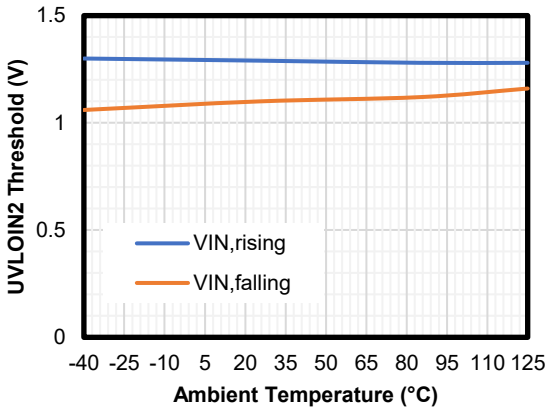
VBIAS = open, V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 8 Enable Threshold vs Input Voltage



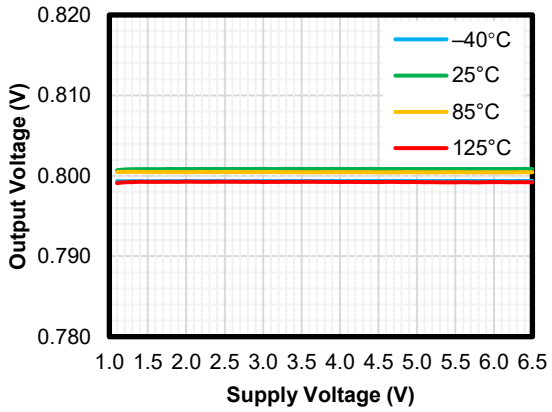
VBIAS = 3 V, V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 9 UVLOIN1 vs. Temperature



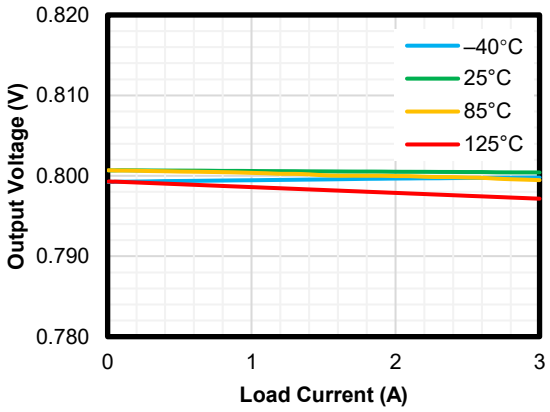
VBIAS = open, V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 10 UVLOIN2 vs. Temperature



VBIAS = 3 V, V_{OUT} = 0.8 V, I_{OUT} = 5 mA

Figure 11 Line Regulation



V_{IN} = 1.1 V, VBIAS = 3 V, V_{OUT} = 0.8 V

Figure 12 Load Regulation

Detailed Description

Overview

The TPL930 series products are 3-A high-current, 6-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with typically 145-mV ultra-low dropout voltage. The TPL930 series products support both fixed output voltage ranges from 0.8 V to 3.95 V and adjustable output voltage ranges from 0.8 V to 5.2 V with external resistor divider.

Ultra-low noise, high PSRR, and high output current capability makes the TPL930 series products ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensures the TPL930 series products optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD and DSP.

Functional Block Diagram

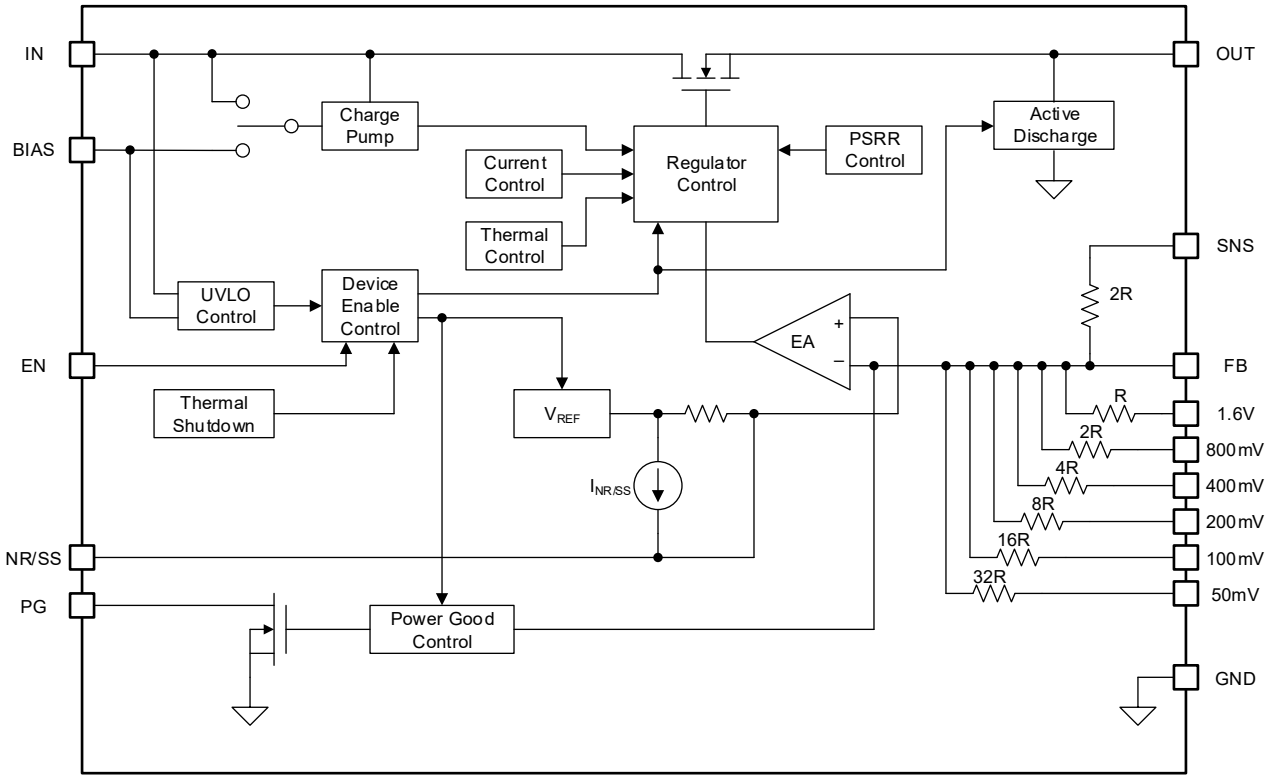


Figure 13 Functional Block Diagram

Feature Description

Enable (EN)

The TPL930 series provide a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the V_{EN} voltage falls below $V_{IL(EN)}$, the LDO device turns off, and when the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

Under-Voltage Lockout (UVLO)

The TPL930 series use an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly.

Voltage Regulation

The TPL930 series provide two options to set the output voltage: fixed output voltage by the programming pins or adjustable the output voltage by external resistors.

- ## Fixed Output Voltage Setting

The TPL930 series integrate resistor divider internally to set the fixed output voltage. The fixed output voltage can be set from 0.8V to 3.95V by connecting the output voltage setting pins (pin 5 to pin 11) to ground or left them open. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{NR/SS} + V_{Pin\_Settings} \quad (1)$$

Table 1 provides a full list of different output voltage target and the corresponding pin settings.

Table 1 Fixed Output Voltage Setting

V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V		V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
Pin	5	6	7	9	10	11		Pin	5	6	7	9	10	11
0.80	Open	Open	Open	Open	Open	Open		2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open		2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open		2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open		2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open		2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open		2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open		2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open		2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open		2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open		2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open		2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open		2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open		3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open		3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open		3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open		3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open		3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open		3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open		3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open		3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open		3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open		3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open		3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open		3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open		3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open		3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open		3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open		3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open		3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open		3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open		3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open		3.95	GND	GND	GND	GND	GND	GND

- ## Adjustable Output Voltage Setting

The TPL930 series also provide an adjustable output voltage option. Using external resistors divider, the output voltage of TPL930 series is determined by the value of the resistor R1 and R2 in Figure 14. Use Equation 2 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Where the feedback voltage V_{FB} is 0.8 V.

Table 2 provides a list of recommended resistor combinations to achieve the common output voltage values.

Table 2 External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.80	0	Open	0.800
0.81	2	160	0.810
0.82	4.02	160	0.820
0.83	6.04	160	0.830
0.84	8.06	160	0.840
0.85	10	160	0.850
0.86	12	160	0.860
0.87	12.4	143	0.869
0.88	12.4	124	0.880
0.89	12	107	0.890
0.90	12.4	100	0.899
0.95	12.4	66.5	0.949
1.00	12.4	49.9	0.999
1.10	12.4	33.2	1.099
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.792
1.90	12.1	8.87	1.891
2.50	12.4	5.9	2.481
2.85	12.1	4.75	2.838
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324
3.60	12.1	3.48	3.582
4.50	11.8	2.55	4.502
5.00	12.4	2.37	4.986

Programmable Soft Start

The TPL930 series integrate a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin (CNR/SS), the output start-up time can be can calculated with Equation 3.

$$t_{Start-up} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (3)$$

Where:

- the typical value of $V_{NR/SS}$ is 0.8V
- the typical value of $I_{NR/SS}$ is 7.2uA
- $C_{NR/SS}$ is the external capacitor at the NR/SS pin

Charge Pump Noise

The TPL930 series integrate a charge pump to improve the PSRR and transient response under low input voltage conditions and it generates a minimal amount of noise at the frequency around 15 MHz. It is recommended to use 10-nF to 100-nF bypass capacitors close to the load a ferrite bead between the LDO output and the load input capacitors forms a pi-filter to reduce the high-frequency noise level.

Power Good (PG)

The TPL930 series integrate an open-drain output power good indicator. Connect PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if power good function is used, or left PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reached the power good threshold $V_{PG,TH}$. When output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to high voltage level to indicate the output voltage is ready.

Output Active Discharge

The TPL930 series integrate an output discharge path from OUT to GND. When the device is disabled, either EN or VIN is lower than turn-on threshold, the output will actively discharge the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through internal power MOSFET can permanently damage the device, and external current protection is essential at this condition.

Over-Current Protection and Short-to-Ground Protection

The TPL930 series integrate an internal current limit that helps to protect the device during fault conditions.

- When the output is pulled down below the target output voltage, over-current protection starts to work and limit the output current to a typical value of 4.5 A.
- When the output is shorted to ground directly, short-to-ground protection starts to work and limit the output current to I_{SC}.

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause the over temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is –40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term using.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL930 series products are 3-A high-current, 6-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with typically 145-mV ultra-low dropout voltage. The following application schematic shows a typical usage of the TPL930 series.

Typical Application

Adjustable Output Operation

Figure 14 shows a typical application schematic of the TPL930 series with adjustable output operation. Refer to section *Adjustable Output Voltage Setting* to set the output voltage.

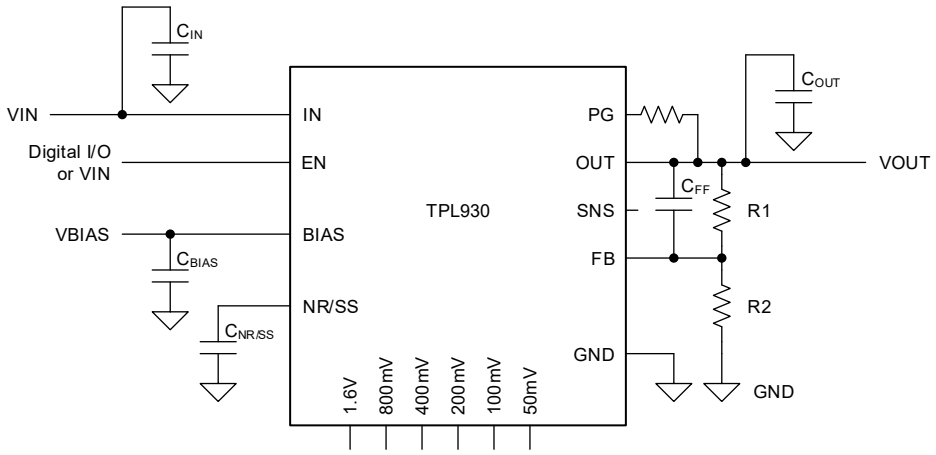


Figure 14 Adjustable Output Operation

Fixed Output Operation

Figure 15 shows a typical application schematic of the TPL930 series with fixed output operation. Refer to section *Fixed Output Voltage Setting* to set the output voltage. In this example, output voltage is set to 1.8 V ($V_{NR/SS}$ +0.8 V + 0.2 V).

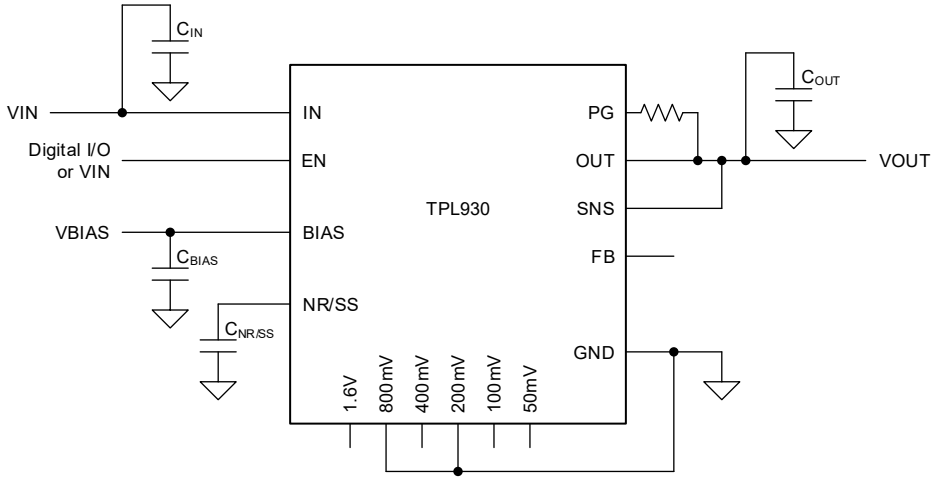


Figure 15 Fixed 1.8V Output Voltage Operation

Input Capacitor and Output Capacitor

The TPL930 series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature.

3PEAK recommends adding a 10 μF or greater capacitor with a 0.1 μF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL930 series requires an output capacitor with a minimum effective capacitance value of 22 μF. 3PEAK recommends selecting a X7R-type 47-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 4.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

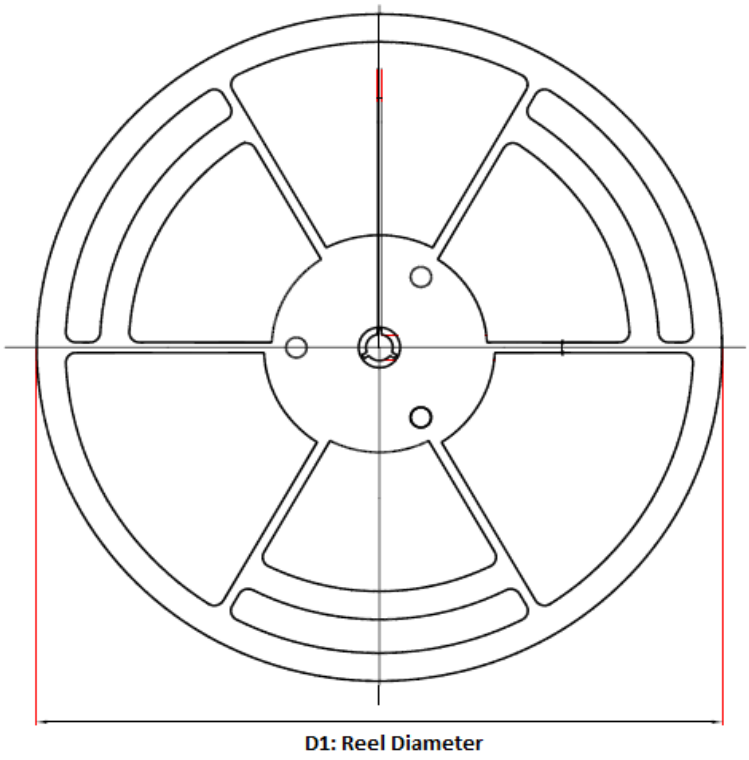
The junction temperature can be estimated using Equation 5. θ_{JA} is the junction-to-ambient thermal resistance.

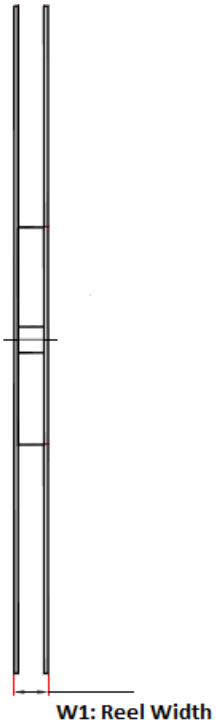
$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

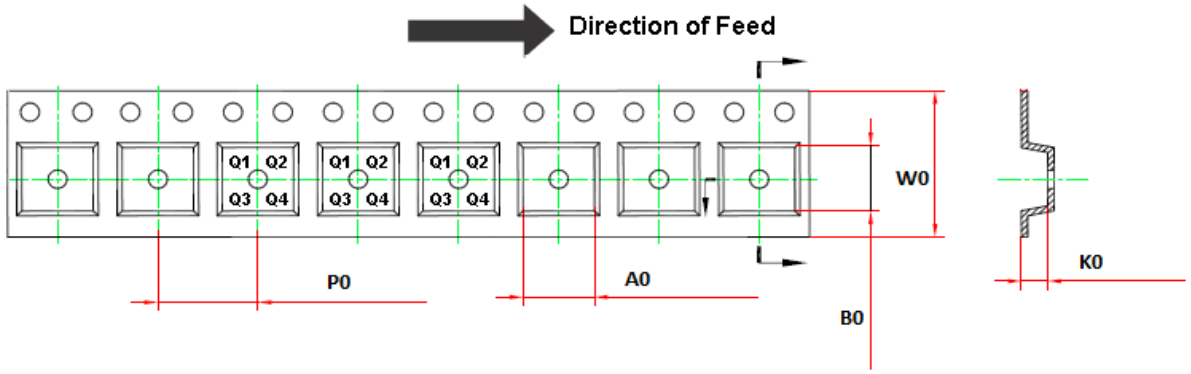
Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible, and vias between capacitors and device power pins must be avoid.
- It is recommended to bypass the input pin to ground with a 0.1 μF bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Tape and Reel Information



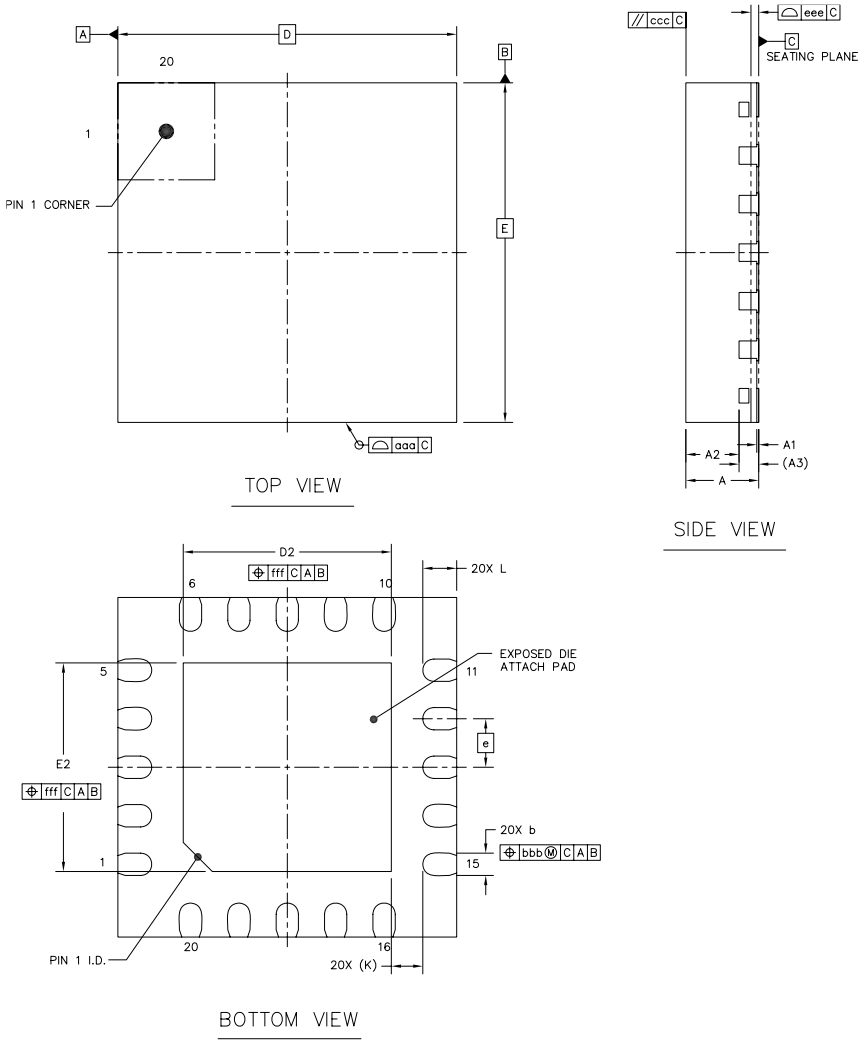




Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPL930ADJ-QF6R	3.5×3.5 QFN-20	330	17.6	3.80	3.80	1.1	8.0	12.0	Q2

Package Outline Dimensions

3.5×3.5 QFN-20



		SYMBOL	MIN	NOM	MAX
Total Thickness		A	0.7	0.8	1
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	---	0.70	---
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.18	0.23	0.30
Body Size	X	D	3.4	3.5	3.6
	Y	E	3.4	3.5	3.6
Lead Pitch		e	0.5 BCS		
EP Size	X	D2	1.95	2.05	2.15
	Y	E2	1.95	2.05	2.15
Lead Length		L	0.35	0.40	0.45
Lead Tip to Exposed Pad Edge		K	0.275	0.325	0.375
Package Edge Tolerance		aaa	0.1		
Mold Flatness		ccc	0.1		
Coplanarity		eee	0.08		
Lead Offset		bbb	0.1		
Exposed Pad Offset		fff	0.1		