

## Features

- Single-Channel Isolated Gate Driver with Optocoupler-Compatible Input
- 4.5-A Source/5-A Sink Peak Output Current with Rail-to-Rail Output
- 14-V to 40-V Output Driver Supply Voltage
- 8-V and 12-V  $V_{CC}$  UVLO Options
- 5.7-V Reverse Polarity Voltage Handling Capability on Input Stage
- Ultra-Fast Output Driving
  - 105-ns Propagation Delay
  - 25-ns Delay Matching
  - 35-ns Pulse Width Distortion
- 5.7-kV<sub>RMS</sub> Reinforced Isolation Rating
- $\pm 150$ -kV/ $\mu$ s Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP6 Package
- Operating Ambient Temperature  $T_A$   $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN EN IEC 60747-17 (VDE 0884-17):2021
  - 5.7-kV<sub>RMS</sub> Isolation Rating per UL 1577
  - CSA Component Acceptance Service Notice 5A
  - CQC Certification per GB 4943.1-2022

## Applications

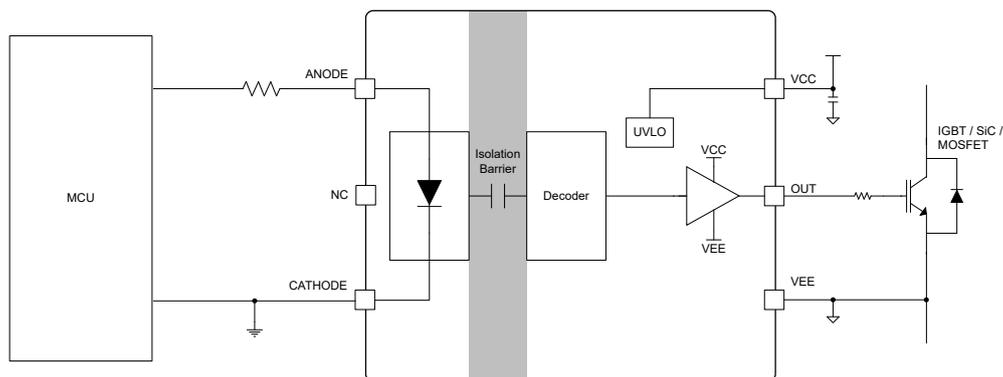
- Industrial Motor-Control Drives
- Industrial Power Supplies, UPS
- Solar Inverters
- Induction Heating

## Description

The TPM23513 driver is a single-channel isolated gate driver for IGBTs, MOSFETs, and SiC MOSFETs. Its input is optocoupler compatible with the industrial standard wide-body WSOP6 package. Its driving capability can support a 4.5-A source and 5-A sink current. The output stage can withstand high voltages up to 40 V and supports the latest generation of IGBT and SiC-based applications.

The TPM23513 device provides high electromagnetic immunity and low emissions at low power consumption. Its isolation channel is separated by a double-capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. 3PEAK proprietary galvanic isolation technology supports 150 kV/ $\mu$ s common-mode transient immunity (CMTI), which is critical especially for SiC applications. The TPM23513 input stage emulates an opto-diode with enhanced noise immunity. Its enhanced reliability can support high-power industrial applications.

## Typical Application Circuit



## Table of Contents

<b>Features</b> .....	<b>1</b>
<b>Applications</b> .....	<b>1</b>
<b>Description</b> .....	<b>1</b>
<b>Typical Application Circuit</b> .....	<b>1</b>
<b>Product Family Table</b> .....	<b>3</b>
<b>Revision History</b> .....	<b>3</b>
<b>Pin Configuration and Functions</b> .....	<b>4</b>
<b>Specifications</b> .....	<b>5</b>
Absolute Maximum Ratings <sup>(1)</sup> .....	5
ESD, Electrostatic Discharge Protection.....	5
Recommended Operating Conditions.....	5
Thermal Information.....	6
Safety Limiting Values.....	6
Insulation Specifications.....	7
Electrical Characteristics.....	8
Timing Characteristics.....	9
Parameter Measurement.....	9
Typical Performance Characteristics.....	12
<b>Detailed Description</b> .....	<b>14</b>
Overview.....	14
Functional Block Diagram.....	14
Feature Description.....	15
<b>Application and Implementation</b> .....	<b>16</b>
Typical Application .....	16
<b>Layout</b> .....	<b>18</b>
Layout Guideline.....	18
Layout Recommendations.....	18
<b>Tape and Reel Information</b> .....	<b>19</b>
<b>Package Outline Dimensions</b> .....	<b>20</b>
WSOP6.....	20
<b>Order Information</b> .....	<b>21</b>
<b>IMPORTANT NOTICE AND DISCLAIMER</b> .....	<b>22</b>

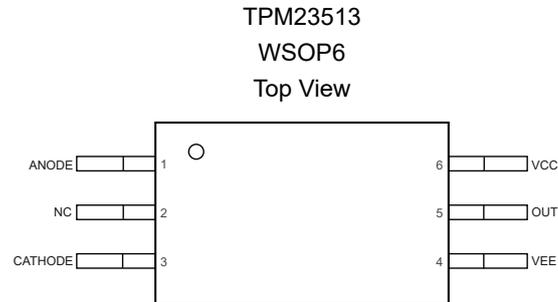
## Product Family Table

Order Number	UVLO Threshold (V)	Package
TPM23513-SOER	12.5	WSOP6
TPM23513B-SOER	8.5	WSOP6
TPM23513-SOER-S	12.5	WSOP6

## Revision History

Date	Revision	Notes
2023-12-04	Rev A.0	Initial release
2024-05-15	Rev A.1	Updated MSL Level and Isolation Parameters
2024-09-30	Rev A.2	Updated Thermal Resistance and Isolation Parameters
2025-01-17	Rev A.3	Updated Isolation Certificate, Insulation Parameters, Features, and Description
		Updated the POD format of the WSOP6.

## Pin Configuration and Functions



**Table 1. Pin Functions: TPM23513**

Pin		I/O	Description
No.	Name		
1	ANODE	I	Emulated diode anode input
2	NC	-	No Connection
3	CATHODE	O	Emulated diode cathode input
4	VEE	P	Output power ground
5	VOUT	O	Gate driver output
6	VCC	P	Output power supply

**4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver**
**Specifications**
**Absolute Maximum Ratings <sup>(1)</sup>**

Parameter		Min	Max	Unit
Input Voltage	Reverse Input Voltage, CATHODE – ANODE		8.25	V
	Average Transient Input Current, $I_{F(AVG)}$		25	mA
	Peak Transient Input Current, $I_{F(TRAN)}$		1	A
Output Voltage	Output Supply Voltage, $V_{CC} - V_{EE}$	-0.3	40	V
	$V_{OUT}$	$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
$T_J$	Maximum Junction Temperature	-40	150	°C
$T_A$	Operating Ambient Temperature Range	-40	125	°C
$T_{STG}$	Storage Temperature Range	-65	150	°C
$T_L$	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

**ESD, Electrostatic Discharge Protection**

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

**Recommended Operating Conditions**

Parameter		Min	Max	Unit
$V_{CC} - V_{EE}$	Output Supply Voltage (TPM23513 12V UVLO)	14	40	V
$V_{CC} - V_{EE}$	Output Supply Voltage (TPM23513B 8V UVLO)	10	40	V
$V_{OUT}$	Output Voltage	$V_{EE}$	$V_{CC}$	V
$I_{F(ON)}$	Input Diode Forward Current, on-state	7	16	mA
$V_{F(OFF)}$	Input Diode Forward Voltage, off-state	-6	0.9	V
$T_J$	Junction Temperature	-40	150	°C
$T_A$	Operating Ambient Temperature	-40	125	°C

**Thermal Information**

Package	$\theta_{JA}$	$\theta_{JB}$	$\theta_{JC-top}$	Unit
WSOP6	117.19	61.67	53.95	$^{\circ}\text{C}/\text{W}$

**Safety Limiting Values**

Parameter	Test Conditions	Min	Typ	Max	Unit
$I_s$	Safety input, output, or supply current			50	mA
				25	
$P_s$	Safety input, output, or total power			750	mW
$T_s$	Maximum safety temperature			150	$^{\circ}\text{C}$

**4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver**
**Insulation Specifications**

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8.5	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8.5	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 22	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification	For Rated Mains Voltage ≤ 300 V <sub>RMS</sub>	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C <sub>IO</sub>	Isolation Capacitance	V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz	0.5	pF
R <sub>IO</sub>	Isolation Resistance	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25 °C	> 10 <sup>9</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125 °C	> 10 <sup>10</sup>	
		V <sub>IO</sub> = 500 V, T <sub>A</sub> = 150 °C	> 10 <sup>11</sup>	
V <sub>IORM</sub>	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum Working Isolation Voltage	AC voltage; TDDb Test	1060	V <sub>RMS</sub>
		DC voltage	1500	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum Transient Isolation Voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification);	8000	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.3 × V <sub>IOSM</sub> (qualification) = 11700v	9000	V <sub>PK</sub>
V <sub>ISO</sub>	UL 1577 Withstand Isolation Voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5000 V <sub>RMS</sub> , t = 60 s (in qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> - 6000 V <sub>RMS</sub> , t = 1 s (100% in production)	5700	V <sub>RMS</sub>
q <sub>pd</sub>	Apparent Charge	Method a, After the Input/Output safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

**4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver**
**Electrical Characteristics**

All test conditions:  $V_{CC} - V_{EE} = 14$  to  $40$  V,  $V_{EE}$  referred as GND,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted.

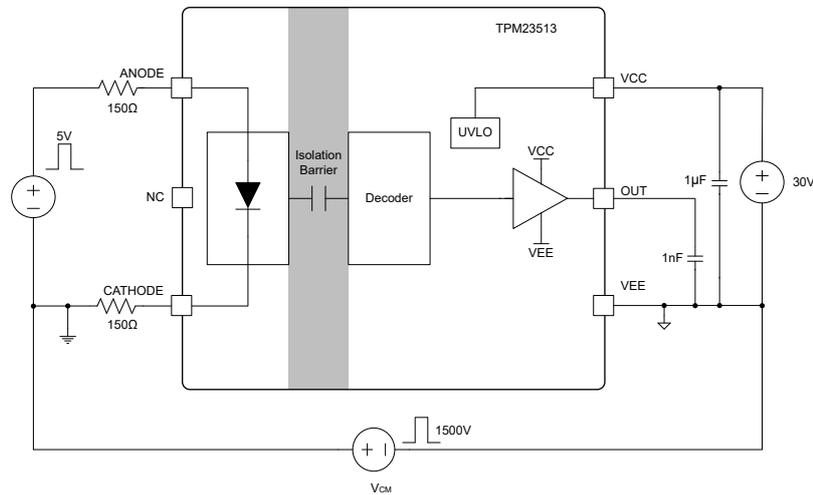
Parameter		Conditions	Min	Typ	Max	Unit
<b>Input</b>						
$I_{FTH\_R}$	Input Forward Threshold Current, Rising Edge	$V_{OUT} > 5$ V	1.1	3.6	4.8	mA
$V_F$	Input Forward Voltage	$I_F = 10$ mA	1.8	2.05	2.4	V
$V_{FTH\_F}$	Input Threshold Voltage, falling edge	$V_{OUT} < 5$ V	0.9	1.4	1.9	V
$\Delta V_F/\Delta T$	Input Forward Voltage, Temperature Coefficient	$I_F = 10$ mA		0.9		mV/ $^\circ\text{C}$
$V_R$	Input Reverse Breakdown Voltage	$I_R = 10$ $\mu\text{A}$	8.25			V
$C_{IN}$	Input Parasitic Capacitance	$F = 0.5$ MHz		15		pF
<b>Output</b>						
$I_{OH}$	Output Source Peak Current <sup>(1)</sup>	$I_F = 10$ mA, $V_{CC} = 15$ V, $C_{LOAD} = 0.18$ $\mu\text{F}$ , $V_{CC} = 0.18$ $\mu\text{F}$ , $t_{pw} < 10$ $\mu\text{s}$		4.5		A
$I_{OL}$	Output Sink Peak Current <sup>(1)</sup>	$I_F = 10$ mA, $V_{CC} = 15$ V, $C_{LOAD} = 0.18$ $\mu\text{F}$ , $V_{CC} = 0.18$ $\mu\text{F}$ , $t_{pw} < 10$ $\mu\text{s}$		5		A
$V_{OH}$	Output Voltage, $V_{CC} - V_{OUT}$	OUT = H, $I_{OUT} = -20$ mA	70	180	360	mV
$V_{OL}$	Output Voltage, $V_{OUT} - V_{EE}$	OUT = L, $I_{OUT} = 20$ mA		12	25	mV
$I_{CC\_H}$	Output Quiescent Current, OUT = H	OUT = H, $I_{OUT} = 0$ mA	0.8	1.53	2.4	mA
$I_{CC\_L}$	Output Quiescent Current, OUT = L	OUT = L, $I_{OUT} = 0$ mA	0.8	1.50	2.4	mA
<b>Under Voltage Lockout, TPM23513 (12-V UVLO Version)</b>						
$V_{UVLO\_R}$	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	11	12.5	13.9	V
$V_{UVLO\_F}$	Under Voltage Lock-out Threshold, Falling Edge		10	11.5	12.9	V
$V_{UVLO\_HYS}$	UVLO Hysteresis			1		V
<b>Under Voltage Lockout, TPM23513B (8-V UVLO Version)</b>						
$V_{UVLO\_R}$	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	7.8	8.95	9.8	V
$V_{UVLO\_F}$	Under Voltage Lock-out Threshold, Falling Edge		7.05	8.35	9.2	V
$V_{UVLO\_HYS}$	UVLO Hysteresis			0.57		V

(1) Guaranteed by design

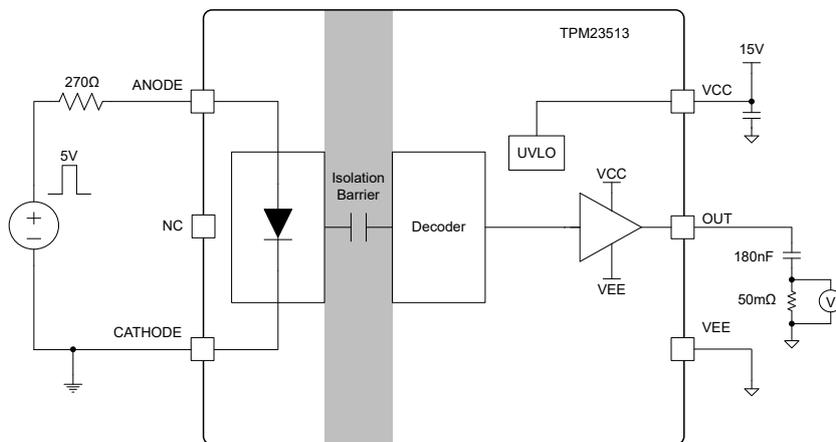
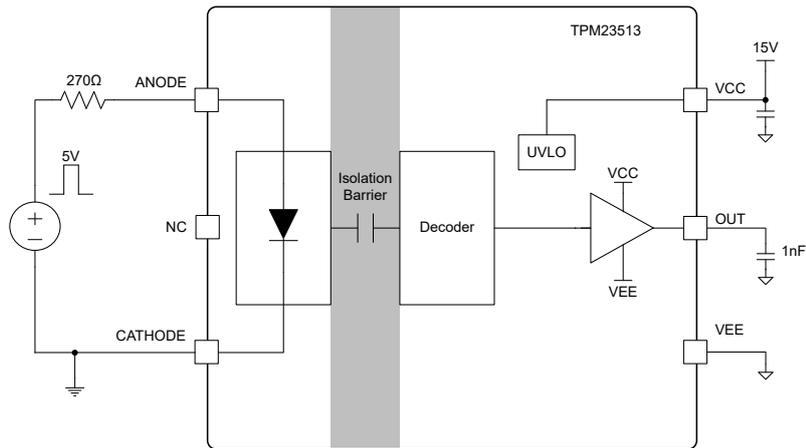
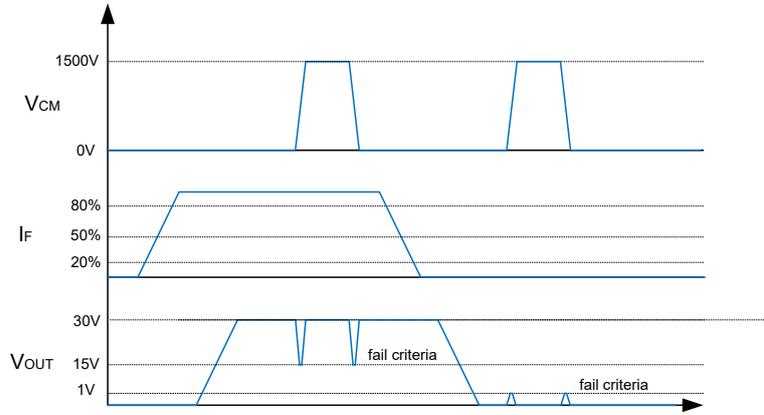
**4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver**
**Timing Characteristics**

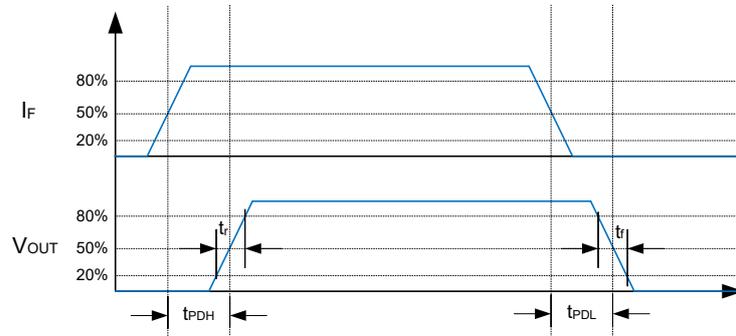
Parameter		Test Conditions	Min	Typ	Max	Unit
$t_r$	Output Rise Time <sup>(1)</sup>	$F_{SW} = 20 \text{ kHz, (50\% Duty Cycle)}$ $V_{CC} = 15 \text{ V}$		8.2	28	ns
$t_f$	Output Fall Time <sup>(1)</sup>			6.5	25	ns
$t_{PLH}$	Propagation Delay, Low to High			54.9	105	ns
$t_{PHL}$	Propagation Delay, High to Low			47.4	105	ns
$t_{PWD}$	Pulse Width Distortion [ $t_{PHL} - t_{PLH}$ ]			-35	9.35	35
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay between any Two Parts <sup>(1)</sup>	$F_{SW} = 20 \text{ kHz, (50\% Duty Cycle)}$ $V_{CC} = 15 \text{ V, } I_F = 10 \text{ mA}$			25	ns
$t_{UVLO\_rec}$	UVLO Recovery Delay	$V_{CC}$ Rising from 0 V to 15 V		28.8	47	$\mu\text{s}$
$CMT_{IH}$	Common-mode Transient Immunity (Output High) <sup>(1)</sup>	$I_F = 10 \text{ mA, } V_{CM} = 1500 \text{ V, } V_{CC} = 30 \text{ V, } T_A = 25 \text{ }^\circ\text{C}$	150			$\text{kV}/\mu\text{s}$
$CMT_{IL}$	Common-mode Transient Immunity (Output Low) <sup>(1)</sup>	$V_F = 0 \text{ V, } V_{CM} = 1500 \text{ V, } V_{CC} = 30 \text{ V, } T_A = 25 \text{ }^\circ\text{C}$	150			$\text{kV}/\mu\text{s}$

(1) Guaranteed by design

**Parameter Measurement**
**Driver Parameter**


4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver



**4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver**

Typical Performance Characteristics

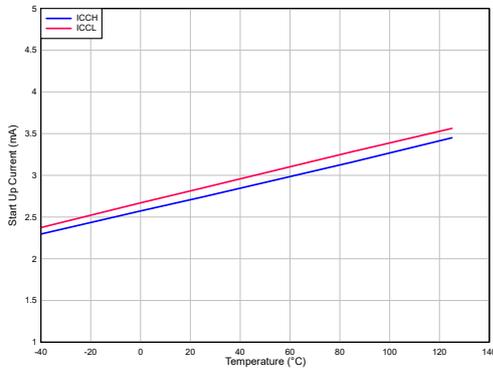


Figure 1. Start-up Current vs. Temperature

V<sub>CC</sub> = 15 V

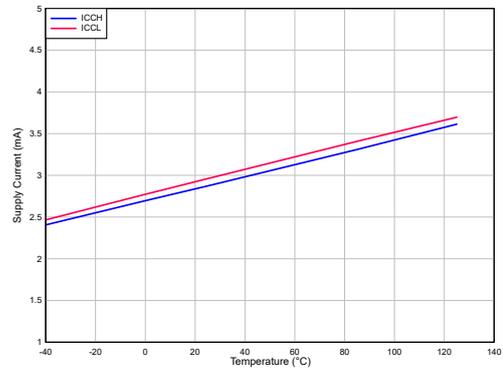


Figure 2. Start-up Current vs. Temperature

V<sub>CC</sub> = 30 V

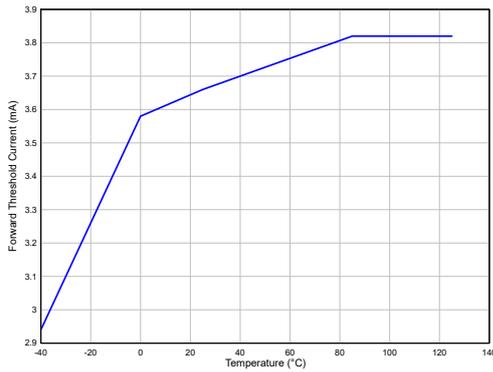


Figure 3. Forward Threshold Current vs. Temperature

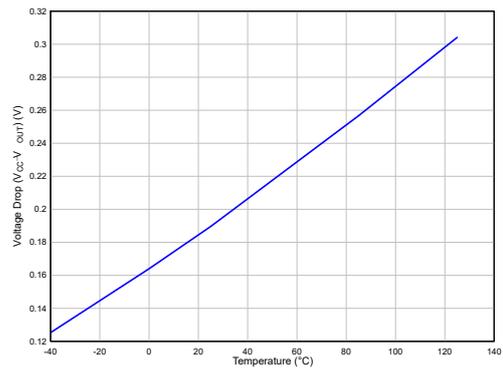


Figure 4. VOH Voltage Drop vs. Temperature

I<sub>OUT</sub> = 20mA

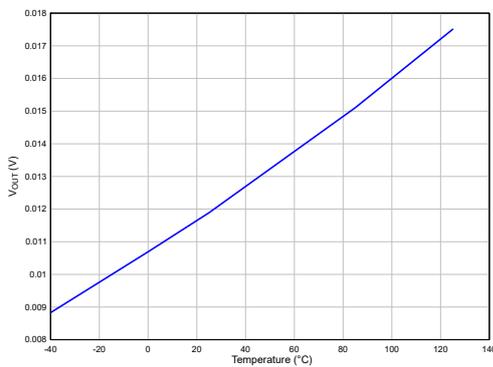


Figure 5. VOL Voltage Drop vs. Temperature

I<sub>OUT</sub> = -20 mA

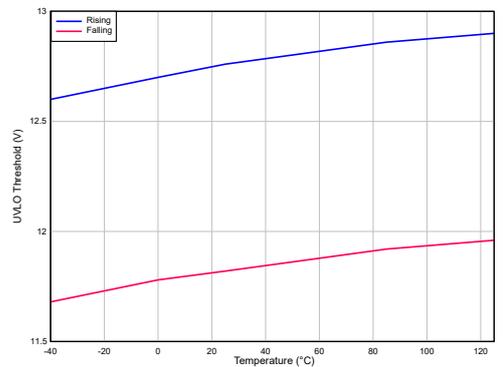


Figure 6. UVLO Threshold vs. Temperature

12-V UVLO Version

4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver

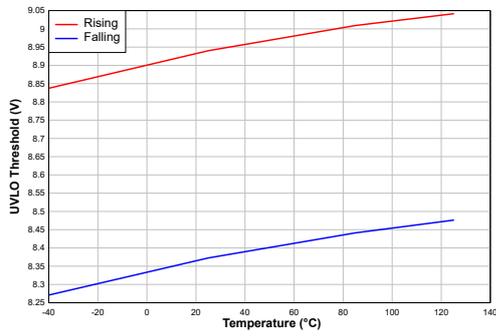


Figure 7. UVLO Threshold vs. Temperature  
8-V UVLO Version

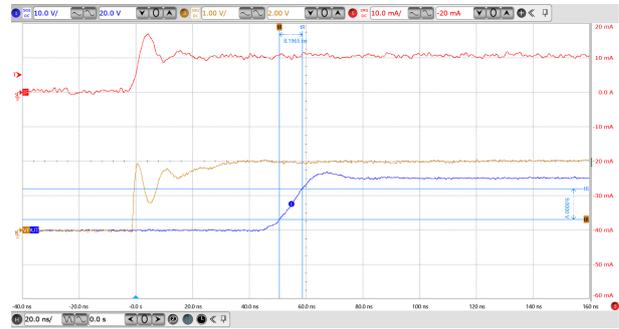


Figure 8. Output Rising Edge



Figure 9. Output Falling Edge

## Detailed Description

### Overview

The TPM23513 is a single-channel isolated gate driver for MOSFETs, IGBTs, and SiC FETs with an optocoupler compatible input stage which is an emulated diode. It has a 40-V maximum operating driver voltage, which is especially suitable for high-power fast-transient IGBT / SiC applications.

The TPM23513 is designed to replace the optocoupler gate driver with industry-standard wide-body 6-pin package WSOP6, with more than 8.5-mm creepage and clearance to withstand over 1060- $V_{RMS}$  working voltage, reinforced isolation, and 5.7-k $V_{RMS}$  for 60s and a surge rating of 8-k  $V_{PK}$ . 3PEAK proprietary isolation technology supports common-mode transient immunity of greater than 150 kV/ $\mu$ s.

### Functional Block Diagram

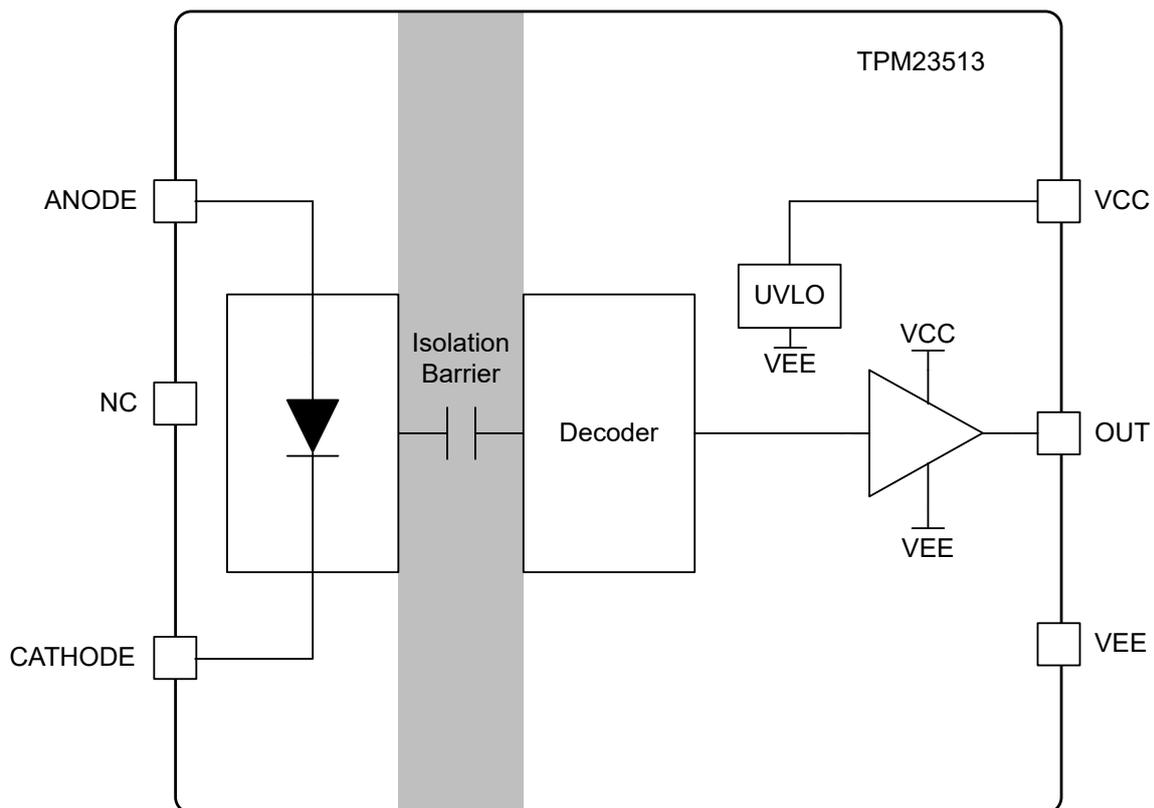


Figure 10. Functional Block Diagram

## Feature Description

### Emulated Diode Input

The input stage of TPM23513 is an emulated diode input to be pin-to-pin compatible with optocoupler input. Working like an opto-diode, when the current flows from ANODE and CATHODE, the forward voltage drop between ANODE and CATHODE is typical 2.1 V. An external resistor can be placed on the ANODE side or the CATHODE side or both to limit the current. 3PEAK recommends that the forward current should be from 7 mA to 30 mA. When the input current is higher than the threshold current  $I_{FTH\_R}$ , the TPM23513 internal isolation transmitter starts to send CMTI-optimized high-frequency On-Off-Keying (OOK) signals through the double-capacitive silicon dioxide ( $\text{SiO}_2$ ) isolation layer. 3PEAK proprietary isolation technology provides high CMTI performance against fast  $dV/dt$  scenarios, which is especially useful for latest-generation applications like SiC FETs.

### Decoder & Output Stage

The high-frequency signal is converted by the decoder via double-capacitive insulation barrier as the output stage's input. The rail-to-rail output stage provides a high-peak current during the output slewing. The output  $V_{CC}$  supports a maximum 40-V input.

The TPM23513 output stage is able to deliver high current sourcing up to 4.5 A and sinking up to 5.5 A with low propagation delay.

### Protection

#### Under-Voltage Lock Out (UVLO)

The device has a UVLO feature to monitor voltage between  $V_{CC}$  and  $V_{EE}$  to prevent under-driven working conditions. When  $V_{CC}$  rises above the UVLO rising threshold, the output follows the device input; when  $V_{CC}$  falls below the UVLO falling threshold longer than the deglitch timer, the device gets into UVLO protection and holds output low. The UVLO has a hysteresis of  $UVLO_{HYS}$  to prevent power supply noises during switching.

3PEAK provides 2 UVLO options, 12-V UVLO option TPM23513 and 8-V UVLO option TPM23513B.

#### Active Pulldown

The output stage has an under-voltage lock-out feature to protect the output driver from malfunction during low-voltage operation. When  $V_{CC}$  is lower than the UVLO threshold, the output will be driven low. When  $V_{CC}$  is higher than the UVLO threshold, the output will be operated according to the input bias state. When  $V_{CC}$  is unbiased, the output will be pulled lower to 2 V to avoid false turning on.

#### Short Circuit Clamping

The device has a short-circuit clamping feature to clamp driver output voltage and protect IGBT/MOSFET gate from over-voltage breakdown or degradation. The short-circuit can withstand 500 mA for 10  $\mu\text{s}$  and a continuous current of 20 mA. In case higher current conduction is required, 3PEAK recommends to use external Schottky diodes in parallel.

## Application and Implementation

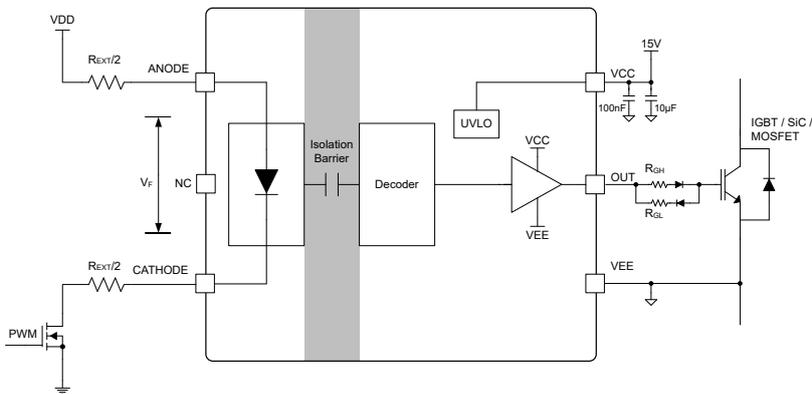
### Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

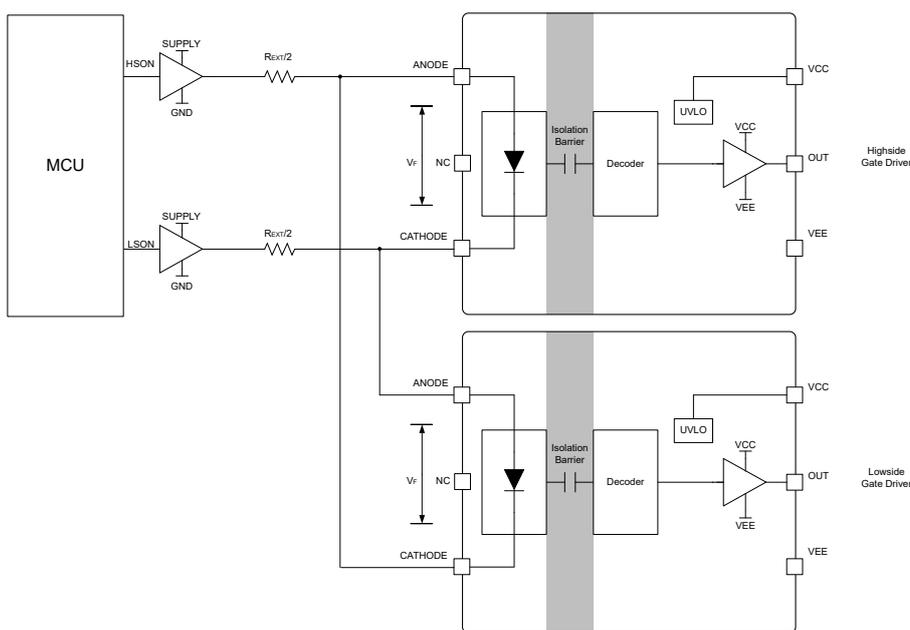
## Typical Application

The TPM23513 supports pin-to-pin replacement of common opto-coupler-based gate drivers. Serial resistor is added to the input path to limit current between 7 mA and 25 mA.

### Low-side NMOS Driving Stage



### Half-bridge Driver with Interlock



---

## 4.5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver

For most half-bridge driver applications, 2 pcs of TPM23513 can be used with MCU interlock feature, and prevent shoot-through since the input will reject when LSON and HSON are both at high state or low state. The reverse input voltage between ANODE and CATHODE can be as high as SUPPLY voltage, 3PEAK recommends supply voltage be set below 5.5-V considering 6.5-V input reverse breakdown voltage.

### Input Resistor

Common MCU cannot supply large enough current to turn on the input diode. 3PEAK recommends using an NMOS FET to drive with current limiting resistors. The serial resistor is used to limit diode current as below equation, 3PEAK recommends using  $R_{EXT}$  between 200  $\Omega$  and 300  $\Omega$ .

$$R_{EXT} = \frac{V_{SUPPLY} - V_F}{I_F} - R_{BUFFER} \quad (1)$$

10- $\mu$ F VCC capacitor and 100-nF decoupling capacitor should be placed close to the device VCC node.

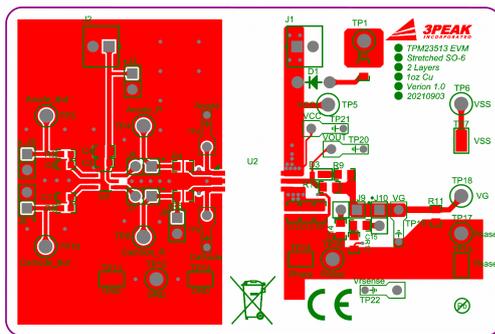
The power supply between VCC and VEE must be greater than UVLO. 3PEAK recommends 15 V and above. In case of negative shutdown voltage is needed, 3PEAK recommends separating VEE from the IGBT emitter/MOSFET source node. and tie VEE to negative voltage with reference to the IGBT emitter / MOSFET source node. Total VCC-VEE should be smaller than 40 V.

## Layout

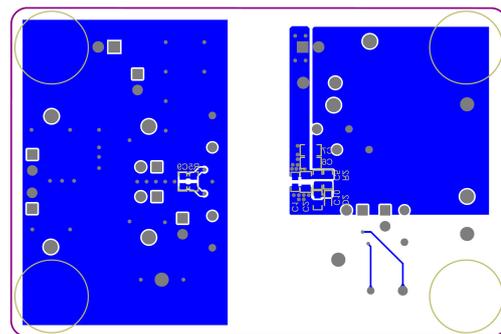
### Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- For current mode input drivers, a low ESR and ESL capacitor should be placed close to the Cathode and Anode pins.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

### Layout Recommendations

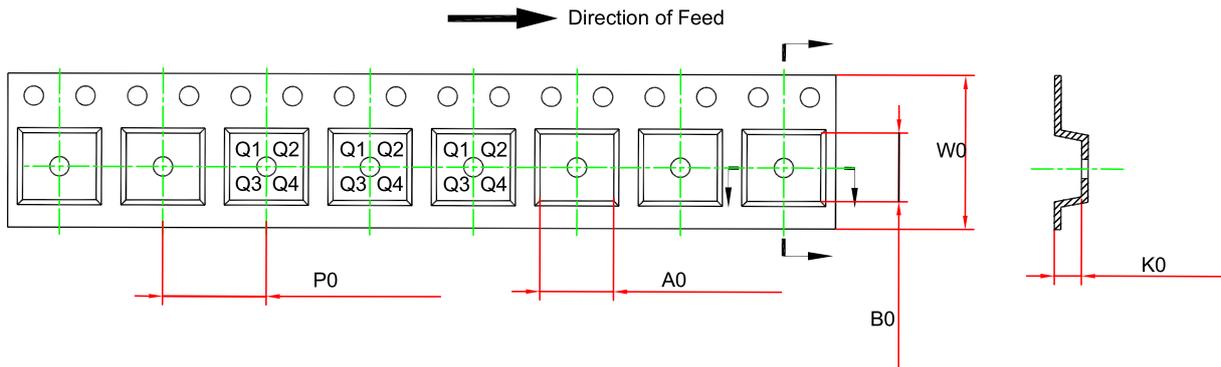
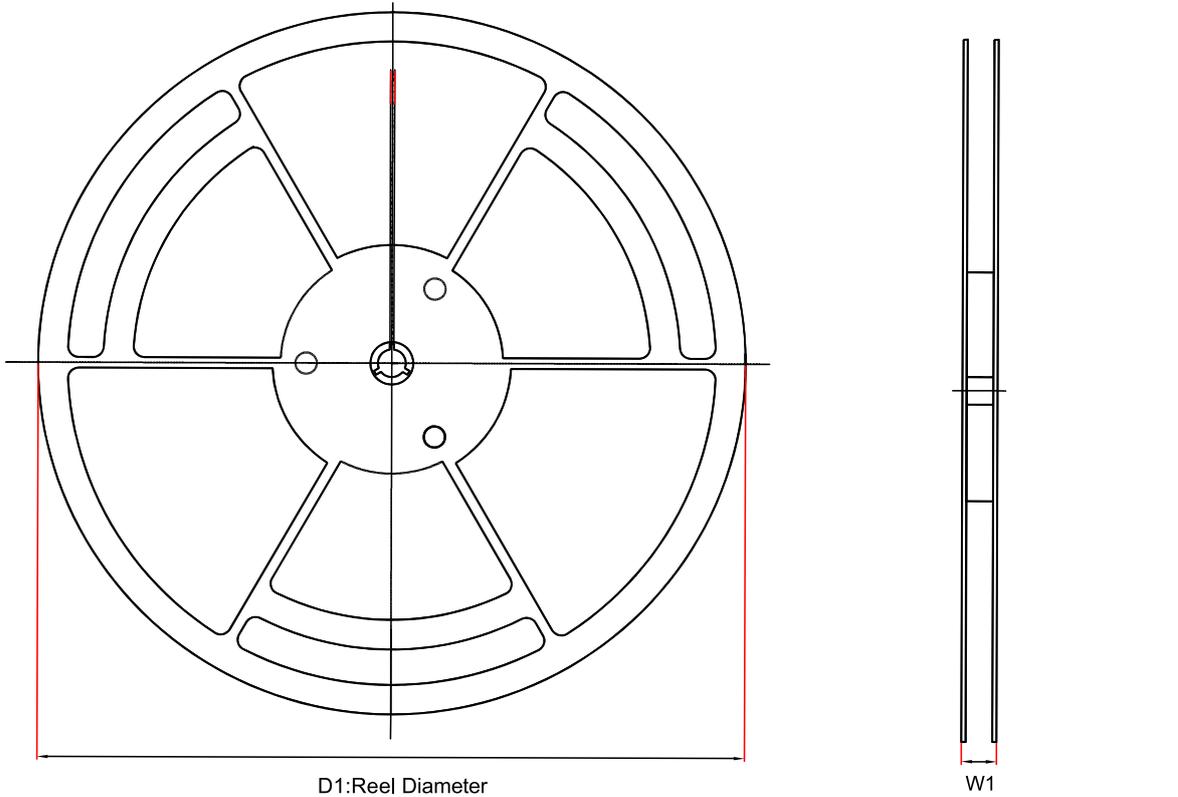


Top Layer



Bottom Layer

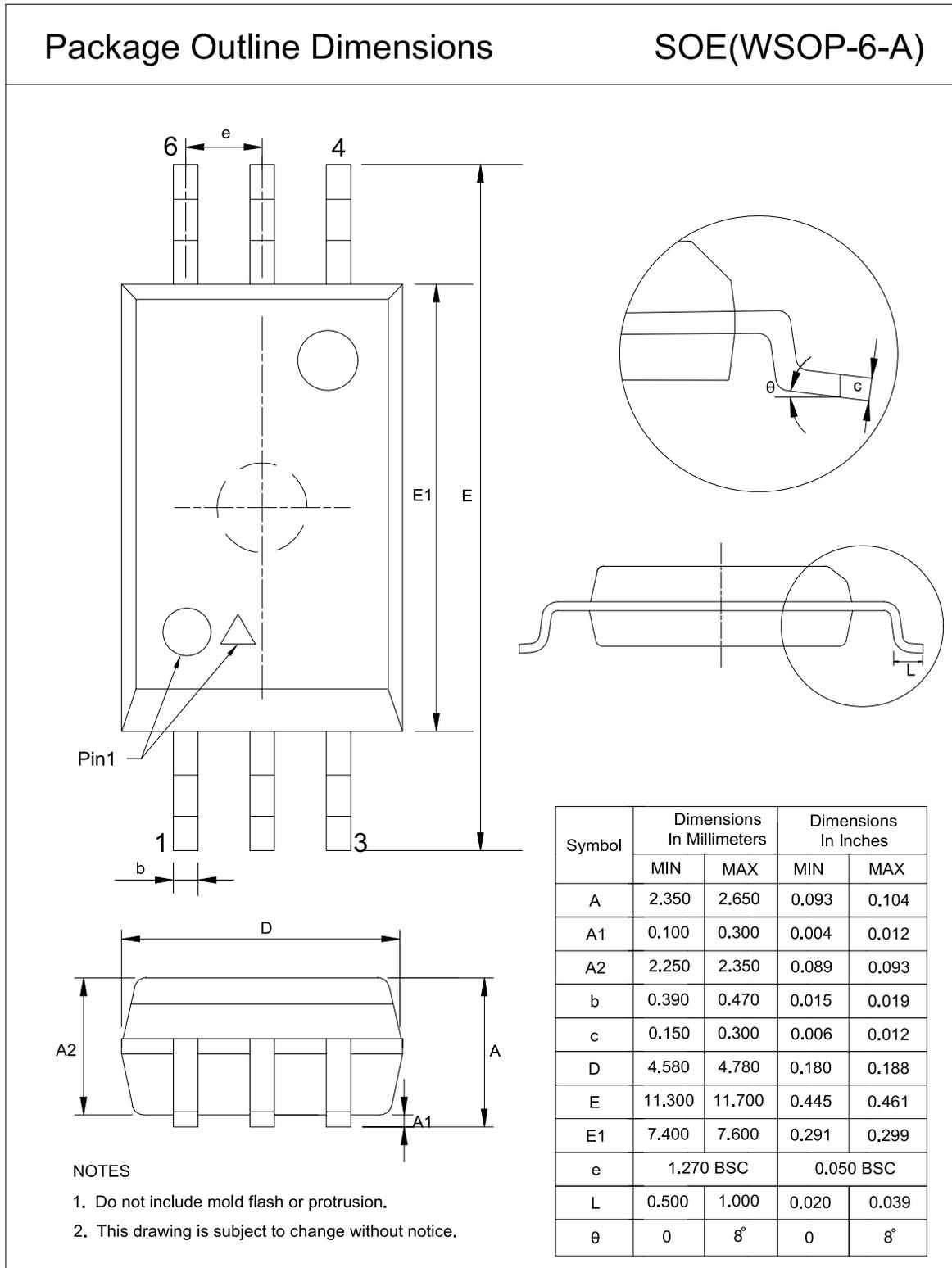
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM23513-SOER	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1
TPM23513B-SOER	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1
TPM23513-SOER-S	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1

Package Outline Dimensions

WSOP6



## Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM23513-SOER	-40 to 125°C	WSOP6	M513	3	1000	Green
TPM23513B-SOER	-40 to 125°C	WSOP6	M513B	3	1000	Green
TPM23513-SOER-S	-40 to 125°C	WSOP6	M513	3	1000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

## IMPORTANT NOTICE AND DISCLAIMER

**Copyright**© 3PEAK 2012-2025. All rights reserved.

**Trademarks.** Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

**Performance Information.** Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

**Disclaimer.** 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.