5-A/5-A, Opto-Compatible 1-CH Isolated Gate Driver

Features

- Single-Channel Isolated Gate Driver with Optocoupler-Compatible Input
- 5-A Source/5-A Sink Peak Output Current with Rail-to-Rail Output
- 14-V to 40-V Output Driver Supply Voltage
- 8-V and 12-V V_{CC} UVLO Options
- 5.7-V Reverse Polarity Voltage Handling Capability on Input Stage
- Ultra-Fast Output Driving
  - 105-ns Propagation Delay
  - 25-ns Delay Matching
  - 35-ns Pulse Width Distortion
- 5.7-kV_{RMS} Reinforced Isolation Rating
- ±150-kV/μs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP8 Package
- Operating Ambient Temperature T_A: −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN ENIEC 60747-17 (VDE 0884-17):2021
  - 5.7-kV_{RMS} Isolation Rating per UL 1577
  - CSA Component Acceptance Service Notice 5A
  - CQC Certification per GB 4943.1-2022

Description

The TPM23514x driver is a single-channel isolated gate driver family for IGBTs, MOSFETs, and SiC MOSFETs.

Its input is optocoupler compatible with the industrial standard wide-body WSOP8 package. Its driving capability can support a 5-A source and 5-A sink current. The output stage can withstand high voltages up to 40 V and supports the latest generation of IGBT and SiC-based applications.

The TPM23514x device provides high electromagnetic immunity and low emissions at low power consumption. Its isolation channel is separated by a double-capacitive silicon dioxide (SiO2) insulation barrier. 3PEAK proprietary galvanic isolation technology supports 150kV/μs common-mode transient immunity (CMTI), which is especially critical for SiC applications. The TPM23514x input stage emulates an opto-diode with enhanced noise immunity. Its enhanced reliability can support high-power industrial applications.

The TPM23514D option provides a desaturation protection feature from IGBT/SiC over-current protection. The TPM23514S option provides a split output feature to configure rise/fall time separately. The TPM23514M option provides an internal miller clamp feature to prevent false turn-on coupled by fast slewing outputs. The TPM23514V option provides a single output pin option.

Applications

- Industrial Motor-Control Drives
- Industrial Power Supplies, UPS
- Solar Inverters
- Induction Heating

Typical Application Circuit

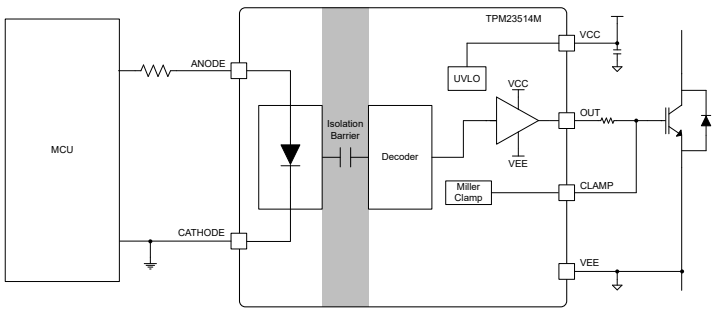


Table of Contents

Product Family Table

Order Number	Feature	UVLO
TPM23514D	Desaturation Protection	12
TPM23514M	Miller Clamp	12
TPM23514BM	Miller Clamp	8
TPM23514S	Split Output	12
TPM23514BS	Split Output	8
TPM23514V	Single VOUT Pin	12

Revision History

Date	Revision	Notes
2024-05-15	Rev A.0	Initial release
2024-07-04	Rev A.1	Corrected TPM23514D Pinout
2025-01-20	Rev A.2	Updated safety-related certifications, Features, and Description

Pin Configuration and Functions

TPM23514D
WSOP8
Top View

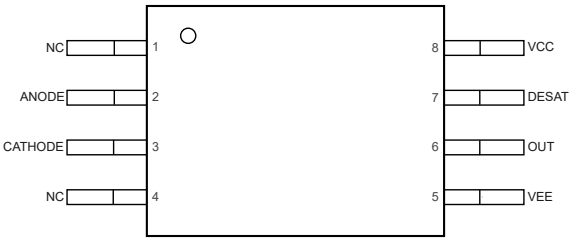


Table 1. Pin Functions: TPM23514D

Pin		I/O	Description
No.	Name		
1	NC	–	No connection
2	ANODE	I	Emulated diode anode input
3	CATHODE	O	Emulated diode cathode input
4	NC	–	No connection
5	VEE	P	Output power ground
6	OUT	O	Gate driver output
7	DESAT	I	Desaturation comparator input
8	VCC	P	Output power supply

TPM23514M
WSOP8
Top View

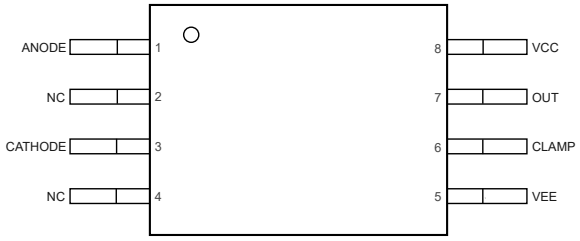


Table 2. Pin Functions: TPM23514M

Pin		I/O	Description
No.	Name		
1	ANODE	I	Emulated diode anode input
2	NC	–	No connection
3	CATHODE	O	Emulated diode cathode input
4	NC	–	No connection
5	VEE	P	Output power ground
6	CLAMP	O	Miller clamp output
7	OUT	O	Gate driver output
8	VCC	P	Output power supply

TPM23514S
WSOP8
Top View

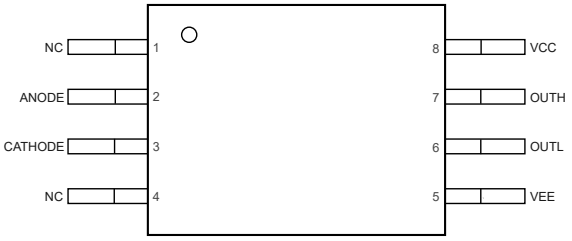


Table 3. Pin Functions: TPM23514S

Pin		I/O	Description
No.	Name		
1	NC	–	No connection
2	ANODE	I	Emulated diode anode input
3	CATHODE	O	Emulated diode cathode input
4	NC	–	No connection
5	VEE	P	Output power ground
6	OUTH	O	Gate driver output pull-up
7	OUTL	O	Gate driver output pull-down
8	VCC	P	Output power supply

TPM23514V
WSOP8
Top View

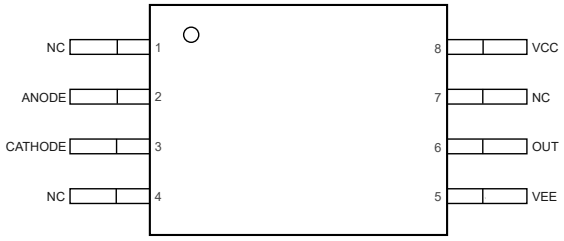


Table 4. Pin Functions: TPM23514V

Pin		I/O	Description
No.	Name		
1	NC	–	No connection
2	ANODE	I	Emulated diode anode input
3	CATHODE	O	Emulated diode cathode input
4	NC	–	No connection
5	VEE	P	Output power ground
6	OUT	O	Gate driver output
7	NC	–	No connection
8	VCC	P	Output power supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Reverse Input Voltage, CATHODE – ANODE		8.25	V
	Average Transient Input Current, $I_{F(AVG)}$		25	mA
	Peak Transient Input Current, $I_{F(TRAN)}$		1	A
Output Voltage	Output Supply Voltage, $V_{CC} - V_{EE}$	−0.3	40	V
	V_{OUT}	V_{EE} − 0.3	V_{CC} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Table 5. TPM23514M

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 6. TPM23514S, TPM23514D

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC} – V_{EE}	Output Supply Voltage (TPM23514 12V UVLO)	14	40	V
V_{CC} – V_{EE}	Output Supply Voltage (TPM23514 8V UVLO)	10	40	V
V_{OUT}	Output Voltage	V_{EE}	V_{CC}	V
$I_{F(ON)}$	Input Diode Forward Current, on-state	7	16	mA
$V_{F(OFF)}$	Input Diode Forward Voltage, off-state	−6	0.9	V
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
I_S	Safety input, output, or supply current	R_{QJA} = 120 °C/W, V_I = 15 V, T_J = 150 °C, T_A = 25 °C			50	mA
		R_{QJA} = 120 °C/W, V_I = 30 V, T_J = 150 °C, T_A = 25 °C			25	
P_S	Safety input, output, or total power	R_{QJA} = 120 °C/W, T_J = 150 °C, T_A = 25 °C			750	mW
T_S	Maximum safety temperature				150	°C

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8.5	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8.5	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 22	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification	For Rated Mains Voltage ≤ 300 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	0.5	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^9	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{10}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^{11}	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification);	8000	V_{PK}
		V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM} (qualification) = 11700v	9000	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5000 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO}- 6000 V_{RMS} ， t = 1 s (100% in production)	5700	V_{RMS}
q_{pd}	Apparent Charge	Method a, After the Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

All test conditions: V_{CC} − V_{EE} = 12 to 40 V, V_{EE} referred as GND, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Input						
I_{FTH_R}	Input Forward Threshold Current, Rising Edge	V_{OUT} > 5 V	1.1	3.6	4.8	mA
V_F	Input Forward Voltage	I_F = 10 mA	1.8	2.05	2.4	V
V_{FTH_F}	Input Threshold Voltage, Falling Edge	V_{OUT} < 5 V	0.9	1.4	1.9	V
$\Delta V_F/\Delta T$	Input Forward Voltage, Temperature Coefficient	I_F = 10 mA		0.9		mV/°C
V_R	Input Reverse Breakdown Voltage	I_R = 10 μA	8.25			V
CIN	Input Parasitic Capacitance	F = 0.5 MHz		15		pF
Output						
I_{OH}	Output Source Peak Current (1)	OUT = H, V_{CC} = 15 V, C_{LOAD} = 0.18 μF, V_{CC} = 0.18 μF, t_{pw} < 10 μs		5		A
I_{OL}	Output Sink Peak Current (1)	I_F = 10 mA, V_{CC} = 15 V, C_{LOAD} = 0.18 μF, V_{CC} = 0.18 μF, t_{pw} < 10 μs		5		A
V_{OH}	Output Voltage, V_{CC} − V_{OUT}	OUT = H, I_{OUT} = −20 mA	70	180	360	mV
V_{OL}	Output Voltage, V_{OUT} − V_{EE}	V_F = 0 V, I_{OUT} = 20 mA		12	25	mV
I_{CC_H}	Output Quiescent Current, OUT = H	OUT = H, I_{OUT} = 0 mA	0.8	1.5	2.4	mA
I_{CC_L}	Output Quiescent Current, OUT = L	V_F = 0 V, I_{OUT} = 0 mA	0.8	1.5	2.4	mA
Under Voltage Lockout, TPM23514 (12-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	11	12.5	13.9	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		10	11.5	12.9	V
V_{UVLO_HYS}	UVLO Hysteresis			1		V
Under Voltage Lockout, TPM23514 (8-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	7.8	8.95	9.8	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		7.05	8.35	9.2	V
V_{UVLO_HYS}	UVLO Hysteresis			0.6		V
Desaturation Protection (TPM23514D Only)						

Parameter		Conditions	Min	Typ	Max	Unit
I_{CHG}	Blanking Capacitor Charge Current	V_{DESAT} = 2.0 V		500		mA
I_{DCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 6.0 V		15		mA
V_{DESAT}	Detection Threshold			9.1		V
V_{DESATL}	Voltage when OUT(L) = LOW, Reference to VEE				1	V
$t_{DESATLEB}$	Leading Edge Blank Time	I_{DESAT} = 15 mA		200		ns
$t_{DESATFIL}$	DESAT Deglitch Filter			150		ns
$t_{DESATOFF}$	DESAT Propagation Delay to OUT(L) 90%			200		ns
$t_{DESATFLT}$	DESAT to FLT Low Delay			600		ns
Internal Miller Clamp (TPM23514M Only)						
V_{CLMPTH}	Miller Clamp Threshold Voltage	$V_{CLAMP} – V_{EE}$		2.1	2.3	V
I_{CLMP}	Miller Clamp Current (1)	$V_{CLAMP} – V_{EE}$ = 3.5 V		1.6		A

(1) Guaranteed by design

Timing Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V		8.2	28	ns
t_f	Output Fall Time (1)			6.5	25	ns
t_{PLH}	Propagation Delay, Low to High			54.9	105	ns
t_{PHL}	Propagation Delay, High to Low			47.4	105	ns
t_{PWD}	Pulse Width Distortion $\|t_{PHL} - t_{PLH}\|$		-35	9.35	35	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay between any Two Parts (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V, I_F = 10 mA			25	ns
t_{UVLO_rec}	UVLO Recovery Delay			28.8	47	µs
$CMTI_H$	Common-mode Transient Immunity (Output High) (1)	I_F= 10 mA, V_{CM} = 1500 V, VCC = 30 V, T_A = 25 °C	150			kV/µs
$CMTI_L$	Common-mode Transient Immunity (Output Low) (1)	V_F= 0 V, V_{CM} = 1500 V, VCC = 30 V, T_A = 25 °C	150			kV/µs

(1) Guaranteed by design

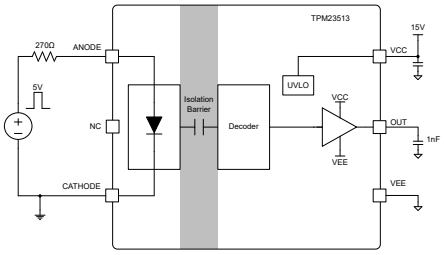


Figure 1. Timing Test Diagram

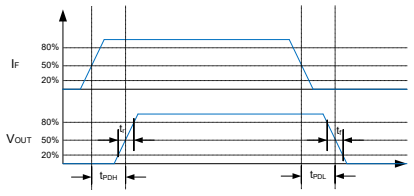


Figure 2. Timing Diagram

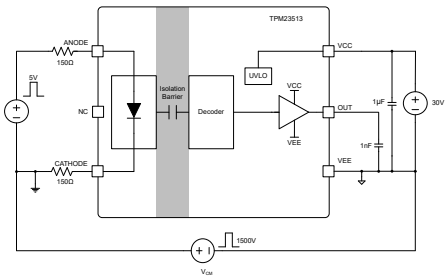


Figure 3. CMTI Test Circuit

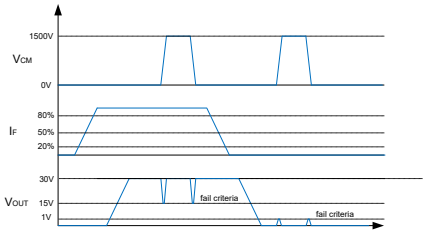


Figure 4. CMTI Test Criteria

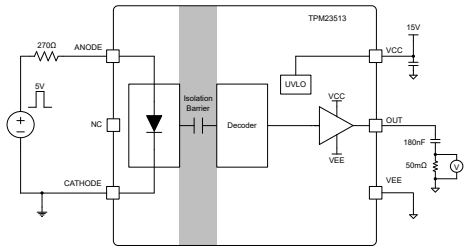


Figure 5. Output Current Test Circuit

Typical Performance Characteristics

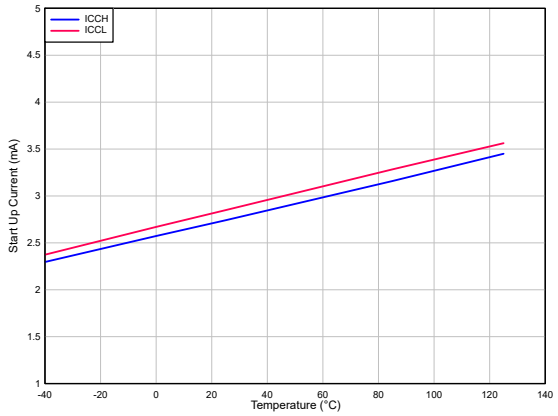


Figure 6. Start-up Current vs. Temperature

V_{CC} = 15 V

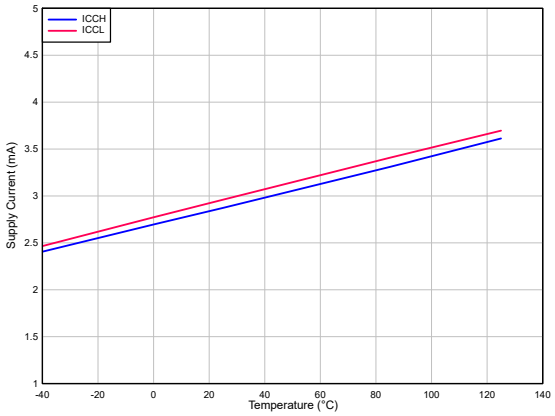


Figure 7. Start-up Current vs. Temperature

V_{CC} = 30 V

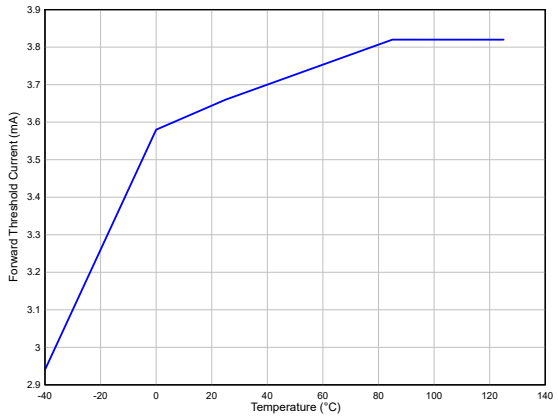


Figure 8. Forward Threshold Current vs. Temperature

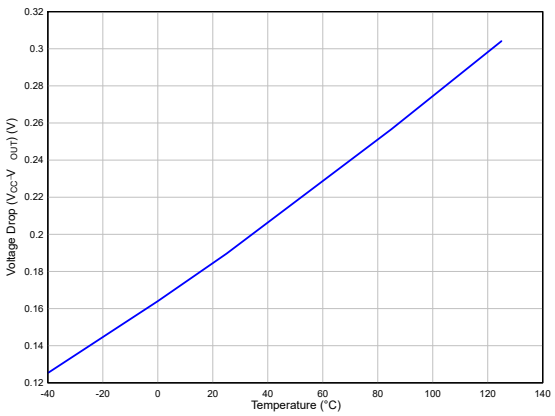


Figure 9. VOH Voltage Drop vs. Temperature

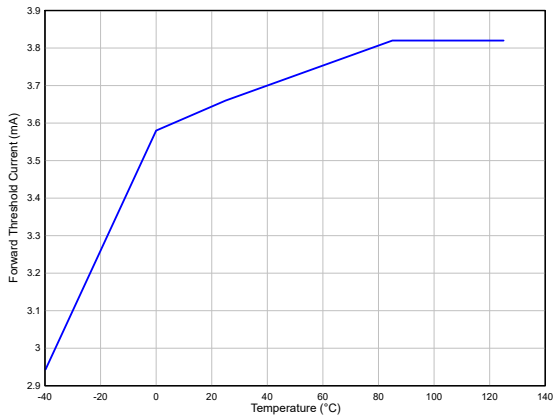


Figure 10. Forward Threshold Current vs. Temperature

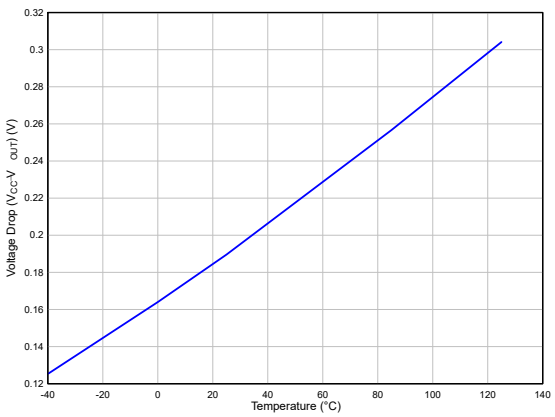


Figure 11. VOH Voltage Drop vs. Temperature

I_{OUT} = 20 mA

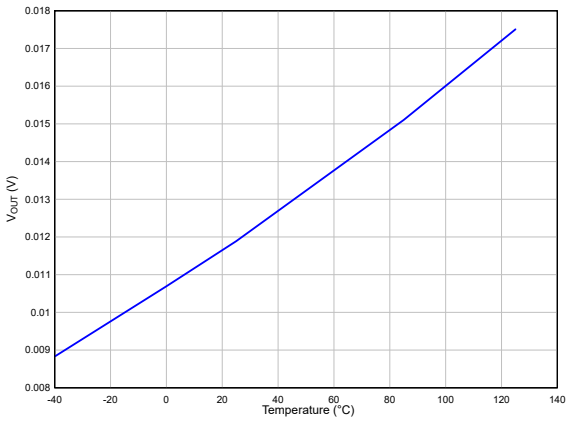


Figure 12. VOI Voltage Drop vs. Temperature

I_{OUT} = –20 mA

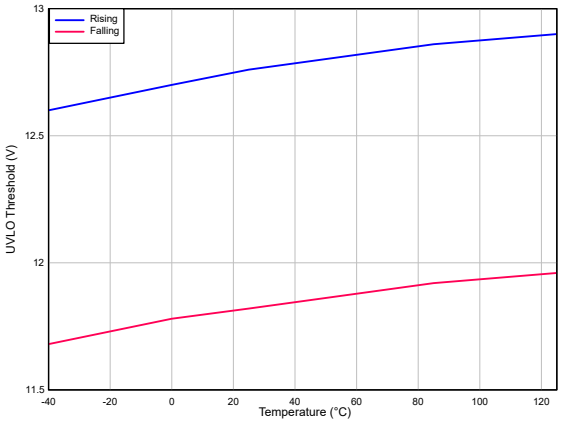


Figure 13. UVLO Threshold vs. Temperature

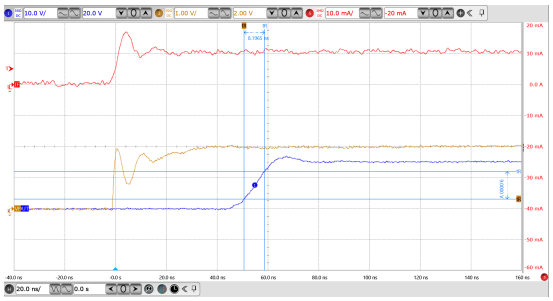


Figure 14. Output Rising Edge

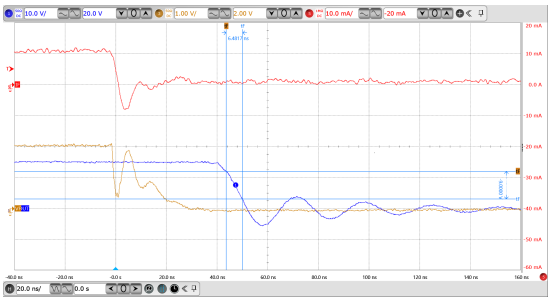


Figure 15. Output Falling Edge

Detailed Description

Overview

The TPM23514x is a single-channel isolated gate driver for MOSFETs, IGBTs, and SiC FETs with an optocoupler compatible input stage. It has a 40-V maximum operating driver voltage, which is especially suitable for high-power fast-transient IGBT/SiC applications.

The TPM23514x is designed to replace the optocoupler gate driver with industry-standard wide-body 8-pin package WSOP8, with more than 8.5-mm creepage and clearance to withstand over 1060-V_{RMS}, reinforced isolation, and 5.7-kV_{RMS}. 3PEAK proprietary isolation technology supports common-mode transient immunity of typical 150 kV/μs.

The TPM23514x offers several variations: split output (TPM23514S), desaturation protection (TPM23514D), and miller clamp(TPM23514M) (refer to the Device Comparison Table). Isolation in the TPM23514x is achieved using high-voltage SiO2-based capacitors with 3PEAK proprietary on-off keying (OOK) modulation scheme. The TPM23514x incorporates advanced circuit techniques to optimize CMTI performance and minimize radiated emissions resulting from the high-frequency carrier and IO buffer switching.

Functional Block Diagram

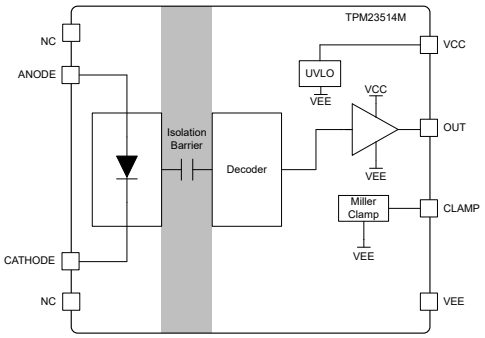


Figure 16. TPM23514M Functional Block Diagram

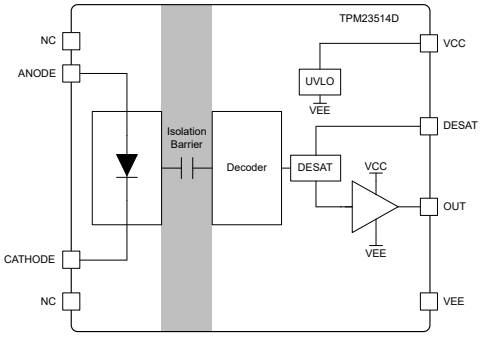


Figure 17. TPM23514D Functional Block Diagram

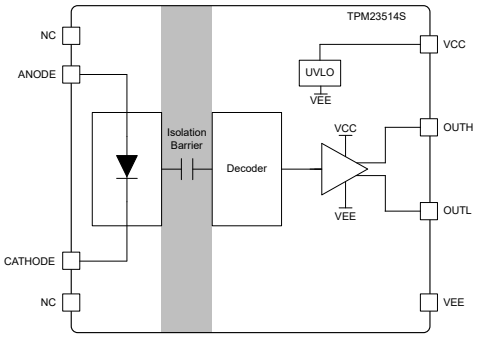


Figure 18. TPM23514S Functional Block Diagram

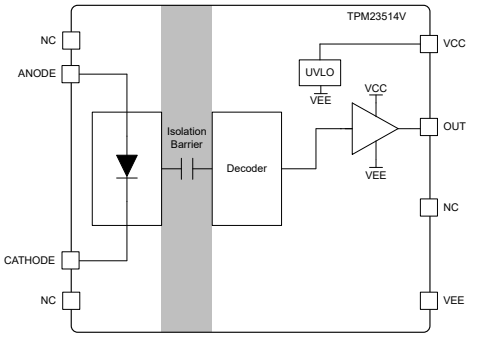


Figure 19. TPM23514V Functional Block Diagram

Feature Description

Emulated Diode Input

The input stage of the TPM23514x is an emulated diode input to be pin-to-pin compatible with the optocoupler input. Working like an opto-diode, when the current flows from ANODE and CATHODE, the forward voltage drop between ANODE and CATHODE is typical 2.1 V. An external resistor can be placed on the ANODE side or the CATHODE side or both to limit the current. 3PEAK recommends that the forward current should be from 7 mA to 30 mA. When the input current is higher than the threshold current I_{FTH_R}, the TPM23514x internal isolation transmitter starts to send CMTI-optimized high-frequency On-Off-Keying (OOK) signals through the double-capacitive silicon dioxide (SiO_2) isolation layer. 3PEAK proprietary isolation technology provides high CMTI performance against fast dV/dt scenarios, which is especially useful for latest-generation applications like SiC FETs.

Decoder & Output Stage

The high-frequency signal is converted by the decoder via a double-capacitive insulation barrier as the output stage's input. The rail-to-rail output stage provides a high-peak current during the output slewing. The output VCC supports a maximum of 40-V input.

UVLO Protection

The output stage has an under-voltage lock-out feature to protect the output driver from malfunction during low-voltage operation. When VCC is lower than the UVLO threshold, the output is driven low. When VCC is higher than the UVLO threshold, the output is operated according to the input bias state. When VCC is unbiased, the output is pulled lower to 2 V to avoid falsely turning on.

Desaturation Protection (DESAT)

The TPM23514D has an internal desaturation protection feature to protect SiC-FET or IGBT from over-current conditions. The device senses the V_{CE} of IGBT or V_{DS} of SiC-FET with the DESAT input pin, and compares it with the internal fixed threshold of 9 V. When the output is on-state, once the DESAT voltage is greater than the threshold after the deglitch timer expires, the device turns off the output and latch off. The DESAT is cleared when the input is turned off. While the input is on-state, the internal VDD sources 500-uA current to pull DESAT high. While the input is off-state, the DESAT is internally pulled down. 3PEAK recommends external resistors and capacitance to prevent false protection from noise.

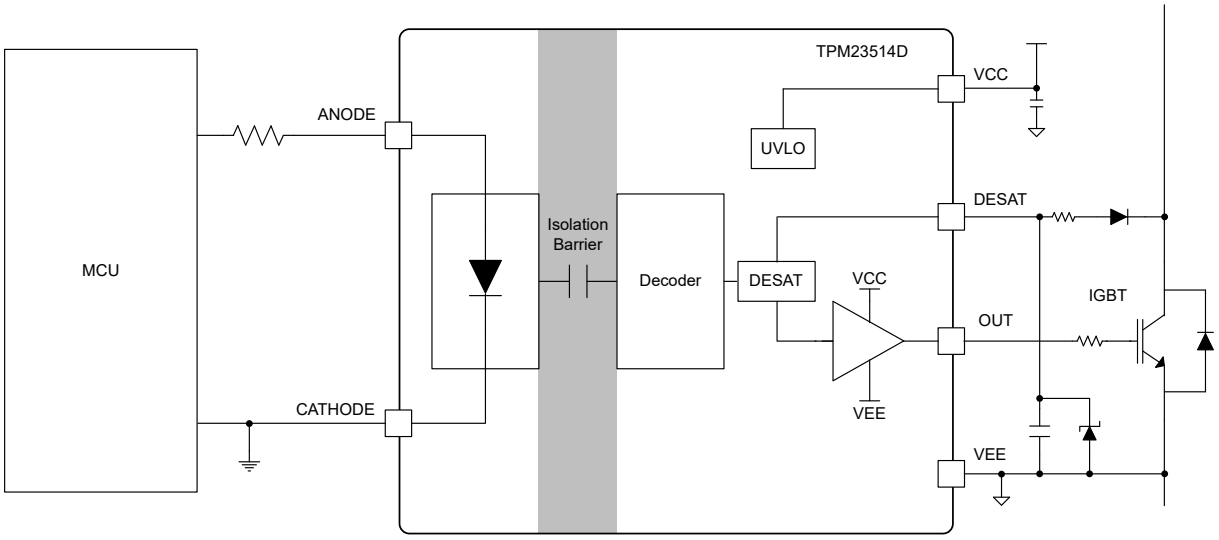


Figure 20. TPM27514D Desaturation Protection Application Diagram

Internal Active Miller Clamp

The TPM23514M provides an internal miller clamp to prevent the output gate from false turning on during off-state. This feature is especially useful for high slew-rate applications when the output can be coupled by high dV/dt. When the output is off state and the gate voltage is lower than V_{CLMPTH}, the miller clamp is turned on with low-impedance path to ground.

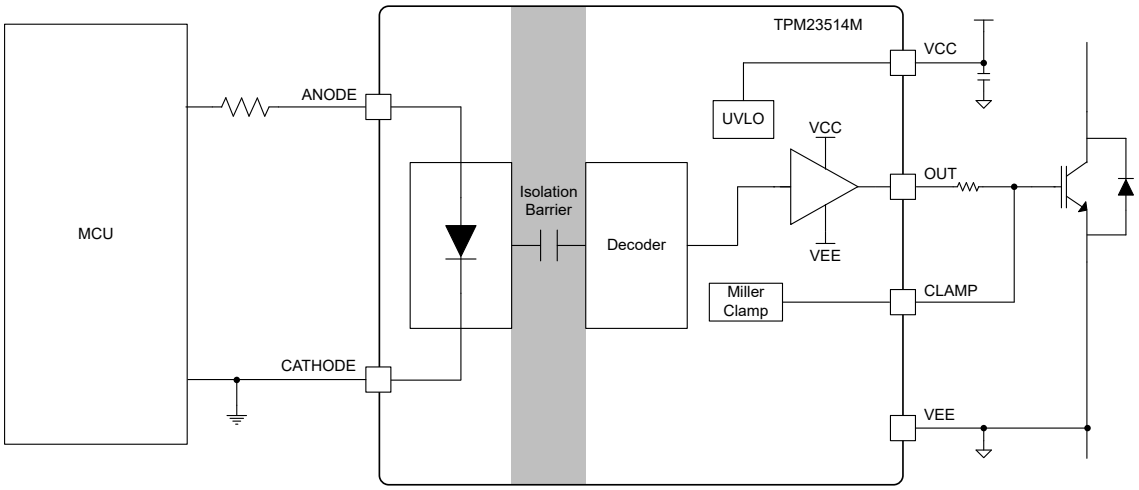


Figure 21. TPM23514M Miller Clamp Application

Split Output

The TPM23514S provides split rail-to-rail pull-up and pull-down outputs. Split outputs provide separate paths for turn-on and turn-off current. With separate paths, the output current can be configured per application needs.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPM23514x supports pin-to-pin replacement of common opto-coupler-based gate drivers. A serial resistor is added to the input path to limit current between 7 mA and 25 mA.

Typical Application

Low-side NMOS Driving

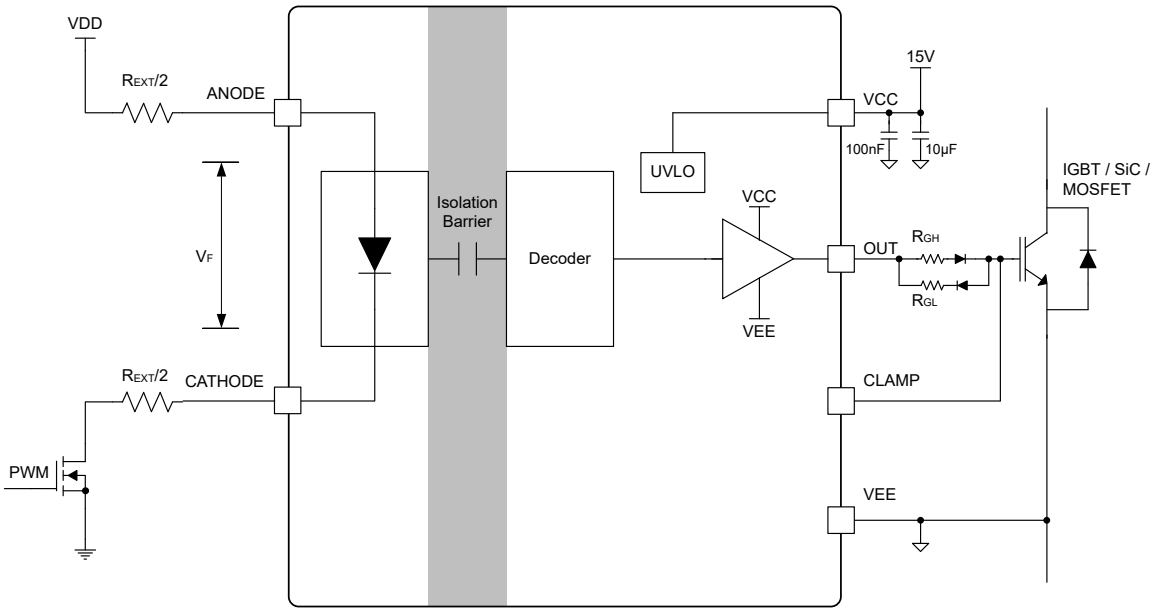
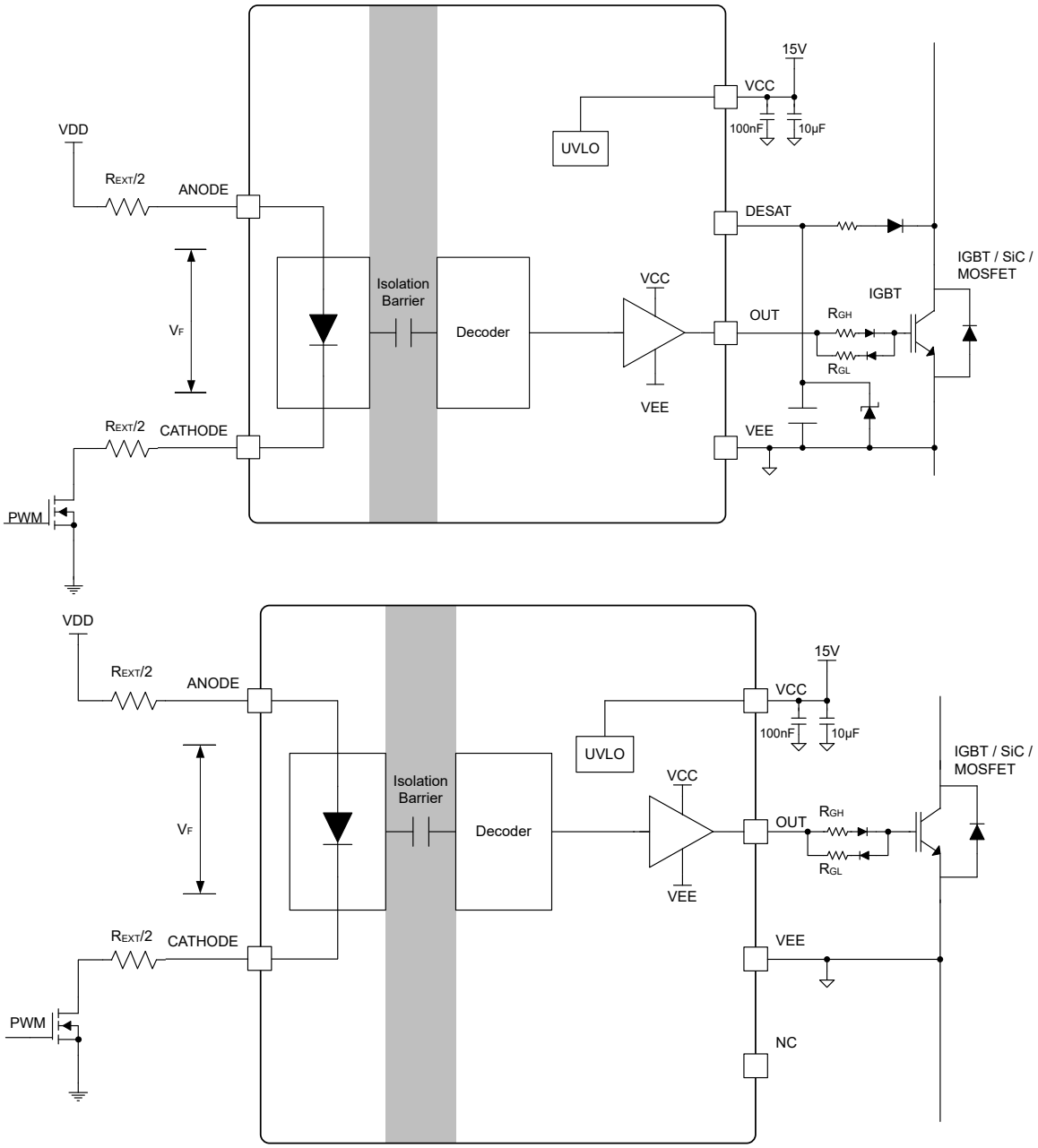
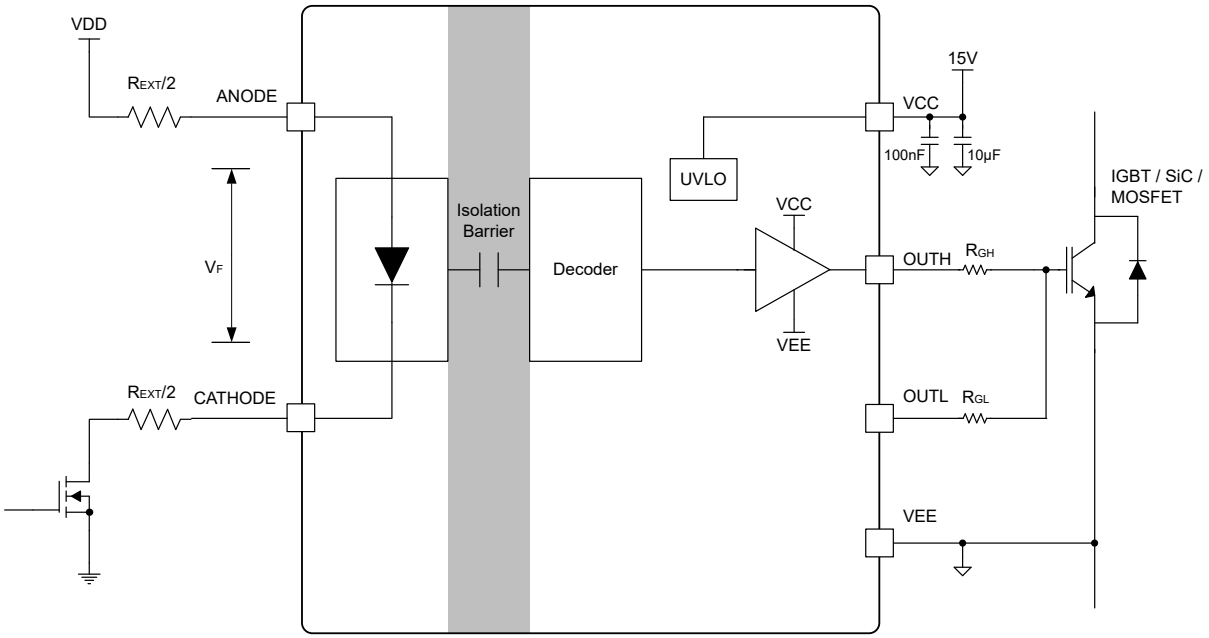
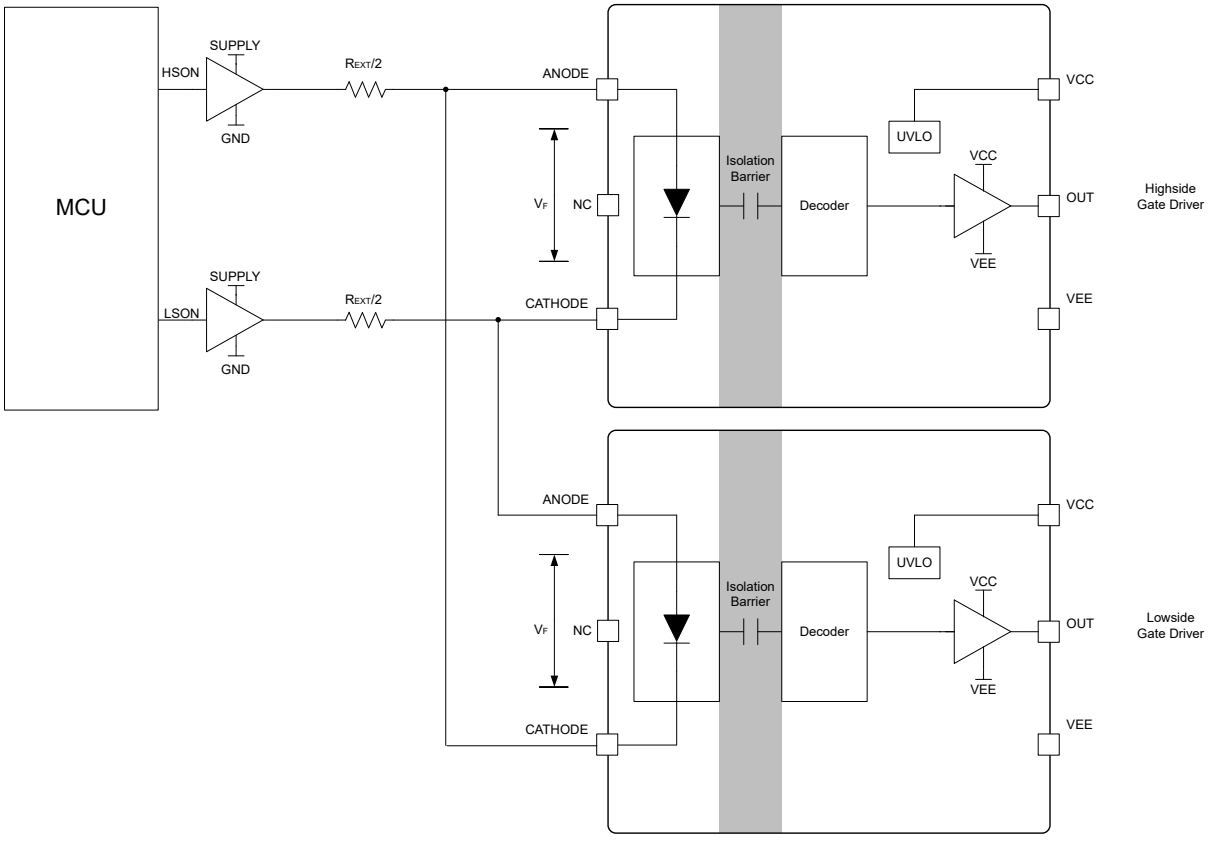


Figure 22. TPM23514M Application Diagram


VDD
REXT/2
ANODE
VF
REXT/2
CATHODE
PWM
Isolation Barrier
Decoder
UVLO
15V
VCC
100nF
10µF
DESAT
VCC
OUT
VEE
VEE
IGBT
RGH
RGL
IGBT / SiC / MOSFET
VDD
REXT/2
ANODE
VF
REXT/2
CATHODE
PWM
Isolation Barrier
Decoder
UVLO
15V
VCC
100nF
10µF
VCC
OUT
VEE
RGH
RGL
IGBT / SiC / MOSFET
VEE
NC



Half-bridge with Interlock

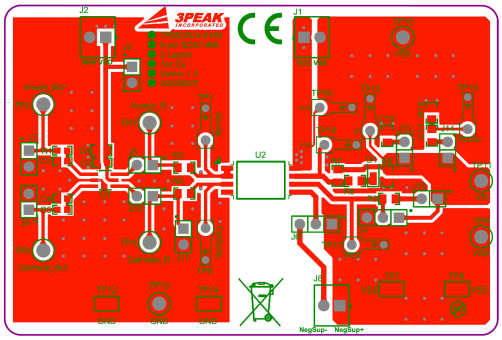


Layout

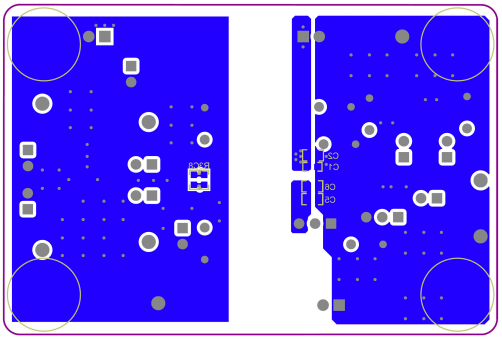
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- For current mode input drivers, a low ESR and ESL capacitor should be placed close to the Cathode and Anode pins.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Recommendations

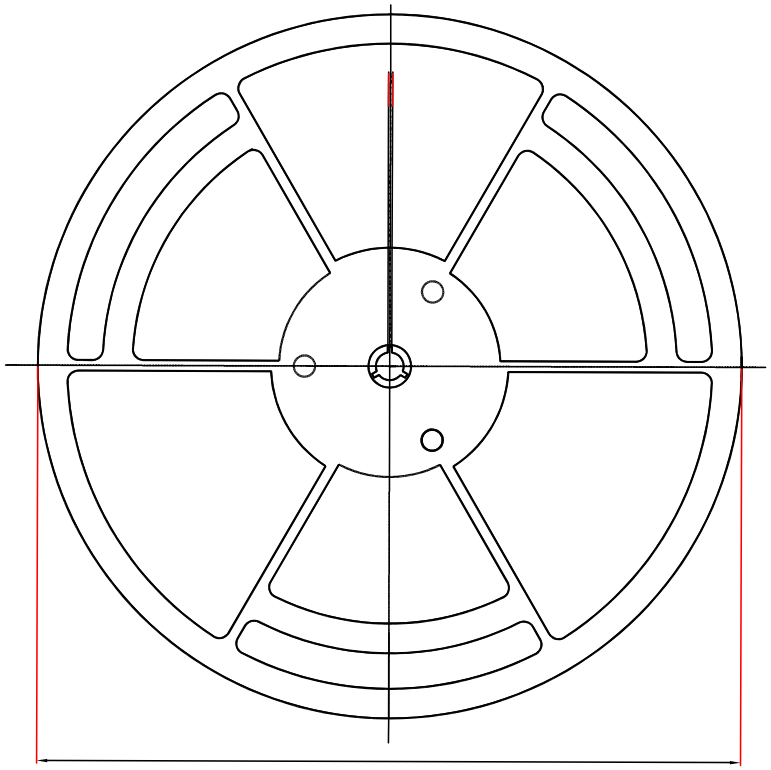


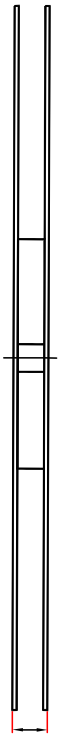
Top Layer

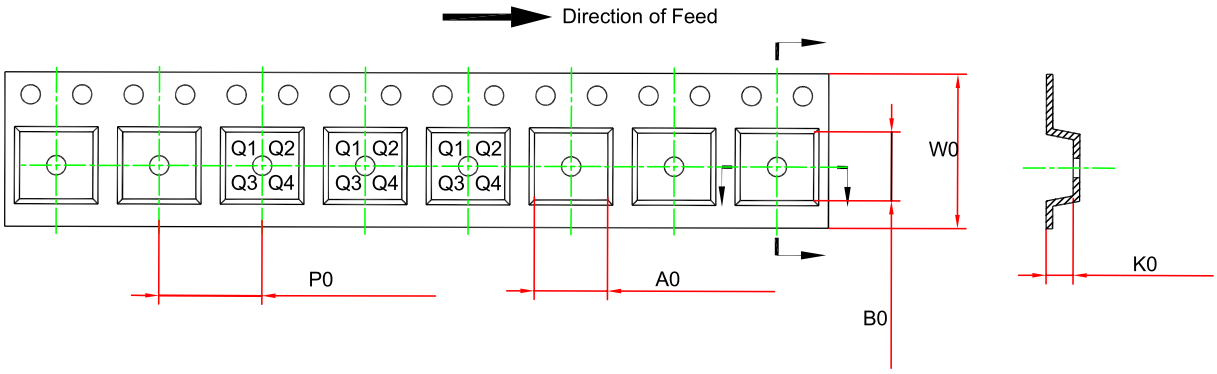


Bottom Layer

Tape and Reel Information







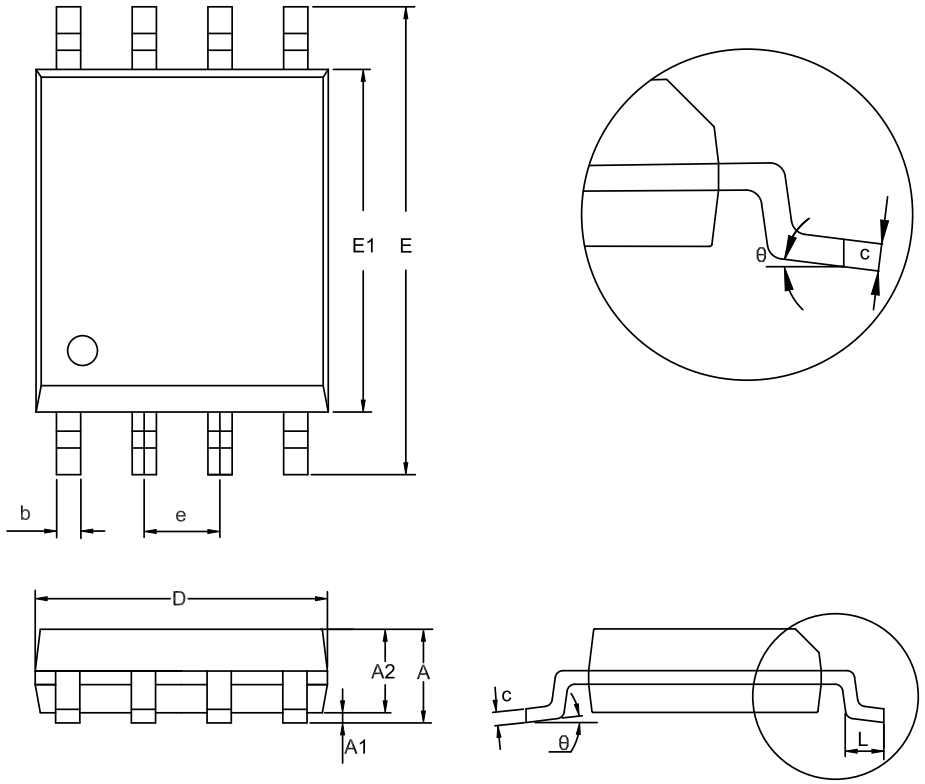
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM23514D-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM23514BM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM23514M-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM23514BS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM23514S-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM23514V-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Package Outline Dimensions

WSOP8

Package Outline Dimensions SOA(WSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.550	2.800	0.100	0.110
A1	0.360	0.460	0.014	0.018
A2	2.190	2.390	0.086	0.094
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM23514D-SOAR (1)	−40 to 125°C	WSOP8	M54D	MSL3	Tape and Reel,1000	Green
TPM23514BM-SOAR (1)	−40 to 125°C	WSOP8	M54BM	MSL3	Tape and Reel,1000	Green
TPM23514M-SOAR	−40 to 125°C	WSOP8	M54M	MSL3	Tape and Reel,1000	Green
TPM23514BS-SOAR (1)	−40 to 125°C	WSOP8	M54BS	MSL3	Tape and Reel,1000	Green
TPM23514S-SOAR (1)	−40 to 125°C	WSOP8	M54S	MSL3	Tape and Reel,1000	Green
TPM23514V-SOAR (1)	−40 to 125°C	WSOP8	M54V	MSL3	Tape and Reel,1000	Green

(1) For future products, please contact 3PEAK representatives for samples and more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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