# TPMC150

## 4, 3, 2 or 1 Channel Synchro/Resolver-to-Digital Converter

Version 1.0

## User Manual

Issue 1.3

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## TPMC150-10

4 Channel Synchro/Resolver-to-Digital Converter

## TPMC150-11

3 Channel Synchro/Resolver-to-Digital Converter

## TPMC150-12

2 Channel Synchro/Resolver-to-Digital Converter

## TPMC150-13

1 Channel Synchro/Resolver-to-Digital Converter

## Signal Conditioning Adapter

### TPMC150-A1-xx

Resolver interface

### TPMC150-A2-xx

Resolver interface with reference oscillator

### TPMC150-A3-xx

High precision synchro/resolver interface

### TPMC150-A4-xx

High precision synchro/resolver interface with reference oscillator

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**Style Conventions**

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low’ is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

| | |
|---|---|
| W | Write Only |
| R | Read Only |
| R/W | Read/Write |
| R/C | Read/Clear |
| R/S | Read/Set |

| Issue | Description | Date |
|:---:|:---:|:---:|
| - | Preliminary Issue | February 2003 |
| 1.0 | First Issue | June 2003 |
| 1.1 | Corrected storage temperature, corrected typos | March 2005 |
| 1.2 | Corrected Connection Examples | January 2006 |
| 1.3 | New address TEWS LLC | September 2006 |

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# 1  Product Description

The TPMC150 is a standard single-width 32 bit PMC module providing four (TPMC150-10), three (TPMC150-11), two (TPMC150-12) or one channel (TPMC150-13) of a Tracking Synchro/Resolver-To-Digital Converter (RDC) with a converter accuracy of 2 arcmin + 1LSB.

The TPMC150 is designed for use in high performance commercial, industrial and military systems. It can by used for many applications like motor control, robot axis control, process control, radar antenna position information, and CNC machine tooling.

Each of the up to four RDC channels on the TPMC150 utilizes DDC's versatile state-of-the-art Tracking Synchro/Resolver-To-Digital Converter RDC19230 with programmable resolution. Resolution programming allows selection of 10, 12, 14 or 16 bit conversion. This combines the high tracking rate of a 10 bit converter with the precision of a 16 bit converter. The RDC19230 provides incremental encoder emulation. Encoder phase signals A, B and Index I are fed to an on board 32 bit up-/down encoder counter with preload and output register. Additionally the synthesized encoder signals are available for external use via RS485/422 output drivers. The RDC19230 provides a 4V velocity output with a linearity of 0.75%, which can be used to replace a tachometer. A 24V isolated digital input per channel can be used as general purpose input or as reference input.

A 'Simultaneous Read' function allows latching of the actual values of the selected converters at the same time.
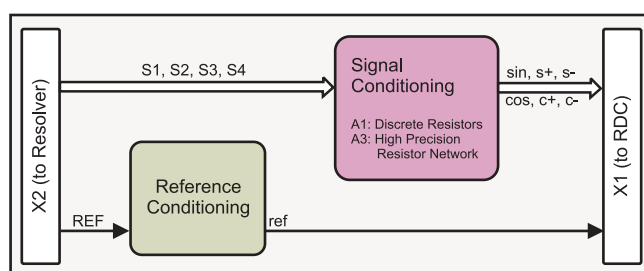


Figure 1-1 : Signal Conditioning Adapter TPMC150-A1/A3

Signal Conditioning Adapters (TPMC150-Ay-xx) are required for each synchro/resolver channel to adapt the signal levels of the synchro/resolver to the RDC19230 and to configure the optional reference oscillator input/output. The Signal Conditioning Adapters will be built individually to customer specification of the synchro or resolver specifications. The Signal Conditioning Adapters are factory installed on the TPMC150.
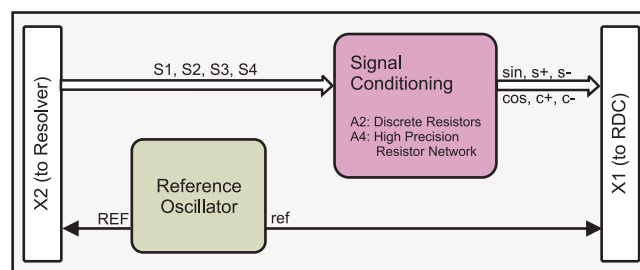


Figure 1-2 : Signal Conditioning Adapter TPMC150-A2/A4 with reference oscillator

Four types of Signal Conditioning Adapters are available to adapt the signal levels of the synchro/resolver to the RDC19230: The TPMC150-A1-xx and the TPMC150-A2-xx use high precision, low TK discrete resistors. These Adapters are mainly used for resolver applications. The TPMC150-A3-xx and the TPMC150-A4-xx use a high precision resistor network with matched resistors. These adapters are mainly used for synchro applications or resolver applications which require highest accuracy. Additionally the TPMC150-A2-xx and the TPMC150-A4-xx offer an on board reference oscillator with factory selectable frequencies in the range of 2 kHz to 10 kHz.

The on board encoder counter for each channel is a 32 bit up-/down counter with preload and output register. The encoder counter is fed with the emulated A, B and Index signals from the RDC19230. The counters are programmable for single, double and quad analysis of the incremental encoder signals. The counter can be manually or automatically loaded with the value of the preload register, depending on mode. An 'Auto Reference Mode' provides the possibility of automatic preload of the encoder counter during normal operation, whenever the motion system passes the reference position. A 'Simultaneous Read' function allows latching of the actual values of the selected encoder counters. These values can then be read successively without interfering with normal counter function.

The TPMC150 offers one digital 24V input per channel which is galvanically isolated by optocouplers. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. The inputs are electronically debounced. Each of the four digital 24V inputs can generate an interrupt, triggered on rising or falling edge. Depending on the selected mode the input can be used as general purpose input or as reference input.
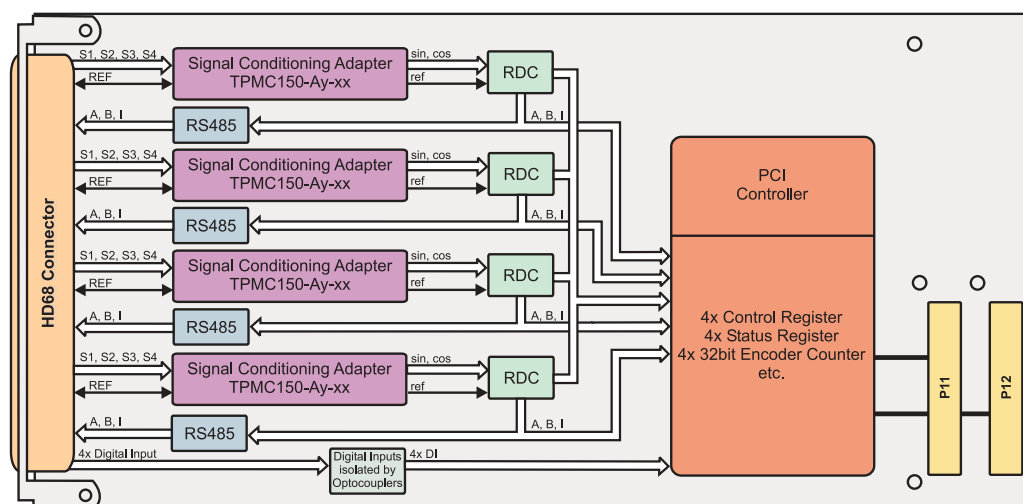


Figure 1-3 : Block Diagram TPMC150-10

# 2 Technical Specification

| | |
|---|---|
| **Mechanical Interface** | PCI Mezzanine Card (PMC) Interface<br>Single Size |
| **Electrical Interface** | PCI Rev. 2.2 compliant<br>33 MHz / 32 bit PCI<br>3.3V and 5V PCI Signaling Voltage |
| **On Board Devices** | |
| **PCI Target Chip** | PCI9030 (PLX Technology) |
| **Converter Chip** | RDC 19230 |
| **Converter Resolution** | Programmable 10,12,14 or 16 bits |
| **Converter Accuracy** | 2 arcmin + 1 LSB |
| **Input Signal Conditioning** | Signal Conditioning Adapter TPMC150-A1 – TPMC150-A4 |
| **Additional Output** | Velocity output<br>Incremental encoder emulation, available as RS422/485 outputs |
| **Motion Feedback** | 32 bit up/down encoder counter with preload and output register per channel |
| **Digital Input** | 1 digital 24V input per channel |
| **I/O Interface** | |
| **I/O Connector** | HD68 SCSI-3 type female connector (no PMC P14 I/O) |
| **Physical Data** | |
| **Power Requirements** | 260 mA typical @ +3.3V DC<br>85 mA typical @ +5.0V DC<br>75 mA typical @ -12V DC |
| **Temperature Range** | Operating    -40°C to +85°C<br>Storage      -55°C to +125°C |
| **MTBF** | TPMC150-10: 240 000 h<br>TPMC150-11: 286 000 h<br>TPMC150-12: 354 000 h<br>TPMC150-13: 464 000 h |
| **Humidity** | 5 – 95 % non-condensing |
| **Weight** | 71 g |

Figure 2-1 : Technical Specification TPMC150

## 2.1 Tracking Rate Characteristics

Tracking Rate, bandwidth and velocity scaling is dependent on the resolution of the RDC.

rps = Revolutions per second

| Resolution | 10 | 12 | 14 | 16 |
|---|---|---|---|---|
| Tracking rate (rps) | 1022 | 255 | 64 | 16 |
| Bandwidth (Hz) | 1024 | | 270 | |
| Carrier frequency (kHz) | 4 - 10 | 4 - 10 | 1 - 7 | 1 - 5 |
| Scale factor (V/rps) | 0.0039 | 0.0157 | 0.0625 | 0.25 |

Figure 2-2 : Tracking Rate Characteristics

## 2.2 Velocity Output Characteristics

| Parameter | Unit | Typical | Min/Max |
|---|---|---|---|
| Polarity | | Positive for increasing angle | |
| Voltage range (full scale) | V | ±4 | |
| Scale factor error | % | 10 | 20 |
| Scale factor TC | PPM/C | 100 | 200 |
| Reversal error | % | 0.75 | 1.3 |
| Linearity | % | 0.25 | 0.5 |
| Zero Offset | mV | 5 | 10 |
| Zero Offset TC | µV/C | 15 | 30 |
| Load | kΩ | | 8 |

Figure 2-3 : Velocity Output Characteristics

Applying loads on the velocity output may affect converter accuracy. To use the velocity output line to monitor speeds, a buffer must be added to the line.

The velocity output is a DC-signal with an AC-ripple. The main components of the ripple are the carrier frequency and double the carrier frequency. The ripple can be filtered behind the buffer. Set the RC to cut off below the carrier frequency.

> **Neither the buffer nor the velocity ripple filter is included on the TPMC150.**
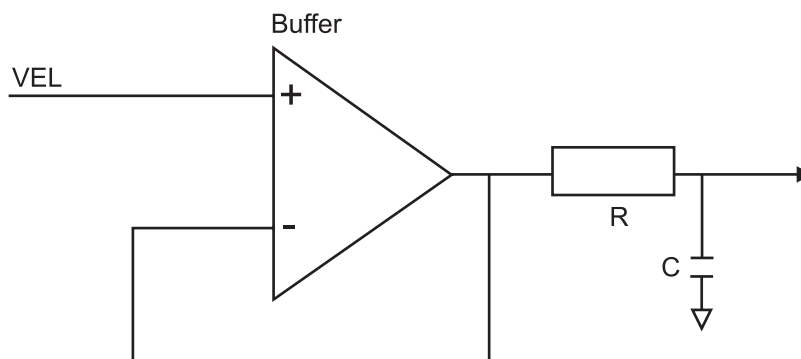


Figure 2-4 : Velocity Ripple Filter

# 2.3 Digital Input Characteristics

The TPMC150 offers one digital 24V input per channel which is galvanically isolated by optocouplers. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. The inputs are electronically debounced. Each of the four digital 24V inputs can generate an interrupt, triggered on rising or falling edge. Depending on the selected reference mode the input can be used as general purpose input or as reference input.

| Parameter | Unit | Typical |
|---|---|---|
| Input isolation | | Optocoupler as galvanic isolation |
| Input voltage | V | 24 |
| Input current | mA | 4.2 (at 24V input voltage) |
| Switching level | V | 12 (min. 7.5, max. 14) |

Figure 2-5 : Digital Input Characteristics
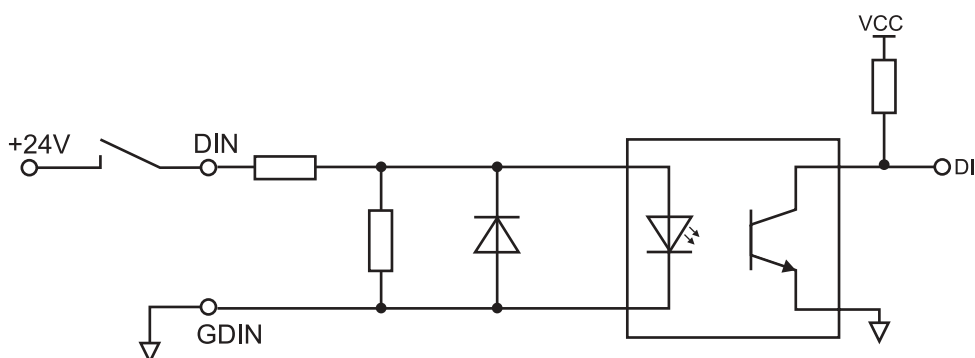


Figure 2-6 : Digital Input Wiring

# 3 TPMC150 Local Space Addressing

## 3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

| PCI9030 Local Space | PCI9030 PCI Base Address (Offset in PCI Configuration Space) | PCI Space Mapping | Size (Byte) | Port Width (Bit) | Endian Mode | Description |
|---|---|---|---|---|---|---|
| 0 | 2 (0x18) | MEM | 128 | 32 | BIG | Register Address Space |
| 1 | 3 (0x1C) | - | - | - | - | Not Used |
| 2 | 4 (0x20) | - | - | - | - | Not Used |
| 3 | 5 (0x24) | - | - | - | - | Not Used |

Figure 3-1 : PCI9030 Local Space Configuration

## 3.2 Register Address Space

PCI Base Address:  PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

| Offset to PCI Base Address 2 | Register Name | Size (Bit) |
|---|---|---|
| 0x00 | Global Control/Status Register | 32 |
| 0x04 | Interrupt Control/Status Register | 32 |
| 0x08 | Digital Input Register | 32 |
| 0x0C | Channel Control Register 1 | 32 |
| 0x10 | Channel Control Register 2 | 32 |
| 0x14 | Channel Control Register 3 | 32 |
| 0x18 | Channel Control Register 4 | 32 |
| 0x1C | Channel Data Register 1 | 32 |
| 0x20 | Channel Data Register 2 | 32 |
| 0x24 | Channel Data Register 3 | 32 |
| 0x28 | Channel Data Register 4 | 32 |
| 0x2C | Channel Status Register 1 | 32 |
| 0x30 | Channel Status Register 2 | 32 |
| 0x34 | Channel Status Register 3 | 32 |
| 0x38 | Channel Status Register 4 | 32 |
| 0x3C | Encoder Counter Preload/Data Register 1 | 32 |
| 0x40 | Encoder Counter Preload/Data Register 2 | 32 |
| 0x44 | Encoder Counter Preload/Data Register 3 | 32 |
| 0x48 | Encoder Counter Preload/Data Register 4 | 32 |
| 0x4C … 0x80 | Reserved | - |

Figure 3-2 : Register Address Space

If in the following register descriptions the equivalent bits of all channels are combined into a bit field, the bit field refers to the channels in ascending order. For example the LSB of the bit field refers to Channel 1 and the MSB to Channel 4.

## 3.2.1 Global Control/Status Register

| Bit | Symbol | Description | Access | Reset |
|---|---|---|---|---|
| 17-31 | | Reserved (Undefined for reads. Write as '0'.) | - | X |
| 16 | CTRL_CON_STA | Multiple Converter Read Status<br>1: Multiple Converter Read in progress | R | 0 |
| 12-15 | CTRL_CON_SEL | Multiple Converter Read Channel Select<br>Writing a '1' to a bit select the corresponding channel for Multiple Converter Read. | R/W | 0000 |
| 11 | CTRL_CON_RD | Multiple Converter Read<br>0: Disabled<br>1: Enabled<br>See chapter 'Multiple Converter Read' for details. | R/W | 0 |
| 10 | CTRL_ENC_STA | Multiple Encoder Read Status<br>1: Multiple Encoder Read in progress | R | 0 |
| 6-9 | CTRL_ENC_SEL | Multiple Encoder Read Channel Select<br>Writing a '1' to a bit select the corresponding channel for Multiple Encoder Read. | R/W | 0000 |
| 5 | CTRL_ENC_RD | Multiple Encoder Read<br>0: Disabled<br>1: Enabled<br>See chapter 'Multiple Encoder Read' for details. | R/W | 0 |
| 4 | CTRL_IRQ | General IRQ Enable<br>0: globally disables interrupts<br>1: globally enables interrupts for the digital 24V inputs. | R/W | 0 |
| 0-3 | CTRL_PRE | Manual Encoder Counter Preload<br>Writing a '1' issues a preload of the corresponding encoder counter with the value of the Encoder Counter Preload Register. This preload method is only possible in the 'None Reference Mode'. After the preload access is executed, these bits are cleared automatically and signal a successful preload. Before using this preload method, the corresponding Encoder Counter Preload Register must be loaded with valid data. | R/W | 0000 |

Figure 3-3 : Global Control/Status Register

**The digital 24V inputs generate interrupts at pin INTA# of the PMC bus. Additional to this Global Interrupt Enable the Interrupt INTA# must be enabled in the Interrupt Control Register (INTCSR; 0x4C) of the PCI Controller PCI9030. Default after power on and reset: INTA# is enabled.**

## 3.2.2 Interrupt Control/Status Register

| Bit | Symbol | Description | Access | Reset |
|---|---|---|---|---|
| 12-31 | | Reserved (Undefined for reads. Write as '0'.) | - | X |
| 8-11 | IRQ_CTRL | Digital Input Interrupt Control<br>0: interrupt on falling edge<br>1: interrupt on rising edge | R/W | 0000 |
| 4-7 | IRQ_STA | Digital Input Interrupt Status<br>0: no interrupt request is pending<br>1: an interrupt request is pending<br>A pending interrupt request for a specific digital 24V input is cleared by writing a '1' to the according status bit. | R/W | 0000 |
| 0-3 | IRQ_EN | Digital Input Interrupt Enable<br>To enable the interrupt for a digital input, set the corresponding bit to '1'. | R/W | 0000 |

Figure 3-4 : Interrupt Control/Status Register

The following table shows a short overview about enabling interrupts and the active trigger edge.

| Digital 24V input | Bit | Interrupt | | Bit | Active edge | |
|---|---|---|---|---|---|---|
| | | disable | enable | | falling | rising |
| DIN1 | 0 | '0' | '1' | 8 | '0' | '1' |
| DIN2 | 1 | '0' | '1' | 9 | '0' | '1' |
| DIN3 | 2 | '0' | '1' | 10 | '0' | '1' |
| DIN4 | 3 | '0' | '1' | 11 | '0' | '1' |

Figure 3-5 : Input Interrupt configuration

## 3.2.3 Digital Input Register

| Bit | Symbol | Description | Access | Reset |
|-----|--------|-------------|--------|-------|
| 4-31 | | Reserved (Undefined for reads. Write as '0'.) | - | X |
| 0-3 | DIN | Digital Input State<br>Reflects the actual state of the digital 24V inputs.<br>This register is always active and reflects the state of the digital 24V inputs at all times. | R | 0000 |

Figure 3-6 : Digital Input Register

In the 'None Reference Mode' and 'Index Mode' the digital 24V inputs can be used as general purpose inputs.

In the 'Reference Mode' and 'Auto Reference Mode' the digital 24V inputs are used as reference inputs.

## 3.2.4 Channel Control Register

| Bit | Symbol | Description | Access | Reset |
|-----|--------|-------------|--------|-------|
| 10-31 | | Reserved (Undefined for reads. Write as '0'.) | - | X |
| 9 | CH_EMU_OUT | Incremental Encoder Emulation Output<br>0: Disabled<br>1: Output of the Encoder Emulation via the RS485/422 drivers enabled<br>See chapter 'Incremental Encoder Emulation Output' for details. | R/W | 0 |
| 8 | CH_EMU_EN | Incremental Encoder Emulation<br>0: Disabled<br>1: Enabled; this bit activates the Incremental Encoder Emulation. When set to '1', the current converter resolution is latched und used for the Incremental Encoder Emulation.<br>This bit also enables the Encoder Counter. | R/W | 0 |
| 6-7 | CH_REF | Encoder Reference Mode<br><table><tr><th colspan="2">Value</th><th>Reference Mode</th></tr><tr><td>0</td><td>0</td><td>None Reference Mode</td></tr><tr><td>0</td><td>1</td><td>Reference Mode</td></tr><tr><td>1</td><td>0</td><td>Auto Reference Mode</td></tr><tr><td>1</td><td>1</td><td>Index Mode</td></tr></table>See chapter 'Reference Mode' for details. | R/W | 00 |
| 4-5 | CH_ESAM | Encoder Signal Analysis Mode<br><table><tr><th colspan="2">Value</th><th>Analysis Mode</th></tr><tr><td>0</td><td>0</td><td>disable Counter</td></tr><tr><td>0</td><td>1</td><td>1x – single</td></tr><tr><td>1</td><td>0</td><td>2x – double</td></tr><tr><td>1</td><td>1</td><td>4x – quad</td></tr></table>See chapter 'Encoder Signal Analysis Mode' for details. | R/W | 00 |

| Bit | Symbol | Description | Access | Reset |
|---|---|---|---|---|
| 3 | CH_SYN_CON | Synchronous Conversion<br>0: Disabled<br>1: Enabled (only Channel 1 & 3)<br>For channel 2 and 4 a set on CH_SYN_CON is ignored and a read access returns a '0'.<br>See chapter 'Operating with Synchronous Conversion' for details. | R/W | 0 |
| 2 | CH_SYN_LAT | Synchronous Status Latch<br>0: Disabled<br>1: Enabled<br>See chapter 'Operating with Synchronous Status Latch' for details. | R/W | 0 |
| 0-1 | CH_RES | Converter Resolution<br>Sets the converter resolution. Available values are:<br><br>| Value | | Resolution |<br>|---|---|---|<br>| 0 | 0 | 10 bit |<br>| 0 | 1 | 12 bit |<br>| 1 | 0 | 14 bit |<br>| 1 | 1 | 16 bit | | R/W | 00 |

Figure 3-7 : Channel Control Register

**The converter resolution can be changed after the Incremental Encoder Emulation resolution is set, but it must not be less than the resolution of the Incremental Encoder Emulation. If the converter resolution is less then the Incremental Encoder Emulation resolution, there will be no Encoder Emulation output!**

## 3.2.5 Channel Data Register

The Channel Data Register contains the 16 bit wide converted data value of the synchro or resolver. When the resolution is set to less than 16 bits, all unused bits are read as '0'. The conversion result is always MSB aligned (i.e. aligned to bit 15). The resolution is controlled by the Channel Control Register.

| Bit | Symbol | Description | Access | Reset |
|---|---|---|---|---|
| 16-31 | | Reserved (Reads as '0') | - | X |
| 0-15 | CH_DATA | Converter Data | R | 0 |

Figure 3-8 : Channel Data Register

The position of the LSB depends on the resolution:

| Resolution | D31-16 | D15 | D14…7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 0 | MSB | X | LSB | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 0 | MSB | X | X | X | LSB | 0 | 0 | 0 | 0 |
| 14 | 0 | MSB | X | X | X | X | X | LSB | 0 | 0 |
| 16 | 0 | MSB | X | X | X | X | X | X | X | LSB |

Figure 3-9 : LSB Position

## 3.2.6 Channel Status Register

| Bit | Symbol | Description | Access | Reset |
|---|---|---|---|---|
| 3-31 | | Reserved (Undefined for reads. Write as '0'.) | - | X |
| 2 | CH_STA_DIR | Direction of Motion<br>0: down (clockwise, angle decreasing)<br>1: up (counter clockwise, angle increasing)<br>On a static signal, CH_STA_DIR indicates the last direction of motion. | R | 0 |
| 1 | CH_STA_AM | Adapter mounting<br>0: Adapter mounted<br>1: No adapter mounted | R | 0 |
| 0 | CH_STA_BIT | Converter Build-in-Self-Test<br>Built-In-Test (BIT) = '1' indicates an error. The causes for an error are as follows:<br>1. Loss of Signal (LOS). Both input signals (+S/-S and +C/-C) drop below the threshold voltage of 500mV.<br>2. Phase Error. The input signal phase is more than 180° different from the reference signal phase.<br>3. Excessive Error. The digital output is more than a 100 LSBs different from the input angle.<br>4. Loss of Reference (LOR). The reference input signal is less than 500mV.<br>On normal operation, a BIT occurs during large step changes of the input or on high accelerations that cause acceleration lag. | R | 0 |

Figure 3-10: Channel Status Register

**The direction indication is reliable only when the Encoder Emulation is active. If the Encoder Emulation is not active, this bit reflects the 'U'-output of the RDC19230, which is not reliable on static angles.**

If CH_STA_BIT is read as '1' the resolution could be changed from its programmed value one step down to a lower resolution. This would allow the converter to settle out faster (see chapter 'Changing Resolution on the Fly').

## 3.2.7 Encoder Counter Preload/Data Register

A write access updates the Encoder Counter Preload Register. A read access reads the Encoder Counter Data Register.

| Bit | Symbol | Description | Access | Reset |
|------|----------|-------------|--------|-------|
| 0-31 | ENC_PRE | Encoder Counter Preload Register<br>The Encoder Counter Preload Register is used in all modes for reference preload. | W | 0 |
| 0-31 | ENC_DATA | Encoder Counter Data Register<br>The actual encoder counter value is latched into the Encoder Counter Data Register. | R | 0 |

Figure 3-11: Encoder Counter Preload/Data Register

If the Multiple Encoder Read feature is used for the Encoder Counter Data Registers, a read access latches all counter values for the enabled counters at the same time. Then the Encoder Counter Data Registers can be read one after the other. A new Multiple Encoder Read access is only possible after finishing the read of all latched Encoder Counter Data Registers.

# 4 PCI9030 Target Chip

## 4.1 PCI Configuration Registers (PCR)

### 4.1.1 PCI9030 Header

| PCI CFG Register Address | Write '0' to all unused (Reserved) bits | | | | | | | PCI writeable | Initial Values (Hex Values) |
|---|---|---|---|---|---|---|---|---|---|
| | 31 | 24 | 23 | 16 | 15 | 8 | 7 0 | | |
| 0x00 | Device ID | | | | Vendor ID | | | N | 0096 1498 |
| 0x04 | Status | | | | Command | | | Y | 0280 0000 |
| 0x08 | Class Code | | | | | | Revision ID | N | 118000 0A |
| 0x0C | BIST | | Header Type | | PCI Latency Timer | | Cache Line Size | Y[7:0] | 00 00 00 00 |
| 0x10 | PCI Base Address 0 for MEM Mapped Config. Registers | | | | | | | Y | FFFFFF80 |
| 0x14 | PCI Base Address 1 for I/O Mapped Config. Registers | | | | | | | Y | FFFFFF81 |
| 0x18 | PCI Base Address 2 for Local Address Space 0 | | | | | | | Y | FFFFFF80 |
| 0x1C | PCI Base Address 3 for Local Address Space 1 | | | | | | | Y | 00000000 |
| 0x20 | PCI Base Address 4 for Local Address Space 2 | | | | | | | Y | 00000000 |
| 0x24 | PCI Base Address 5 for Local Address Space 3 | | | | | | | Y | 00000000 |
| 0x28 | PCI CardBus Information Structure Pointer | | | | | | | N | 00000000 |
| 0x2C | Subsystem ID | | | | Subsystem Vendor ID | | | N | s.b. 1498 |
| 0x30 | PCI Base Address for Local Expansion ROM | | | | | | | Y | 00000000 |
| 0x34 | Reserved | | | | | | New Cap. Ptr. | N | 000000 40 |
| 0x38 | Reserved | | | | | | | N | 00000000 |
| 0x3C | Max_Lat | | Min_Gnt | | Interrupt Pin | | Interrupt Line | Y[7:0] | 00 00 01 00 |
| 0x40 | PM Cap. | | | | PM Nxt Cap. | | PM Cap. ID | N | 4801 00 01 |
| 0x44 | PM Data | | PM CSR EXT | | PM CSR | | | Y | 00 00 0000 |
| 0x48 | Reserved | | HS CSR | | HS Nxt Cap. | | HS Cap. ID | Y[23:16] | 00 00 00 00 |
| 0x4C | VPD Address | | | | VPD Nxt Cap. | | VPD Cap. ID | Y[31:16] | 0000 00 03 |
| 0x50 | VPD Data | | | | | | | Y | 00000000 |

Figure 4-1 : PCI9030 Header

Subsystem-ID Value (Offset 0x0C):   TPMC150-10 0x000A

TPMC150-11 0x000B

TPMC150-12 0x000C

TPMC150-13 0x000D

## 4.1.2 PCI Base Address Initialization

**PCI Base Address Initialization is scope of the PCI host software.**

**PCI9030 PCI Base Address Initialization:**

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.

2. Read back the PCI9030 PCI Base Address Register.

3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = '0': Expansion ROM not used

   Bit 0 = '1': Expansion ROM used

4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

**After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.**

| Offset in Config. | Description | Usage |
|---|---|---|
| 0x10 | PCI9030 LCR's MEM | Used |
| 0x14 | PCI9030 LCR's I/O | Used |
| 0x18 | PCI9030 Local Space 0 | Used |
| 0x1C | PCI9030 Local Space 1 | Not used |
| 0x30 | Expansion ROM | Not used |

Figure 4-2 : PCI9030 PCI Base Address Usage

## 4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

**The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).**

**Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.**

| Offset from PCI Base Address | Register | Value | Description |
|---|---|---|---|
| 0x00 | Local Address Space 0 Range | 0x0FFF FF80 | Memory space |
| 0x04 | Local Address Space 1 Range | 0x0000 0000 | Not used |
| 0x08 | Local Address Space 2 Range | 0x0000 0000 | Not used |
| 0x0C | Local Address Space 3 Range | 0x0000 0000 | Not used |
| 0x10 | Local Exp. ROM Range | 0x0000 0000 | Not used |
| 0x14 | Local Re-map Register Space 0 | 0x0000 0001 | Enabled, Offset 0 |
| 0x18 | Local Re-map Register Space 1 | 0x0000 0000 | Not used |
| 0x1C | Local Re-map Register Space 2 | 0x0000 0000 | Not used |
| 0x20 | Local Re-map Register Space 3 | 0x0000 0000 | Not used |
| 0x24 | Local Re-map Register ROM | 0x0000 0000 | Not used |
| 0x28 | Local Address Space 0 Descriptor | 0x01B1 7B60 | Local timing |
| 0x2C | Local Address Space 1 Descriptor | 0x0000 0000 | Not used |
| 0x30 | Local Address Space 2 Descriptor | 0x0000 0000 | Not used |
| 0x34 | Local Address Space 3 Descriptor | 0x0000 0000 | Not used |
| 0x38 | Local Exp. ROM Descriptor | 0x0000 0000 | Not used |
| 0x3C | Chip Select 0 Base Address | 0x0000 0041 | Chip select |
| 0x40 | Chip Select 1 Base Address | 0x0000 0000 | Not used |
| 0x44 | Chip Select 2 Base Address | 0x0000 0000 | Not used |
| 0x48 | Chip Select 3 Base Address | 0x0000 0000 | Not used |
| 0x4C | Interrupt Control/Status | 0x0043 | Interrupt configuration |
| 0x4E | EEPROM Write Protect Boundary | 0x0030 | Standard write protection |
| 0x50 | Miscellaneous Control Register | 0x0078 0000 | Retry delay = max |
| 0x54 | General Purpose I/O Control | 0x0000 0000 | All pins are outputs |
| 0x70 | Hidden1 Power Management data select | 0x0000 0000 | Not used |
| 0x74 | Hidden 2 Power Management data scale | 0x0000 0000 | Not used |

Figure 4-3 : PCI9030 Local Configuration Register

## 4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values

- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values

- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

| Address | Offset | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
|         | 0x00   | 0x02   | 0x04   | 0x06   | 0x08   | 0x0A   | 0x0C   | 0x0E   |
| 0x00    | 0x0096 | 0x1498 | 0x0280 | 0x0000 | 0x1180 | 0x000A | s.b.   | 0x1498 |
| 0x10    | 0x0000 | 0x0040 | 0x0000 | 0x0100 | 0x4801 | 0x0001 | 0x0000 | 0x0000 |
| 0x20    | 0x0000 | 0x0000 | 0x0000 | 0x0003 | 0x0FFF | 0xFF80 | 0x0000 | 0x0000 |
| 0x30    | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0001 |
| 0x40    | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 |
| 0x50    | 0x01B1 | 0x7B60 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 |
| 0x60    | 0x0000 | 0x0000 | 0x0000 | 0x0041 | 0x0000 | 0x0000 | 0x0000 | 0x0000 |
| 0x70    | 0x0000 | 0x0000 | 0x0030 | 0x0043 | 0x0078 | 0x0000 | 0x0000 | 0x0000 |
| 0x80    | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0x90    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xA0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xB0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xC0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xD0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xE0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xF0    | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |

Figure 4-4 : Configuration EEPROM TPMC150-xx

Subsystem-ID Value (Offset 0x0C):     TPMC150-10 0x000A

TPMC150-11 0x000B

TPMC150-12 0x000C

TPMC150-13 0x000D

## 4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

**CNTRL[30] PCI Adapter Software Reset:**

Value of 1 resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

# 5 Configuration Hints

## 5.1 Software Reset (Controller and LRESET#)

A host on the PCI bus can set the software reset bit in the Miscellaneous Control Register (CNTRL; 0x50) of the PCI Controller PCI9030 to reset the Controller and assert LRESET# output. The PCI9030 remains in this reset condition until the PCI host clears the software reset bit.

## 5.2 Big / Little Endian

- PCI – Bus ( Little Endian )

| Byte 0 | AD[7..0] |
|--------|----------|
| Byte 1 | AD[15..8] |
| Byte 2 | AD[23..16] |
| Byte 3 | AD[31..24] |

- Every Local Address Space (0...3) and the Expansion ROM Space can programmed to operate in Big or Little Endian Mode.

| Big Endian | | Little Endian | |
|------------|---------|---------------|---------|
| **32 Bit** | | **32 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| Byte 1 | D[23..16] | Byte 1 | D[15..8] |
| Byte 2 | D[15..8] | Byte 2 | D[23..16] |
| Byte 3 | D[7..0] | Byte 3 | D[31..24] |
| **16 Bit upper lane** | | **16 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| Byte 1 | D[23..16] | Byte 1 | D[15..8] |
| **16 Bit lower lane** | | | |
| Byte 0 | D[15..8] | | |
| Byte 1 | D[7..0] | | |
| **8 Bit upper lane** | | **8 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| **8 Bit lower lane** | | | |
| Byte 0 | D[7..0] | | |

Figure 5-1 : Local Bus Little/Big Endian

**Standard use of the TPMC150:**

| | |
|---|---|
| Local Address Space 0 | 32 bit bus in Big Endian Mode |
| Local Address Space 1 | not used |
| Local Address Space 2 | not used |
| Local Address Space 3 | not used |
| Expansion ROM Space | not used |

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the Mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9030 manual which is also part of the TPMC150-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

| Short cut Offset | Name | |
|---|---|---|
| LAS0BRD | 0x28 | Local Address Space 0 Bus Region Description Register |
| LAS1BRD | 0x2C | Local Address Space 0 Bus Region Description Register |
| LAS2BRD | 0x30 | Local Address Space 0 Bus Region Description Register |
| LAS3BRD | 0x34 | Local Address Space 0 Bus Region Description Register |
| EROMBRD | 0x38 | Expansion ROM Bus Region Description Register |

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

# 5.3 Local read/write

The local register design is developed for a long word (32 bit) read/write access. A byte or word access could fail.

# 5.4 Changing Resolution on the Fly

A technique used to increase the tracking rate while maintaining low speed accuracy is to switch the resolution of the converter on the fly (sometimes called gear shifting). This allows the user to increase resolution when the input is changing at slow speeds, or decrease the resolution when high tracking rates are required. This change is accomplished by simply changing the digital resolution controls.

However, the change in resolution will introduce a transient in the output code as well as the velocity. This is due to internal gain changes when the resolution is switched.

This technique can also be used to reduce errors from large input steps or over velocity conditions. When the Build-In-Test of the converter indicates an error, the resolution can be changed from its programmed value one step down to a lower resolution. This allows the converter to settle out faster.

## 5.5 Operating Modes

### 5.5.1 Converter Operating Modes

#### 5.5.1.1 Operating with Synchronous Status Latch

Operating with Synchronous Status Latch is separately selected for each channel if CH_SYN_LAT of the respective Channel Control Register is set to '1'. In this case, the Channel Status Register latches the status at Channel Data Register read time. The latch is released by a read access to the Channel Status Register. Subsequent reads to the Channel Data Register without reading the Channel Status Register will leave the Status Register unchanged, i.e. the latched Status Register will not be updated.

Sequence:

| | |
|---|---|
| read Data | → freeze the status at data read |
| read Status | → release status latch |
| check Build-In-Test | → If CH_STA_BIT is read as '0', the data value is valid |

#### 5.5.1.2 Operating with Synchronous Conversion

Operating with Synchronous Conversion for Channel 1 and Channel 2 is selected if CH_SYN_CON of the Channel 1 Control Register is set to '1'. Operating with Synchronous Conversion for Channel 3 and Channel 4 is selected if CH_SYN_CON of the Channel 3 Control Register is set to'1'. In this case the value of channel 2 (channel 4) is converted simultaneously with channel 1 (channel 3). Status Registers are latched at Channel 1 (Channel 3) Data Register read time if the Synchronous Status Latch is enabled.

Sequence (example for channel 1 & 2):

| | |
|---|---|
| read channel 1 data | → start conversion for channel 1 and 2 |
| | → latch the status for channel 1 and 2 (if Synchronous Status Latch enabled) |
| read channel 1 status | → release latch of Channel 1 Status Register (if enabled) |
| read channel 2 data | → release Channel 2 Data Register |
| read channel 2 status | → release latch of Channel 2 Status Register (if enabled) |
| Check Build-In-Test of both status registers | → If CH_STA_BIT is read as '0', the data value is valid. |

This feature may be useful, when two-speed-resolvers (coarse and fine) are used. Refer to the RDC19230 manual available on www.ddc-web.com for a software example.

### 5.5.1.3 Multiple Converter Read

If the Multiple Converter Read feature is used for the Channel Data Registers, a read access to one of the enabled Channel Data Registers starts a conversion for all the enabled converters at the same time. The data will be latched. The latched Channel Data Registers can then be read one after the other. A new Multiple Converter Read access is only possible after finishing the read of all latched Channel Data Registers.

During a Multiple Converter Read access CTRL_CON_STA is set to the value '1'. CTRL_CON_STA changes to '0' after the last read access to the enabled and latched Channel Data Registers.

The 'Synchronous Status Latch' and 'Synchronous Conversion' are not affected by this feature and will work as usual.

Registers may be reread within the multiple read sequence und will then contain current data. This will not affect the remaining unread registers.

## 5.5.2  Encoder Operating Modes

The Encoder Emulation is activated by writing a '1' to the CH_EMU_EN in the Channel Control Register. When CH_EMU_EN is set to '1', the current converter resolution is latched and used for the Incremental Encoder Emulation.

> **The converter resolution can be changed after the Incremental Encoder Emulation resolution is set, but it must not be less than the resolution of the Incremental Encoder Emulation. If the converter resolution is less then the Incremental Encoder Emulation resolution, there will be no Encoder Emulation output!**

To enable the Incremental Encoder Emulation with a certain resolution and change the converter resolution afterwards, following steps have to be done:

Write access: Set the resolution to be used for the Incremental Encoder Emulation

Write access: Enable the Incremental Encoder Emulation

Write access: Set the converter resolution

### 5.5.2.1 Incremental Encoder Emulation Output

The Incremental Encoder Emulation Output can be used for systems that are designed to interface with incremental optical encoders. To enable the Encoder Emulation Output, write a '1' to the CH_EMU_OUT in the Channel Control Register.

The number of encoder pulses per revolution is dependent of the programmed Incremental Encoder Emulation Resolution:

| Resolution/Bit | 10 | 12 | 14 | 16 |
|---|---|---|---|---|
| Encoder pulses per revolution | 256 | 1024 | 4096 | 16384 |

Figure 5-2 : Incremental Encoder Resolution

The index pulse is high, when all the bits of the converter data are zero. If the converter resolution is programmed differently than the resolution of the Incremental Encoder Emulation the converter resolution will determine the resolution of the index pulse.

## 5.5.2.2 Encoder Signal Analysis Mode

The CH_ ESAM bits of the Channel Control Register define the encoder counter clock generation.

| Value | | Mode |
|---|---|---|
| 0 | 0 | disable Counter |
| 0 | 1 | 1x – single |
| 1 | 0 | 2x – double |
| 1 | 1 | 4x – quad |

Figure 5-3 : Encoder Signal Analysis Modes

The encoder counter can be programmed to interpret the encoder inputs as 1x, 2x or 4x clock, as described in figure 'Encoder Signal Analysis Modes' before.
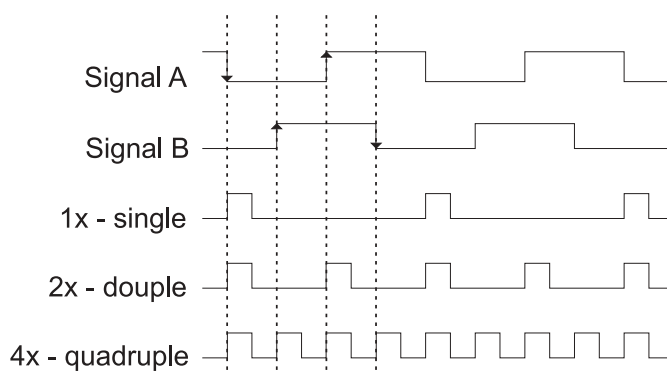


Figure 5-4 : Encoder signal interpretation

| Encoder Signal Analysis Modes | Resolution/Bit | | | |
|---|---|---|---|---|
| | 10 | 12 | 14 | 16 |
| **1x – single** | 256 | 1024 | 4096 | 16384 |
| **2x – double** | 512 | 2048 | 8192 | 32768 |
| **4x – quad** | 1024 | 4096 | 16384 | 65536 |

Figure 5-5 : Encoder count per revolution

To let the encoder counter count with the same resolution as set for encoder emulation, the Encoder Signal Analysis Mode must be set to 4x.

## 5.5.2.3 Reference Mode

The CH_REF bits of the Channel Control Register control the Encoder Reference Mode. The following table shows the available configurations:

| Value | | Mode |
|---|---|---|
| 0 | 0 | None Reference Mode |
| 0 | 1 | Reference Mode |
| 1 | 0 | Auto Reference Mode |
| 1 | 1 | Index Mode |

Figure 5-6 : Encoder Reference Modes

**None Reference Mode**

In this mode there is no automatic preload of the encoder counter. Only a manual is possible. To make an encoder counter preload in this mode, a write access to the CTRL_PRE bits in the Global Control/Status Register is necessary.

**Reference Mode**

This mode controls the encoder counter with the corresponding digital 24V input (used as reference input) and the encoder index signal. A specified reference input signal and a following index impulse produce a counter preload. The host software must set the motion direction during such a reference access to backward.

The following figure shows the two normal preload accesses. An encoder motion area with eleven index pulses and the corresponding reference input is described as an example.
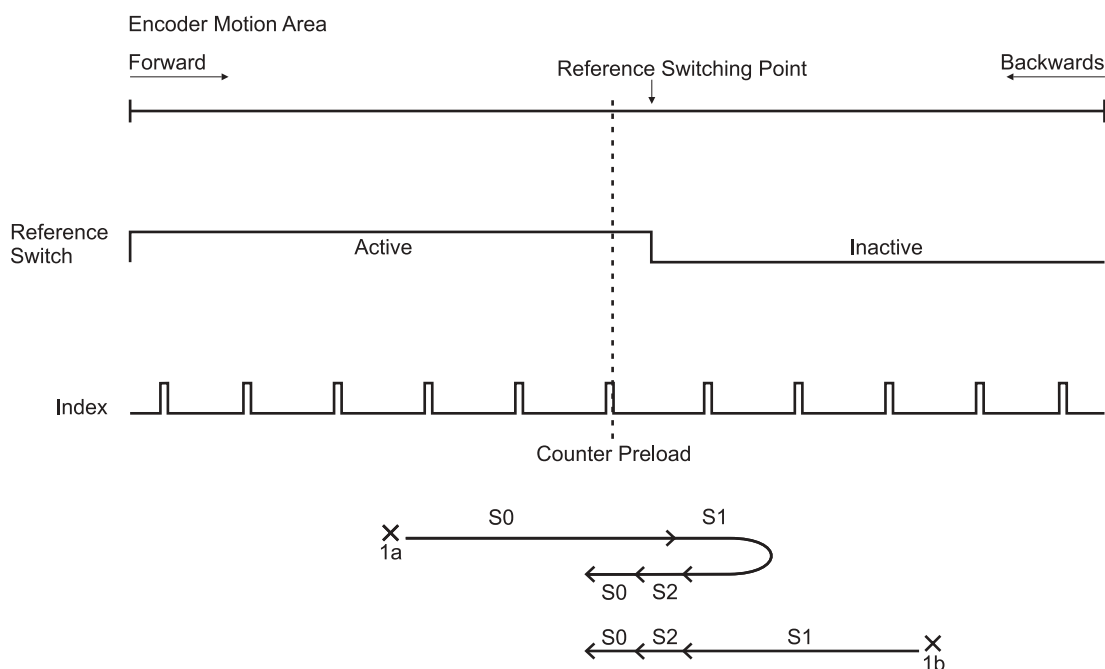


Figure 5-7 : Encoder preload example

Two different 'start positions' (1a and 1b) are shown:

**Position 1a:**

Direction is forward and the reference input is active. The host software must move into the area where the reference input is inactive. Now the direction must be changed. The next index pulse after entering the area with reference input active triggers the preload function of the encoder counter.

**Position 1b:**

Direction is backwards and the reference input is inactive. The host software must move further backwards, and after entering the area with reference input active the next index pulse triggers the preload function of the encoder counter.

A correct execution of the reference function can be monitored in the Channel Control Register. After successful execution the mode of this encoder is changed from bit combination '01' (Reference Mode) to '00' (None Reference Mode).

**It must be guaranteed that the encoder motion area is divided into two areas, one with reference input active and one with reference input inactive.**

**Auto Reference Mode**

This mode is the automation of the Reference Mode. That means every time the reference switching point and a following index pulse are crossed during backwards direction, a new preload is generated. **In Auto Reference Mode there is no change of the mode in the Channel Control Register!**

**Index Mode**

In this mode the digital 24V input is not used. Only the index impulse produces a counter preload. After setting this mode, the next occurrence of the index signal, independent from direction, will preload the counter. A correct execution of this preload function can be monitored in the Channel Control Register. After successful execution the mode of this encoder is set from bit combination '11' (Index) to '00' (None Reference Mode).

## 5.5.2.4 Multiple Encoder Read

If the Multiple Encoder Read feature is used for the Encoder Counter Data Registers, a read access one of the enabled Encoder Counter Data Registers latches all counter values for the enabled counters at the same time. Then the Encoder Counter Data Registers can be read one after the other. A new Multiple Encoder Read access is only possible after finishing the read of all latched Encoder Counter Data Registers.

During a Multiple Encoder Read access CTRL_ENC_STA is set to the value '1'. CTRL_ENC_STA changes to '0' after the last read access to the enabled and latched Encoder Counter Data Registers.

Registers may be reread within the multiple read sequence und will then contain current data. This will not affect the remaining unread registers.

## 5.6 Binary Angle Relationships

| Resolution in Bits | $2^n$ | LSB as % of full scale | Degrees/Bit | Minutes/Bit | Radians/Bit |
|---|---|---|---|---|---|
| 0 | 1 | 100 | 360 | 21600 | 6.28318531 |
| 1 | 2 | 50 | 180 | 10800 | 3.14159265 |
| 2 | 4 | 25 | 90 | 5400 | 1.57079633 |
| 3 | 8 | 12.5 | 45 | 2700 | 0.78539816 |
| 4 | 16 | 6.25 | 22.5 | 1350 | 0.39269908 |
| 5 | 32 | 3.125 | 11.25 | 675 | 0.19634954 |
| 6 | 64 | 1.5625 | 5.625 | 337.5 | 0.09817477 |
| 7 | 128 | 0.78125 | 2.8125 | 168.75 | 0.04908739 |
| 8 | 256 | 0.390625 | 1.40625 | 84.375 | 0.02454369 |
| 9 | 512 | 0.1953125 | 0.703125 | 42.1875 | 0.01227185 |
| 10 | 1024 | 0.09765625 | 0.3515625 | 21.09375 | 0.00613592 |
| 11 | 2048 | 0.04882813 | 0.1757813 | 10.54686 | 0.00306796 |
| 12 | 4096 | 0.02441406 | 0.0878906 | 5.27344 | 0.00153398 |
| 13 | 8192 | 0.01220703 | 0.0439453 | 2.63672 | 0.00076699 |
| 14 | 16384 | 0.00610352 | 0.0219727 | 1.31836 | 0.00038350 |
| 15 | 32768 | 0.00305176 | 0.0109863 | 0.65918 | 0.00019175 |
| 16 | 65536 | 0.00152588 | 0.0054932 | 0.32959 | 0.00009587 |

Figure 5-8 : Binary Angle Relationships

Angle in degrees = $\dfrac{Data \cdot 360°}{2^{16}}$

Angle in minutes = $\dfrac{Data \cdot 21600'}{2^{16}}$

Angle in radians = $\dfrac{Data \cdot 2\pi}{2^{16}}$

# 6  Signal Conditioning Adapter

Each synchro/resolver channel has to be equipped with a Signal Conditioning Adapter (TPMC150-Ay-xx) to adapt the signal levels of the synchro/resolver to the RDC19230 inputs and to configure the optional reference oscillator input/output. Each channel can be equipped with an individual Signal Conditioning Adapter, it is not necessary to equip all channels with the same adapter. The Signal Conditioning Adapters will be built individually to customer specification of the synchro or resolver specifications (replacing the 'xx'). The adapters are factory installed on the TPMC150.
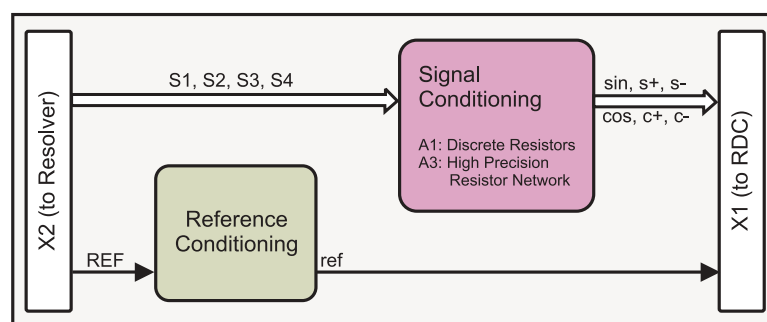


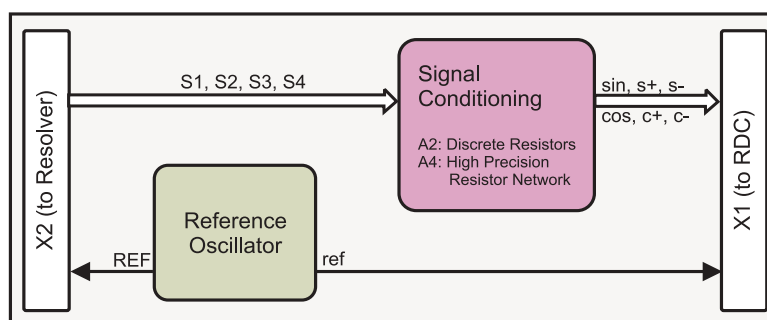Figure 6-1 : Signal Conditioning Adapter TPMC150-A1/A3



Figure 6-2 : Signal Conditioning Adapter TPMC150-A2/A4 with reference oscillator

Four types of Signal Conditioning Adapters are available: The TPMC150-A1 and the TPMC150-A2 use high precision, low TK discrete resistors. These adapters are mainly used for resolver applications. The TPMC150-A3 and the TPMC150-A4 use a high precision resistor network with matched resistors. These adapters are mainly used for synchro applications or resolver applications which require highest accuracy. Additionally the TPMC150-A2 and the TPMC150-A4 offer an on board reference oscillator with factory selectable frequencies in the range of 2 kHz to 10 kHz.

| Main Variant | A1 | A2 | A3 | A4 |
|---|---|---|---|---|
| Discrete resistors | X | X | | |
| Resistor network | | | X | X |
| Resolver | X | X | X | X |
| Synchro | | | X | X |
| High accuracy | | | X | X |
| Reference oscillator | | X | | X |

Figure 6-3 : TPMC150 Adapter Variants

# 6.1 Signal Conditioning Adapter Characteristics

| Reference Oscillator Output | | |
|---|---|---|
| Frequency | 1-10 kHz, factory selectable | |
| Amplitude | Max. 11.8V / 70mA | |
| Signal Input | | |
| Frequency | Resolution dependent | |
| Signal Voltage | Factory selectable | |
| Reference Input Voltage | Factory selectable | |
| Physical Data | | |
| Power Requirements (TPMC150-A2/A4 only, no load) | 8mA typical @ +5V DC<br>8mA typical @ -5V DC<br>5mA typical @ +12V DC<br>5mA typical @ -12V DC | |
| Temperature Range | Operating | -40°C to +85 °C |
| | Storage | -40°C to +125°C |
| MTBF | 1 880 000 h (TPMC150-A1)<br>1 300 000 h (TPMC150-A2)<br>1 901 000 h (TPMC150-A3)<br>1 310 000 h (TPMC150-A4) | |
| Humidity | 5 – 95 % non-condensing | |
| Weight | 2-3 g | |

Figure 6-4 : Technical Specification TPMC150-A1 – TPMC150-A4

## 6.2 Required Synchro/Resolver specifications

To find a Signal Conditioning Adapter that fits to your synchro/resolver, TEWS TECHNOLOGIES requires the synchro/resolver specification. These are:

- Sensor type (resolver/synchro)

- Signal voltage (resolver: single ended/differential)

- Reference input voltage (single ended/differential)

- Optional: Reference output voltage/frequency

## 6.3 Connector Pin Assignments

### 6.3.1   20 Pin Connector – Front I/O Side

Function and pin numbers are valid for X2, X4, X6, X8

| Pin | Function | Dir. | Pin | Function | Dir. |
|-----|----------|------|-----|----------|------|
| 1 | +REF_EXT | in/out | 2 | n.c. | - |
| 3 | n.c. | - | 4 | -REF_EXT | in/out |
| 5 | n.c. | - | 6 | n.c. | - |
| 7 | S1 | in | 8 | n.c. | - |
| 9 | n.c. | - | 10 | S2 | in |
| 11 | n.c. | - | 12 | n.c. | - |
| 13 | S3 | in | 14 | n.c. | - |
| 15 | n.c. | - | 16 | S4 | in |
| 17 | n.c. | - | 18 | n.c. | - |
| 19 | n.c. | - | 20 | n.c. | - |

Figure 6-5 : Pin Assignment - 20 Pin Connector Front I/O Side

## 6.3.2  20 Pin Connector - Converter Side

Function and pin numbers are valid for X1, X3, X5, X7

| Pin | Function | Dir. | Pin | Function | Dir. |
|-----|----------|------|-----|----------|------|
| 1 | -REF | out | 2 | +REF | out |
| 3 | +5 V | - | 4 | -12 V | - |
| 5 | +C | out | 6 | LOS | out |
| 7 | COS | out | 8 | n.c. | - |
| 9 | -C | out | 10 | n.c. | - |
| 11 | +S | out | 12 | n.c. | - |
| 13 | Sin | out | 14 | n.c. | - |
| 15 | -S | out | 16 | n.c. | - |
| 17 | -5 V | - | 18 | +12 V | - |
| 19 | AGND | - | 20 | GND | - |

Figure 6-6 : Pin Assignment - 20 Pin Connector Converter Side

# 7  <u>Installation Hints</u>

> **When a 90V signal input is used, make sure that the voltage rating of the I/O connector is sufficient to operate with the signal voltage.**

Suggested mating connectors:

HARTING: *har-mik* series, 6003 068 5210

> **Make sure that the cable used to connect the TPMC150 with the synchro/resolver also has a voltage rating which is sufficient for the signal voltage.**

Due to the concept of Signal Conditioning Adapter (TPMC150-Ay-xx), the TPMC150 uses the maximum board height which is allowed by the PMC specification.

> **To avoid damage of the carrier board and/or of the TPMC150 please make sure that there are no conductive components like ceramic PGA's under the PMC socket used for the TPMC150.**
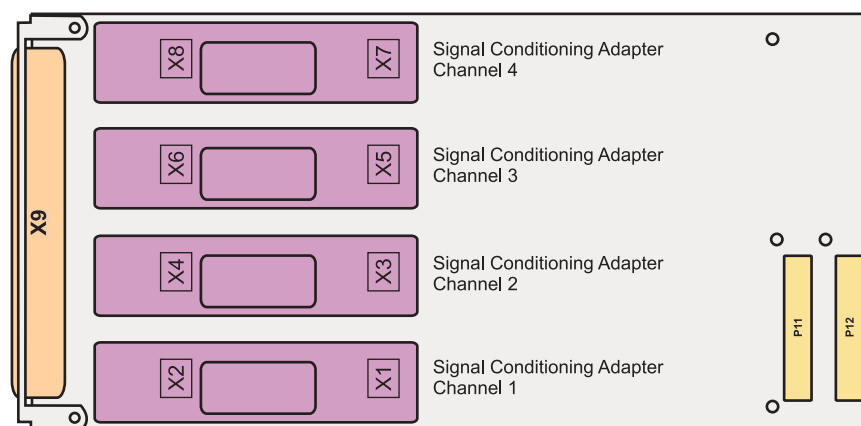


Figure 7-1 : TPMC150 Adapter Placement

## 7.1 Connection Examples

The following pages display several examples how to connect different synchro/resolver configurations to the TPMC150. All examples refer to channel 1. The other channels are connected accordingly (for pin numbers refer to the pin assignment table in chapter 'Pin Assignment').
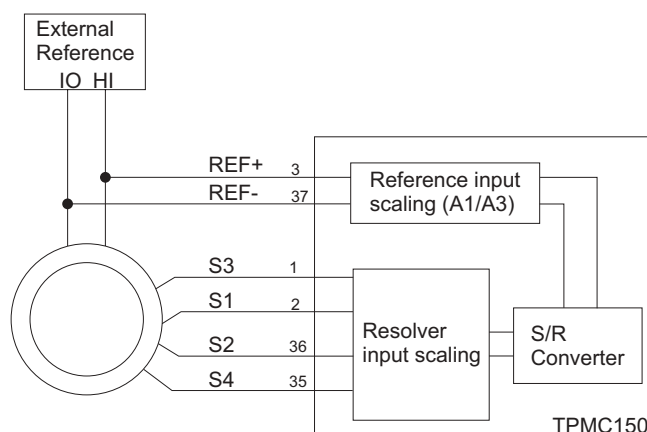
### 7.1.1  Resolver with external reference



Figure 7-2 : Resolver with external reference
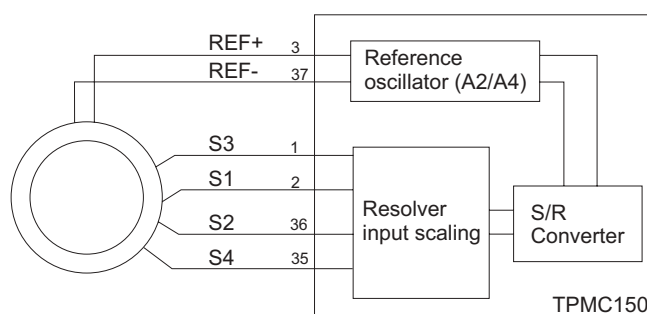
### 7.1.2  Resolver with internal reference



Figure 7-3 : Resolver with internal reference

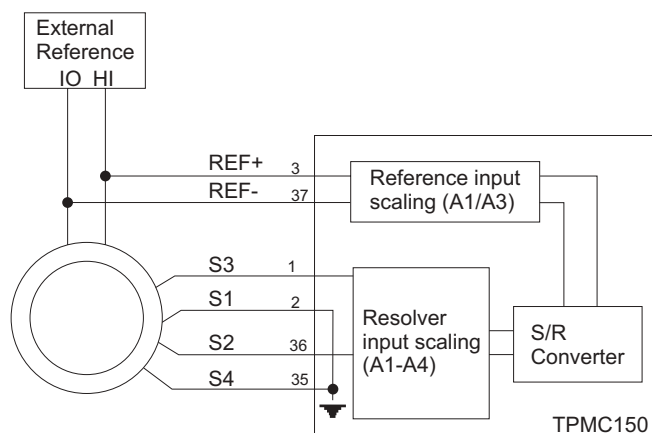## 7.1.3  Single ended resolver with external reference

Figure 7-4 : Single ended resolver with external reference
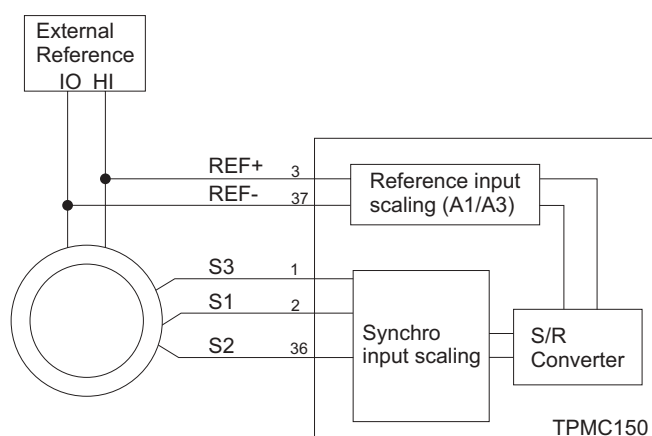
## 7.1.4  Synchro with external reference

Figure 7-5 : Synchro with external reference

# 8 Pin Assignment – I/O Connector

The complete TPMC150 I/O interface is available on the HD68 SCSI-3 type connector ("front I/O"). There is no PMC P14 I/O.

| Pin | Function | Dir. | Pin | Function | Dir. |
|-----|----------|------|-----|----------|------|
| 1 | Channel 1 S3 (sin+) | in | 35 | Channel 1 S4 (cos-) | in |
| 2 | Channel 1 S1 (sin-) | in | 36 | Channel 1 S2 (cos+) | in |
| 3 | Channel 1 Reference+ | in/out | 37 | Channel 1 Reference- | in/out |
| 4 | Channel 1 A- | out | 38 | Channel 1 A+ | out |
| 5 | Channel 1 B- | out | 39 | Channel 1 B+ | out |
| 6 | Channel 1 ZI- | out | 40 | Channel 1 ZI+ | out |
| 7 | Channel 1 Velocity output | out | 41 | AGND | |
| 8 | Channel 2 S3 (sin+) | In | 42 | Channel 2 S4 (cos-) | in |
| 9 | Channel 2 S1 (sin-) | In | 43 | Channel 2 S2 (cos+) | in |
| 10 | Channel 2 Reference + | in/out | 44 | Channel 2 Reference - | in/out |
| 11 | Channel 2 A- | out | 45 | Channel 2 A+ | out |
| 12 | Channel 2 B- | out | 46 | Channel 2 B+ | out |
| 13 | Channel 2 ZI- | out | 47 | Channel 2 ZI+ | out |
| 14 | Channel 2 Velocity output | out | 48 | AGND | |
| 15 | Channel 3 S3 (sin+) | in | 49 | Channel 3 S4 (cos-) | in |
| 16 | Channel 3 S1 (sin-) | in | 50 | Channel 3 S2 (cos+) | in |
| 17 | Channel 3 Reference + | in/out | 51 | Channel 3 Reference - | in/out |
| 18 | Channel 3 A- | out | 52 | Channel 3 A+ | out |
| 19 | Channel 3 B- | out | 53 | Channel 3 B+ | out |
| 20 | Channel 3 ZI- | out | 54 | Channel 3 ZI+ | out |
| 21 | Channel 3 Velocity output | out | 55 | AGND | |
| 22 | Channel 4 S3 (sin+) | in | 56 | Channel 4 S4 (cos-) | in |
| 23 | Channel 4 S1 (sin-) | in | 57 | Channel 4 S2 (cos+) | in |
| 24 | Channel 4 Reference + | in/out | 58 | Channel 4 Reference - | in/out |
| 25 | Channel 4 A- | out | 59 | Channel 4 A+ | out |
| 26 | Channel 4 B- | out | 60 | Channel 4 B+ | out |
| 27 | Channel 4 ZI- | out | 61 | Channel 4 ZI+ | out |
| 28 | Channel 4 Velocity output | out | 62 | AGND | |
| 29 | NC | | 63 | NC | |
| 30 | NC | | 64 | NC | |
| 31 | DI_GND 1 | | 65 | DI_GND 2 | |
| 32 | Digital Input 1 | in | 66 | Digital Input 2 | in |
| 33 | DI_GND 3 | | 67 | DI_GND 4 | |
| 34 | Digital Input 3 | in | 68 | Digital Input 4 | in |

Figure 8-1 : Pin Assignment I/O Connector