

TPN2R503NC

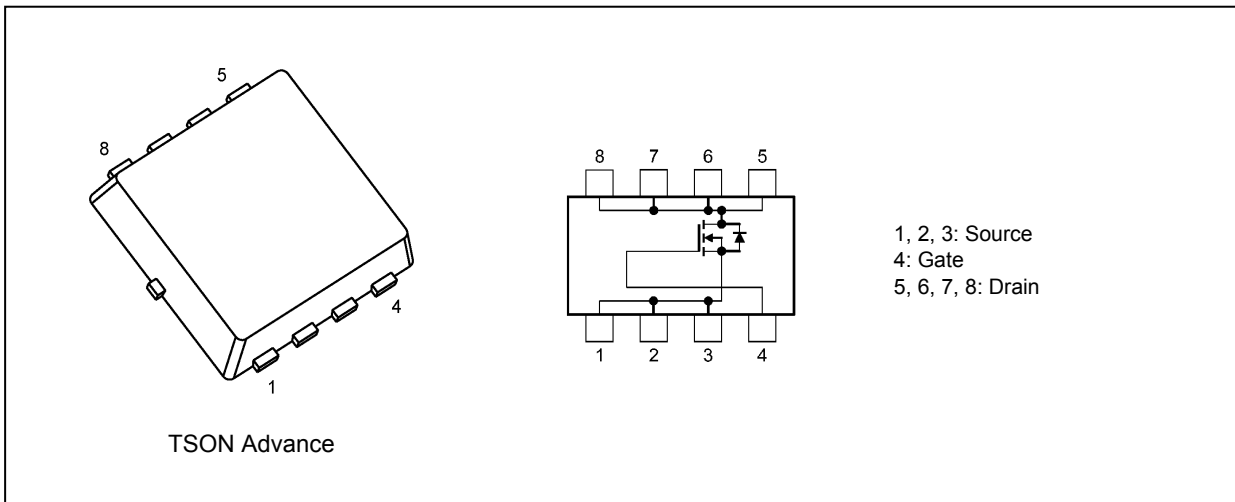
1. Applications

- Power Management Switches

2. Features

- (1) Small footprint due to a small and thin package
- (2) Low drain-source on-resistance: $R_{DS(ON)} = 2.1 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (3) Low leakage current: $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 30 \text{ V}$)
- (4) Enhancement mode: $V_{th} = 1.3 \text{ to } 2.3 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 0.5 \text{ mA}$)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Rating | Unit |
|--|-----------|------------|------------------|
| Drain-source voltage | V_{DSS} | 30 | V |
| Gate-source voltage | V_{GSS} | ± 20 | |
| Drain current (DC) (Silicon limit) (Note 1), (Note 2) | I_D | 85 | A |
| Drain current (DC) (Note 1) | I_D | 40 | |
| Drain current (pulsed) ($t = 1 \text{ ms}$) (Note 1) | I_{DP} | 120 | |
| Power dissipation ($T_c = 25^\circ\text{C}$) | P_D | 35 | W |
| Power dissipation ($t = 10 \text{ s}$) (Note 3) | P_D | 1.9 | W |
| Power dissipation ($t = 10 \text{ s}$) (Note 4) | P_D | 0.7 | W |
| Single-pulse avalanche energy (Note 5) | E_{AS} | 62 | mJ |
| Avalanche current | I_{AR} | 40 | A |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to 150 | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2012-11

5. Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|--|-----------------------|------|------|
| Channel-to-case thermal resistance (T _c = 25°C) | R _{th(ch-c)} | 3.57 | °C/W |
| Channel-to-ambient thermal resistance (t = 10 s) (Note 3) | R _{th(ch-a)} | 65.7 | °C/W |
| Channel-to-ambient thermal resistance (t = 10 s) (Note 4) | R _{th(ch-a)} | 178 | °C/W |

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon capability. Package limit is 45 A.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 30 μH, R_G = 1 Ω, I_{AR} = 40 A



Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)



Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

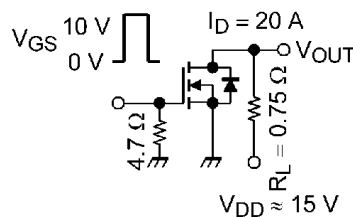
6.1. Static Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---------------|---|-----|------|-----------|------------------|
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | — | — | ± 0.1 | μA |
| Drain cut-off current | I_{DSS} | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ | — | — | 10 | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$ | 30 | — | — | V |
| Drain-source breakdown voltage (Note 6) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$ | 15 | — | — | |
| Gate threshold voltage | V_{th} | $V_{DS} = 10\text{ V}, I_D = 0.5\text{ mA}$ | 1.3 | — | 2.3 | |
| Drain-source on-resistance | $R_{DS(ON)}$ | $V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$ | — | 3.2 | 4.1 | $\text{m}\Omega$ |
| | | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ | — | 2.1 | 2.5 | |

Note 6: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance | C_{iss} | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | — | 2230 | — | pF |
| Reverse transfer capacitance | C_{rss} | | — | 160 | — | |
| Output capacitance | C_{oss} | | — | 650 | — | |
| Switching time (rise time) | t_r | See Figure 6.2.1. | — | 9 | — | ns |
| Switching time (turn-on time) | t_{on} | | — | 14 | — | |
| Switching time (fall time) | t_f | | — | 24 | — | |
| Switching time (turn-off time) | t_{off} | | — | 68 | — | |



Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------|---|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | Q_g | $V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$ | — | 40 | — | nC |
| Gate-source charge 1 | Q_{gs1} | | — | 10 | — | |
| Gate-drain charge | Q_{gd} | | — | 10 | — | |

6.4. Source-Drain Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------|---|-----|------|------|------|
| Reverse drain current (pulsed) (Note 7) | I_{DRP} | — | — | — | 120 | A |
| Diode forward voltage | V_{DSF} | $I_{DR} = 40\text{ A}, V_{GS} = 0\text{ V}$ | — | — | -1.2 | V |

Note 7: Ensure that the channel temperature does not exceed 150°C .

7. Marking

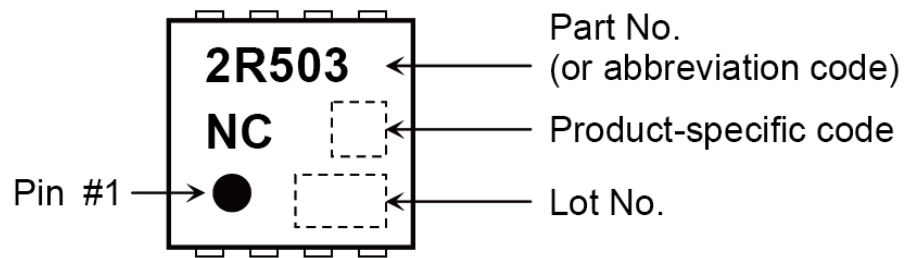


Fig. 7.1 Marking

8. Characteristics Curves (Note)

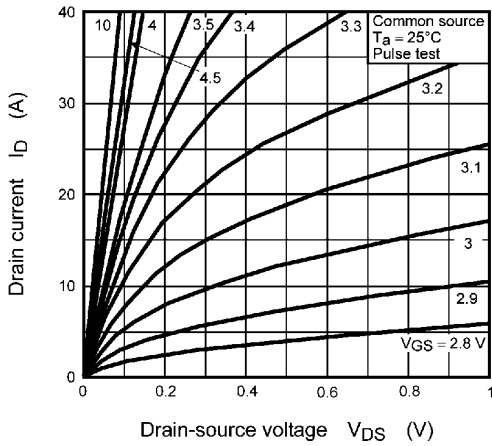


Fig. 8.1 $I_D - V_{DS}$

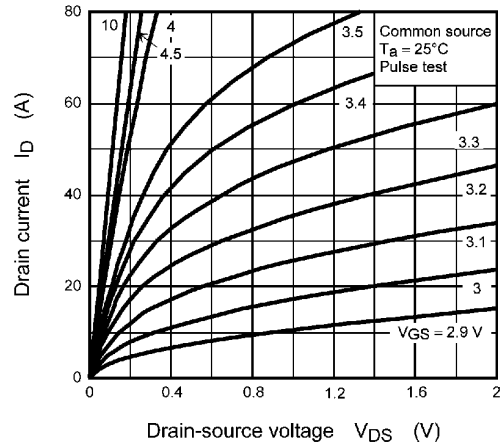


Fig. 8.2 $I_D - V_{DS}$

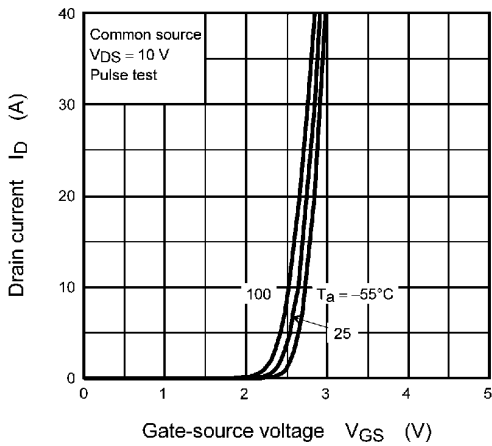


Fig. 8.3 $I_D - V_{GS}$

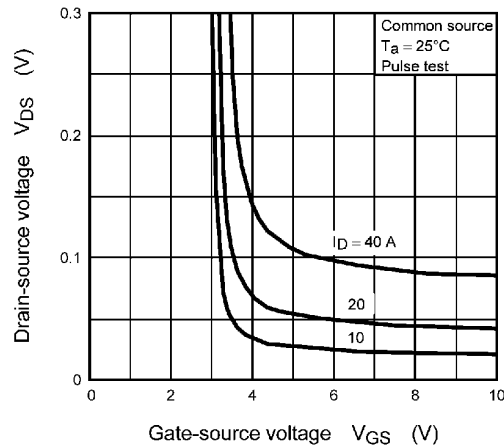


Fig. 8.4 $V_{DS} - V_{GS}$

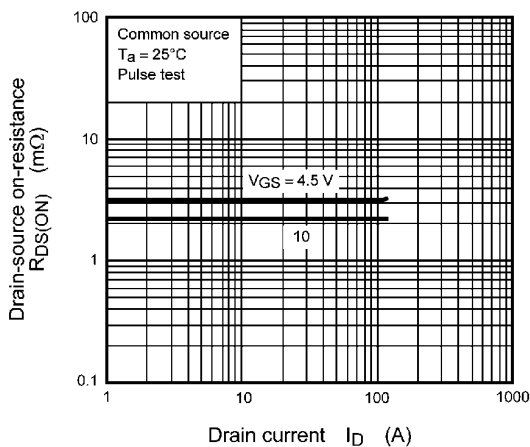


Fig. 8.5 $R_{DS(ON)} - I_D$

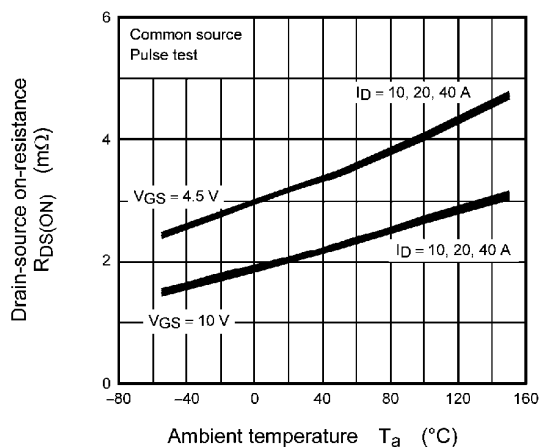


Fig. 8.6 $R_{DS(ON)} - T_a$

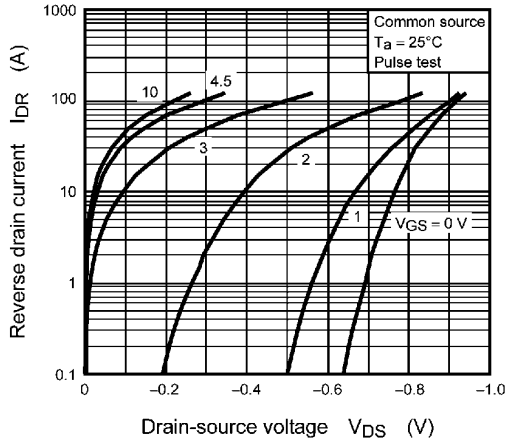


Fig. 8.7 $I_{DR} - V_{DS}$

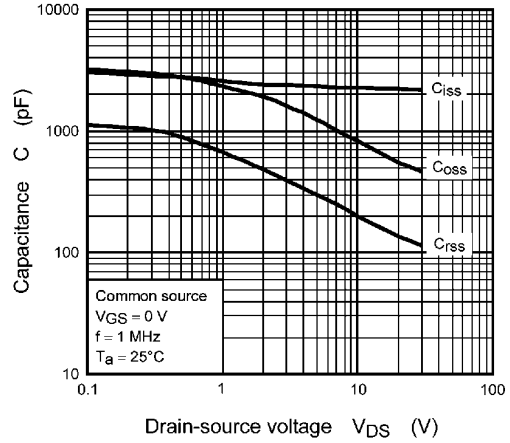


Fig. 8.8 Capacitance - V_{DS}

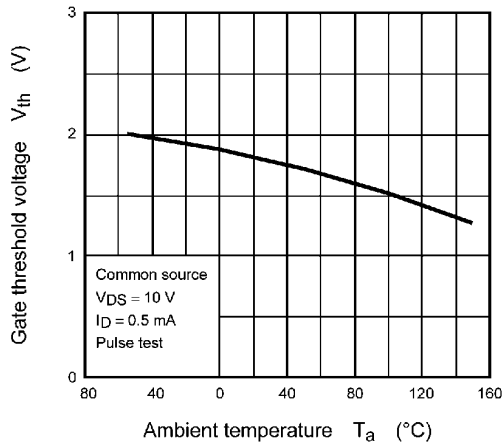


Fig. 8.9 $V_{th} - T_a$

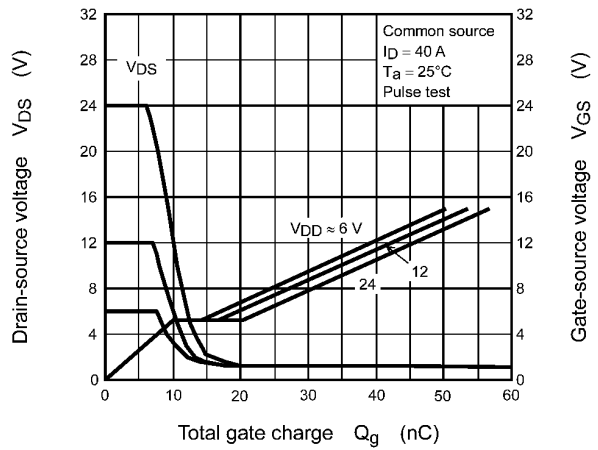
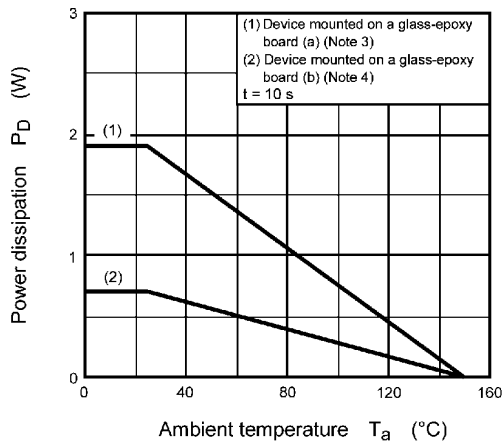
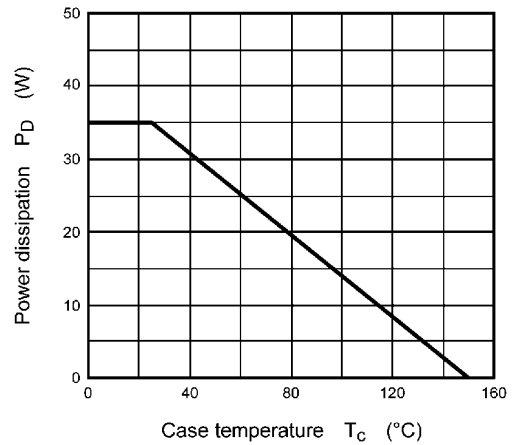


Fig. 8.10 Dynamic Input/Output Characteristics



**Fig. 8.11 $P_D - T_a$
(Guaranteed Maximum)**



**Fig. 8.12 $P_D - T_c$
(Guaranteed Maximum)**

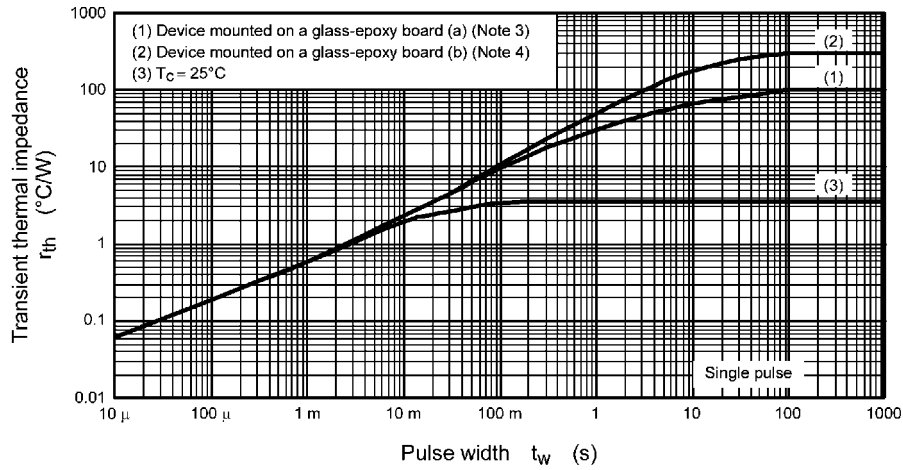


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

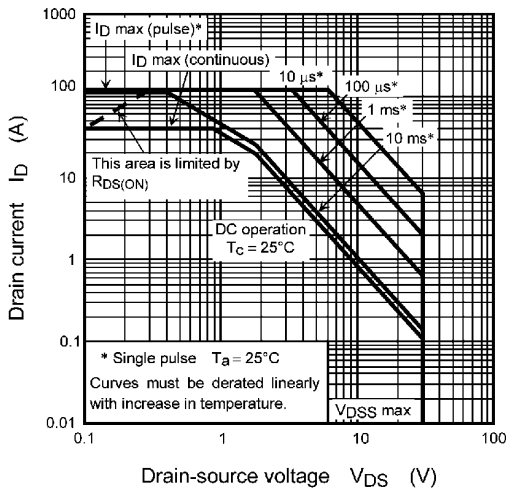


Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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