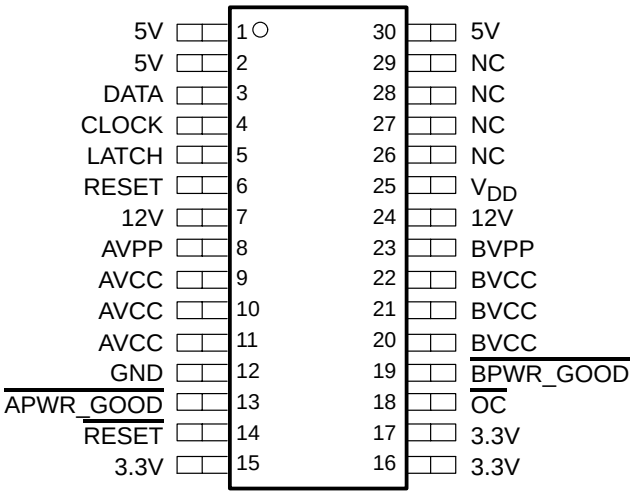
- **Fully Integrated $V_{CC}$ and $V_{pp}$ Switching for Dual-Slot PC Card™ Interface**
- **P²C™ 3-Lead Serial Interface Compatible With CardBus™ Controllers**
- **Meets PC Card Standards**
- **RESET Allows System Initialization of PC Cards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **Space-Saving 30-Pin SSOP (DB) Package**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Power Saving $I_{DD}$ = 83 μA Typ, $I_Q$ = 1 μA**
- **Low $r_{DS(on)}$ (160-mΩ $V_{CC}$ Switch)**
- **Break-Before-Make Switching**

**DB OR DF PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The TPS2202AI PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, thermal protection, and power-good reporting for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power by means of the P²C (PCMCIA Peripheral-Control) Texas Instruments nonproprietary serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to a specific card.

The TPS2202AI incorporates a reset function, selectable by one of two inputs, to help alleviate system errors. The reset function enables PC Card initialization concurrent with host platform initialization, allowing a system reset. Reset is accomplished by grounding the $V_{CC}$ and $V_{pp}$ (flash-memory programming voltage) outputs, which discharges residual card voltage.

End equipment for the TPS2202AI includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handiterminals, and bar-code scanners.

**AVAILABLE OPTIONS**

| $T_J$ | PACKAGED DEVICES | |
|---|---|---|
| | SSOP (DB)† | SSOP (DF)† |
| –40°C to 150°C | TPS2202AIDBR | TPS2202AIDFR |

† The DB and DF packages are only available taped and reeled, inidcated by the R suffix on the device type.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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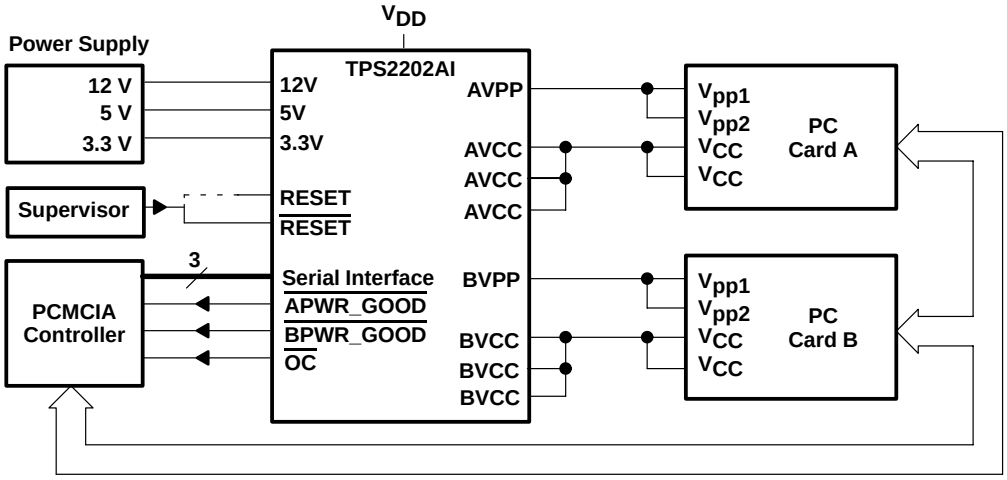
PC Card and CardBus are trademarks of PCMCIA (Personal Computer Memory Card International Association).

## typical PC card power-distribution application




### Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| 3.3V | 15, 16, 17 | I | 3.3-V $V_{CC}$ input for card power |
| 5V | 1, 2, 30 | I | 5-V $V_{CC}$ input for card power |
| 12V | 7, 24 | I | 12-V $V_{pp}$ input for card power |
| AVCC | 9, 10, 11 | O | Switched output that delivers 3.3 V, 5 V, low or high impedance to card |
| AVPP | 8 | O | Switched output that delivers 3.3 V, 5 V, 12 V, low or high impedance to card |
| $\overline{\text{APWR\_GOOD}}$ | 13 | O | Logic-level power-ready output that stays low as long as AVPP is within limits |
| BVCC | 20, 21, 22 | O | Switched output that delivers 3.3 V, 5 V, low or high impedance |
| BVPP | 23 | O | Switched output that delivers 3.3 V, 5 V, 12 V, low or high impedance |
| $\overline{\text{BPWR\_GOOD}}$ | 19 | O | Logic-level power-ready output that remains low as long as BVPP is within limits |
| CLOCK | 4 | I | Logic-level clock for serial data word |
| DATA | 3 | I | Logic-level serial data word |
| GND | 12 | | Ground |
| LATCH | 5 | I | Logic-level latch for serial data word |
| NC | 26, 27, 28, 29 | | No internal connection |
| $\overline{\text{OC}}$ | 18 | O | Logic-level overcurrent reporting output that goes low when an overcurrent condition exists |
| RESET | 6 | I | Logic-level RESET input active high. Do not connect if terminal 14 is used. |
| $\overline{\text{RESET}}$ | 14 | I | Logic-level $\overline{\text{RESET}}$ input active low. Do not connect if terminal 6 is used. |
| $V_{DD}$ | 25 | I | 5-V power to chip |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{DD}$ . . . . . –0.3 V to 7 V
Input voltage range for card power: $V_{I(5V)}$ . . . . . –0.3 V to 7 V
$V_{I(3.3V)}$ . . . . . –0.3 V to $V_{I(5V)}$
$V_{I(12V)}$ . . . . . –0.3 V to 14 V
Logic input voltage . . . . . –0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$ . . . . . internally limited
$I_{O(xVPP)}$ . . . . . internally limited
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 150°C
Operating free-air temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DF | 1158 mW | 9.26 mW/°C | 741 mW | 602 mW |
| DB | 1024 mW | 8.2 mW/°C | 655 mW | 532 mW |

‡ These devices are mounted on an FR4 board with no special thermal considerations.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 4.75 | 5.25 | V |
| Input voltage range, $V_I$ | $V_{I(5V)}$ | 0 | 5.25 | V |
| | $V_{I(3.3V)}$ | 0 | $V_{I(5V)}$§ | V |
| | $V_{I(12V)}$ | 0 | 13.5 | V |
| Output current | $I_{O(xVCC)}$ at 25°C | | 1 | A |
| | $I_{O(xVPP)}$ at 25°C | | 150 | mA |
| Clock frequency | | 0 | 2.5 | MHz |
| Operating virtual junction temperature, $T_J$ | | –40 | 125 | °C |

§ $V_{I(3.3V)}$ should not be taken above $V_{I(5V)}$.

## electrical characteristics, $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)

### dc characteristics

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Switch resistances† | 5 V to xVCC | | | | 160 | mΩ |
| | | 3.3 V to xVCC | | | | 225 | |
| | | 5 V to xVPP | | | | 6 | Ω |
| | | 3.3 V to xVPP | | | | 6 | |
| | | 12 V to xVPP | | | | 1 | |
| $V_{O(xVPP)}$ | Clamp low voltage | | $I_{pp}$ at 10 mA | | | 0.8 | V |
| $V_{O(xVCC)}$ | Clamp low voltage | | $I_{CC}$ at 10 mA | | | 0.8 | V |
| $I_{lkg}$ | Leakage current | $I_{pp}$ High-impedance state | $T_A$ = 25°C | | 1 | 10 | µA |
| | | | $T_A$ = 85°C | | | 50 | |
| | | $I_{CC}$ High-impedance state | $T_A$ = 25°C | | 1 | 10 | |
| | | | $T_A$ = 85°C | | | 50 | |
| $I_I$ | Input current | $I_{DD}$ Supply current | $V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V | | 83 | 150 | µA |
| | | $I_{DD}$ Supply current in shutdown | $V_{O(BVCC)}$ = $V_{O(AVCC)}$ = $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = Hi-Z | | | 1 | µA |
| | Power-ready threshold, $\overline{PWR\_GOOD}$ | | | 10.72 | 11.05 | 11.4 | V |
| | Power-ready hysteresis, $\overline{PWR\_GOOD}$ | 12-V mode | | | 50 | | mV |
| | Short-circuit output-current limit | $I_{O(xVCC)}$ | $T_J$ = 85°C, Output powered up into a short to GND | 0.75 | 1.3 | 1.9 | A |
| | | $I_{O(xVPP)}$ | | 120 | 200 | 400 | mA |

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

### logic section

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Logic input current | | | 1 | µA |
| Logic input high level | | 2 | | V |
| Logic input low level | | | 0.8 | V |
| Logic output high level | $I_O$ = 1 mA | $V_{DD}$ – 0.4 | | V |
| Logic output low level | | | 0.4 | V |
| Logic input minimum pulse width | | 1 | | µs |

### switching characteristics†

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_r$ | Output rise times | $V_{O(xVCC)}$ | | | 1.2 | | ms |
| | | $V_{O(xVPP)}$ | | | 5 | | |
| $t_f$ | Output fall times | $V_{O(xVCC)}$ | | | 10 | | |
| | | $V_{O(xVPP)}$ | | | 14 | | |
| $t_{pd}$ | Propagation delay (see Figure 1‡) | LATCH↑ to $V_{O(xVPP)}$ | $t_{on}$ | | 5.8 | | ms |
| | | | $t_{off}$ | | 18 | | ms |
| | | LATCH↑ to xVCC (3 V) | $t_{on}$ | | 5.8 | | ms |
| | | | $t_{off}$ | | 28 | | ms |
| | | LATCH↑ to xVCC (5 V) | $t_{on}$ | | 4 | | ms |
| | | | $t_{off}$ | | 30 | | ms |

† Refer to Parameter Measurement Information
‡ Propagation delays are with $C_L$ = 100 μF.

## PARAMETER MEASUREMENT INFORMATION

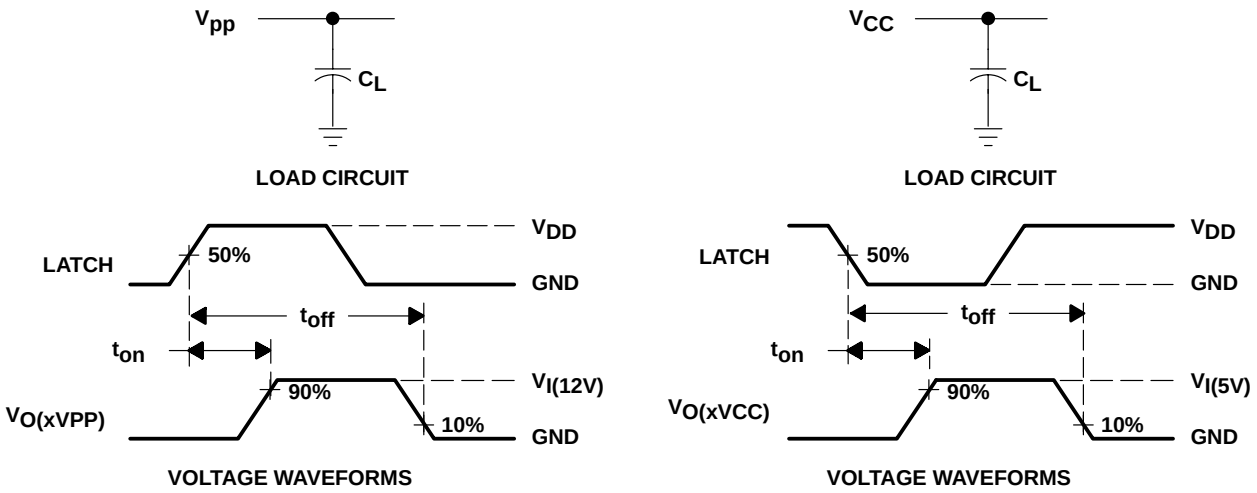
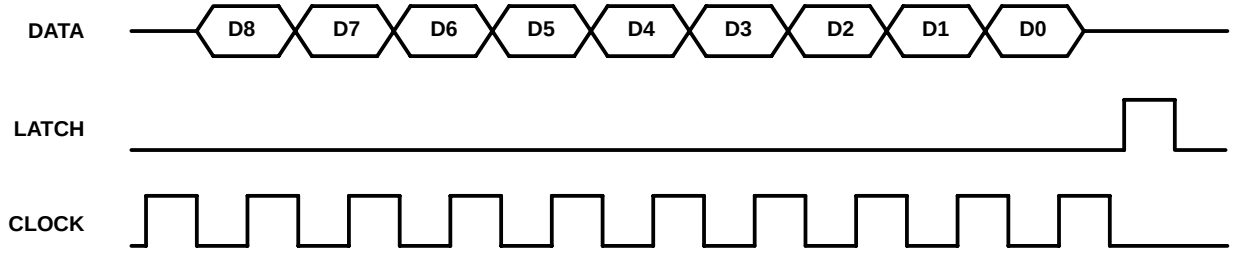



**Figure 1. Test Circuits and Voltage Waveforms**

### Table of Timing Diagrams

| | FIGURE |
|---|---|
| Serial-Interface Timing | 2 |
| xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch | 3 |
| xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch | 4 |
| xVCC Propagation Delay and Rise Time With 100-µF Load, 3.3-V Switch | 5 |
| xVCC Propagation Delay and Fall Time With 100-µF Load, 3.3-V Switch | 6 |
| xVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch | 7 |
| xVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch | 8 |
| xVCC Propagation Delay and Rise Time With 100-µF Load, 5-V Switch | 9 |
| xVCC Propagation Delay and Fall Time With 100-µF Load, 5-V Switch | 10 |
| xVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch | 11 |
| xVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch | 12 |
| xVPP Propagation Delay and Rise Time With 100-µF Load, 12-V Switch | 13 |
| xVPP Propagation Delay and Fall Time With 100-µF Load, 12-V Switch | 14 |




NOTE A: Data is clocked in on the positive leading edge of the clock. The latch should occur before next positive leading edge of the clock. For definition of D0 to D8, see the control logic table.

**Figure 2. Serial-Interface Timing**

## PARAMETER MEASUREMENT INFORMATION

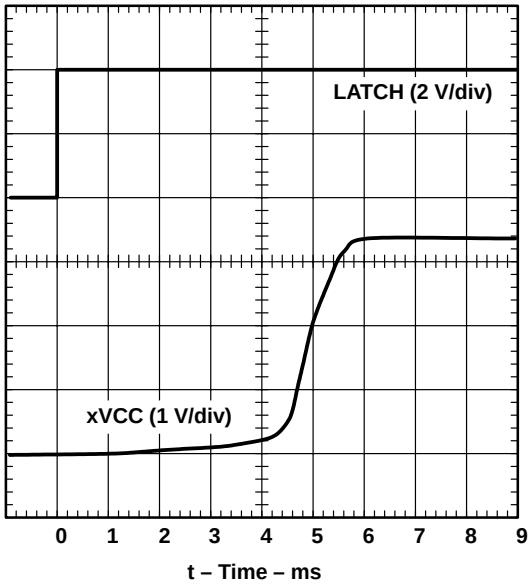



**Figure 3. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch**

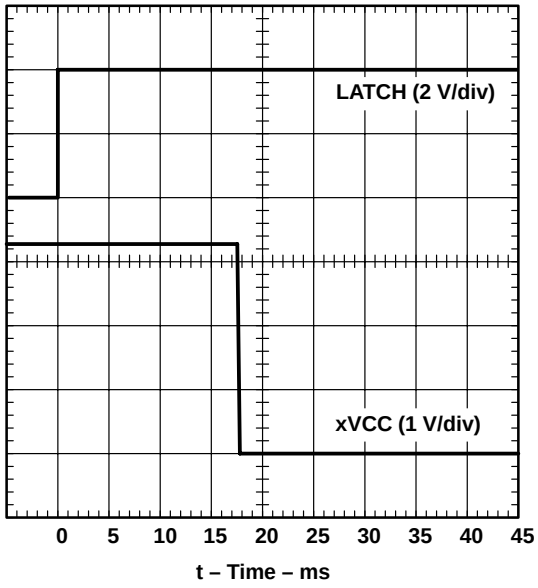



**Figure 4. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch**

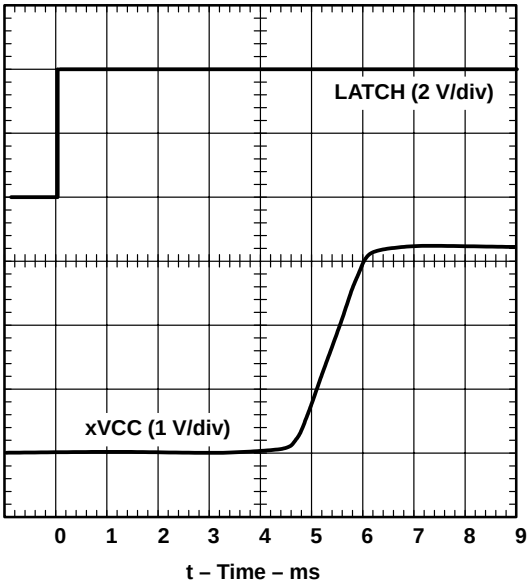



**Figure 5. xVCC Propagation Delay and Rise Time With 100-μF Load, 3.3-V Switch**

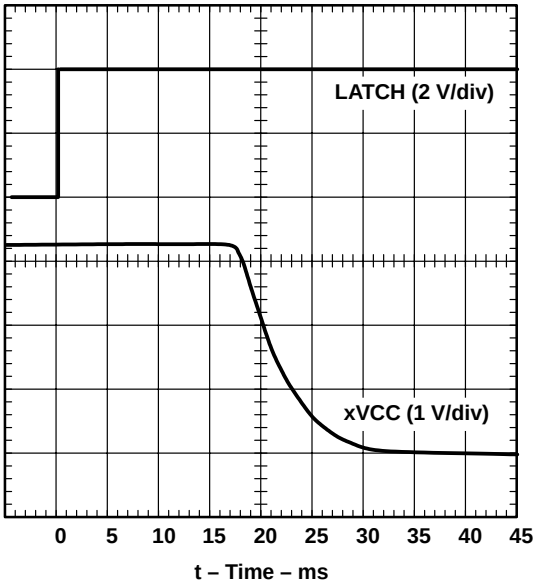



**Figure 6. xVCC Propagation Delay and Fall Time With 100-μF Load, 3.3-V Switch**

## PARAMETER MEASUREMENT INFORMATION

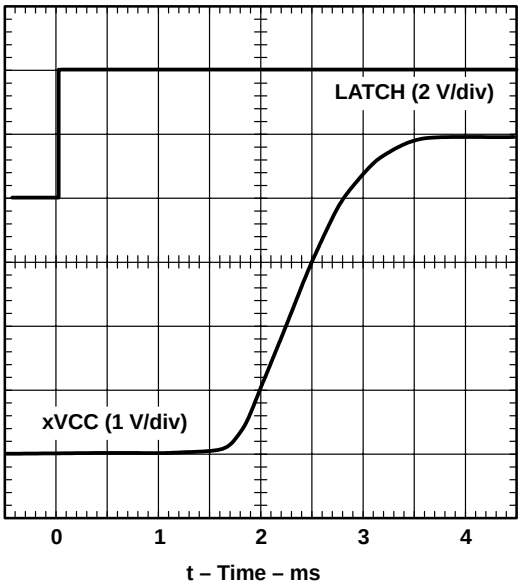



**Figure 7. xVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch**

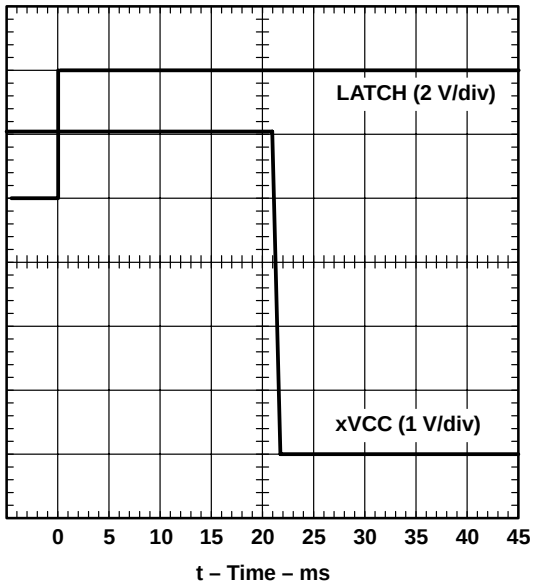



**Figure 8. xVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch**

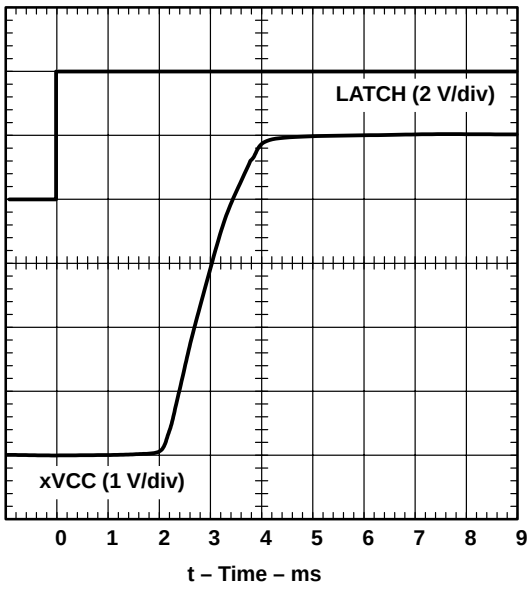



**Figure 9. xVCC Propagation Delay and Rise Time With 100-μF Load, 5-V Switch**

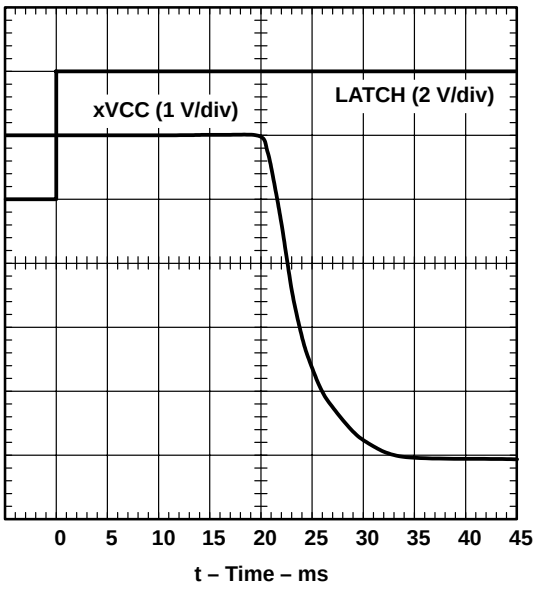



**Figure 10. xVCC Propagation Delay and Fall Time With 100-μF Load, 5-V Switch**

## PARAMETER MEASUREMENT INFORMATION

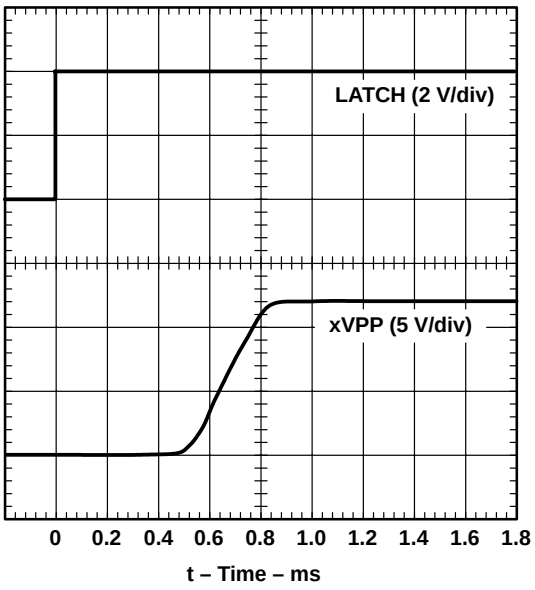



**Figure 11. xVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch**

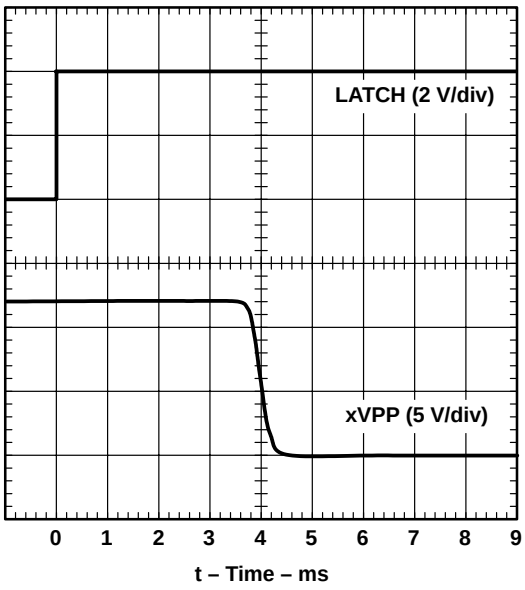



**Figure 12. xVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch**

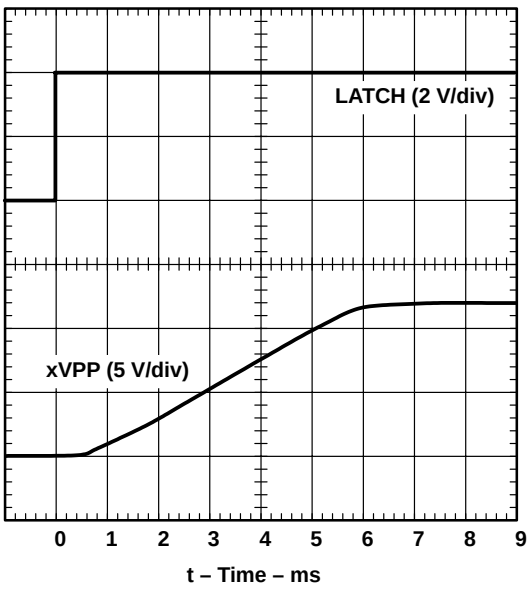



**Figure 13. xVPP Propagation Delay and Rise Time With 100-μF Load, 12-V Switch**

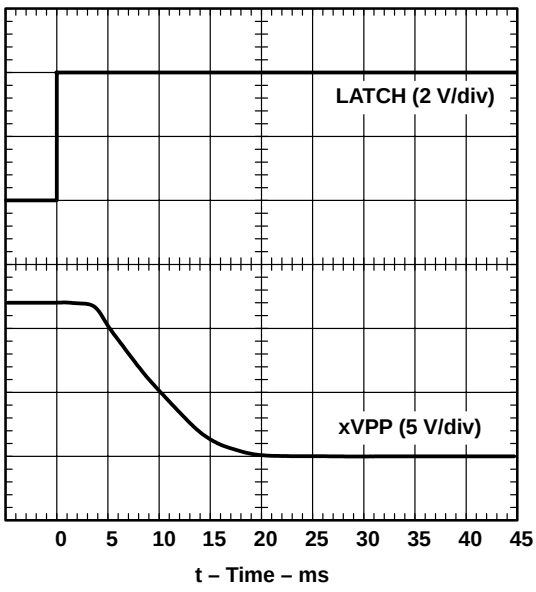



**Figure 14. xVPP Propagation Delay and Fall Time With 100-μF Load, 12-V Switch**

## TYPICAL CHARACTERISTICS†

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $I_{DD}$ | Supply current | vs Junction temperature | 15 |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 3-V switch | vs Junction temperature | 16 |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V switch | vs Junction temperature | 17 |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 12-V switch | vs Junction temperature | 18 |
| $V_{O(xVCC)}$ | Output voltage, 5-V switch | vs Output current | 19 |
| $V_{O(xVCC)}$ | Output voltage, 3.3-V switch | vs Output current | 20 |
| xVPP | Output voltage, $V_{pp}$ switch | vs Output current | 21 |
| $I_{SC(xVCC)}$ | Short-circuit current, 5-V switch | vs Junction temperature | 22 |
| $I_{SC(xVPP)}$ | Short-circuit current, 12-V switch | vs Junction temperature | 23 |

**SUPPLY CURRENT**
**vs**
**JUNCTION TEMPERATURE**

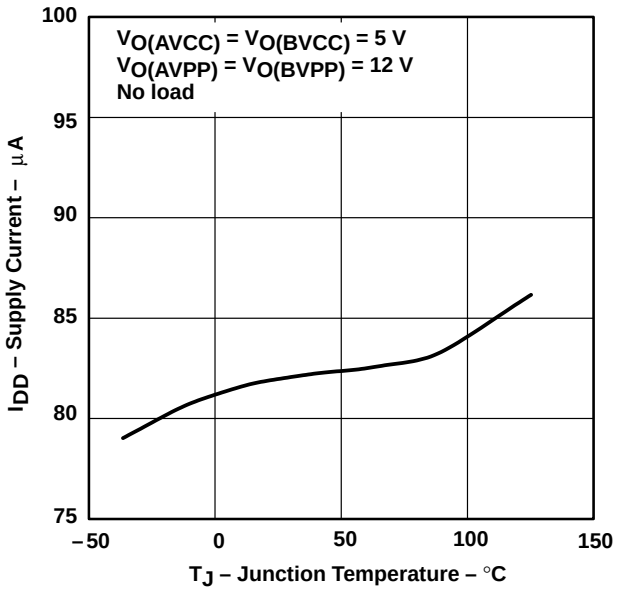



**Figure 15**

† t = pulse tested

## TYPICAL CHARACTERISTICS†

**3.3-V SWITCH**
**STATIC DRAIN-SOURCE ON-STATE RESISTANCE**
**vs**
**JUNCTION TEMPERATURE**

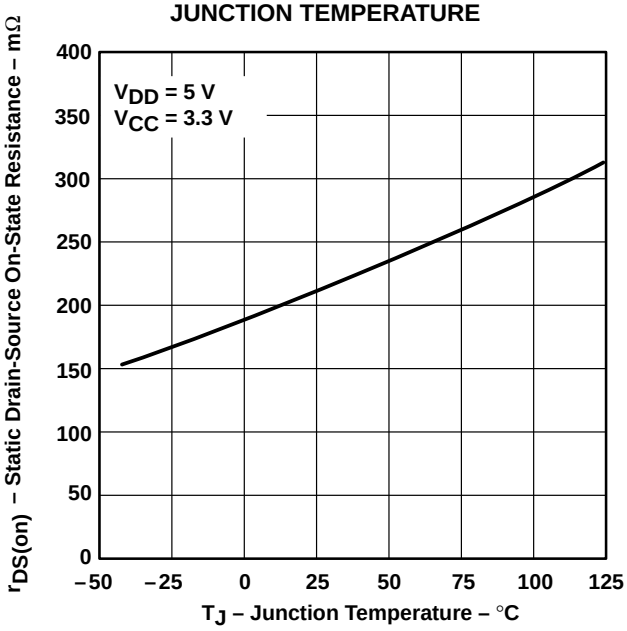



**Figure 16**

**5-V SWITCH**
**STATIC DRAIN-SOURCE ON-STATE RESISTANCE**
**vs**
**JUNCTION TEMPERATURE**

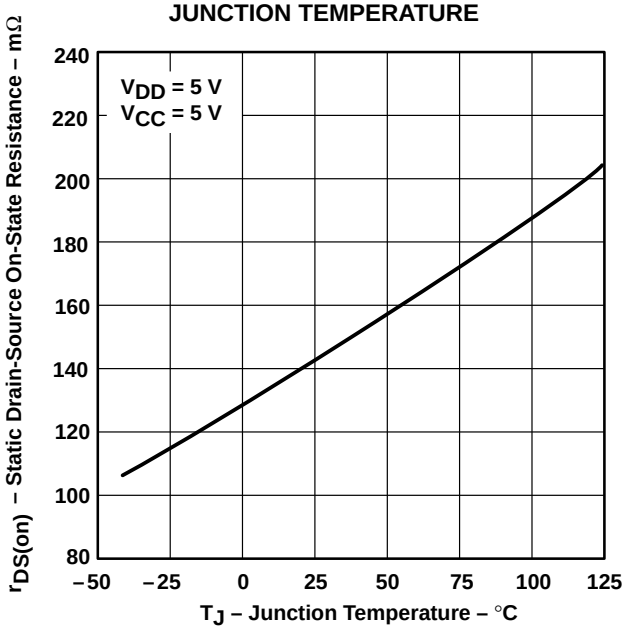



**Figure 17**

**12-V SWITCH**
**STATIC DRAIN-SOURCE ON-STATE RESISTANCE**
**vs**
**JUNCTION TEMPERATURE**

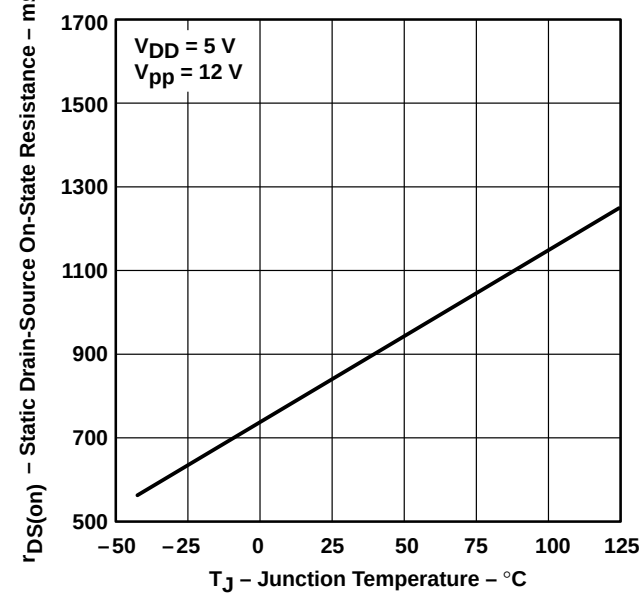



**Figure 18**

**5-V SWITCH**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

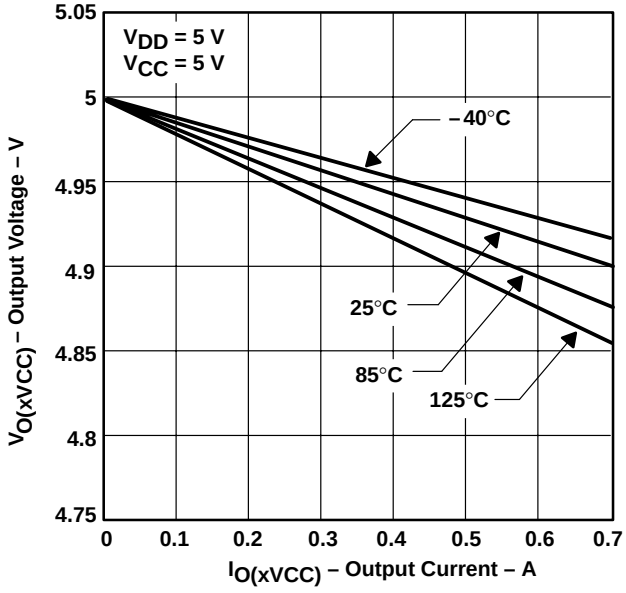



**Figure 19**

† t = pulse tested

## TYPICAL CHARACTERISTICS†

**3-V SWITCH**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

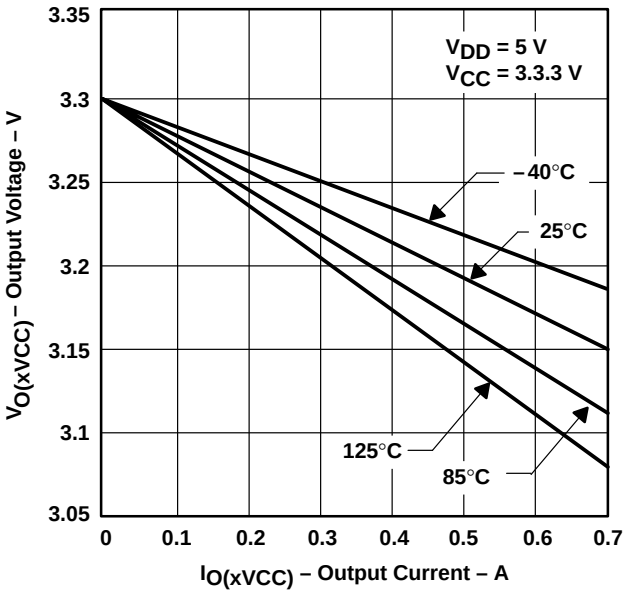



**Figure 20**

**$V_{pp}$ SWITCH**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

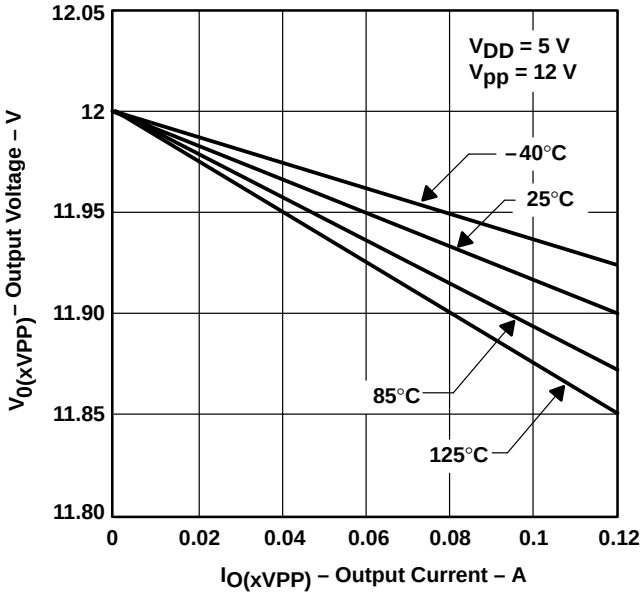



**Figure 21**

**5-V SWITCH**
**SHORT-CIRCUIT CURRENT**
**vs**
**JUNCTION TEMPERATURE**

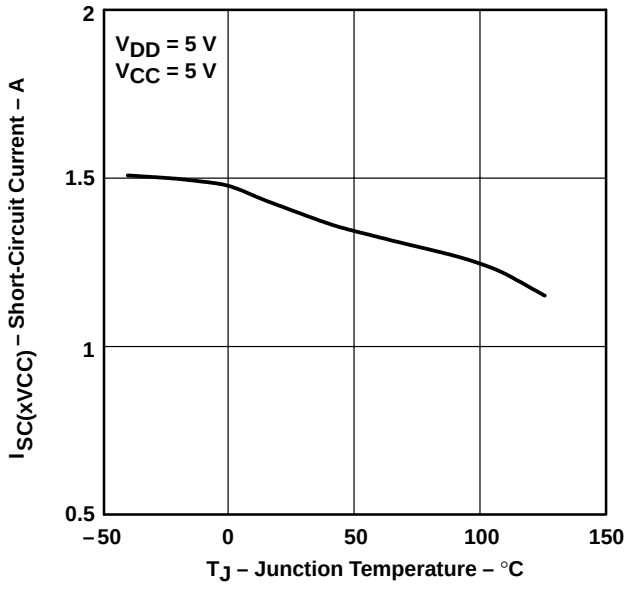



**Figure 22**

**12-V SWITCH**
**SHORT-CIRCUIT CURRENT**
**vs**
**JUNCTION TEMPERATURE**

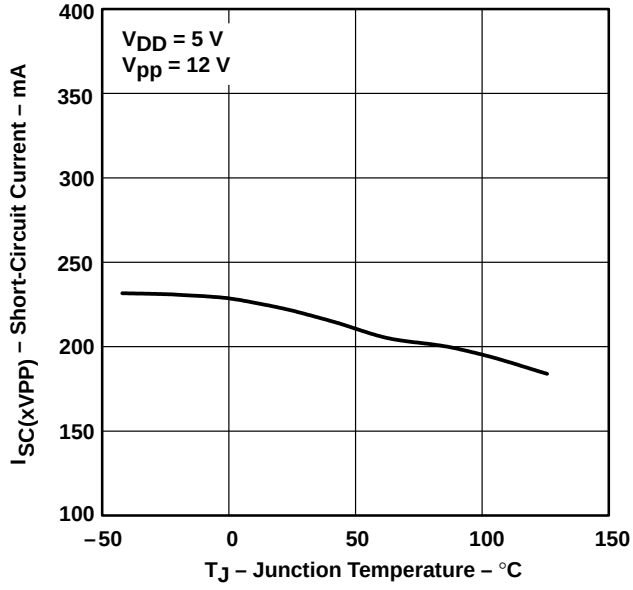



**Figure 23**

† t = pulse tested

## APPLICATION INFORMATION

### overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept. Cards and hosts from different vendors should be compatible and able to communicate with one another transparently.

#### PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the PC Card connector's 68 terminals. This power interface consists of two $V_{CC}$, two $V_{pp}$, and four ground terminals. Multiple $V_{CC}$ and ground terminals minimize connector-terminal and line resistance. The two $V_{pp}$ terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the $V_{CC}$ terminals; flash-memory programming and erase voltage is supplied through the $V_{pp}$ terminals. As each terminal is rated to 0.5 A, $V_{CC}$ and $V_{pp}$ can theoretically supply up to 1 A, assuming equal terminal resistance and no terminal failure. A conservative design would limit current to 500 mA. Some applications, however, require higher $V_{CC}$ currents. Disk drives, for example, may need as much as 750-mA peak current to create the initial torque necessary to spin up the platter. $V_{pp}$ currents, on the other hand, are defined by flash-memory programming requirements, typically under 120 mA.

#### future power trends

The 1-A physical-terminal current alluded to in the PC Card specification has caused some host-system engineers to believe they are required to deliver 1 A within the voltage tolerance of the card. Future applications, such as RF cards, could use the extra power for their radio transmitters. The 5 W required for these cards require very robust power supplies and special cooling considerations. The limited number of host sockets that are able to support cards makes the market for these high-powered PC Cards uncertain. The vast majority of the cards require less than 600 mA continuous current, and the trend is towards even lower powered PC Cards that assure compatibility with a greater number of host systems. Recognizing the need for power derating, an ad hoc committee of the PCMCIA is currently working to limit the amount of steady-state dc current to the PC Card to something less than the currently implied 1 A. When a system is designed to support 1 A, the switch $r_{DS(on)}$, power-supply requirements, and PC Card cooling need to be carefully considered.

#### designing around 1-A delivery

Delivering 1 A means minimizing voltage and power losses across the PC Card power interface, which requires that designers trade off switch resistance and the cost associated with large-die (low $r_{DS(on)}$) MOSFET transistors. The PC Card standard requires that 5 V ±5% or 3.3 V ±0.3 V be supplied to the card. The approximate 10% tolerance for the 3.3-V supply makes the 3.3-V $r_{DS(on)}$ less critical than the 5-V switch. A conservative approach is to allow 2% for voltage-regulator tolerance and 1% for etch- and pin-resistance drops, which leaves 2% (100 mV) for voltage drop at the 5-V switch and at least 6% (198 mV) for the 3.3-V switch.

## APPLICATION INFORMATION

### designing around 1-A delivery (continued)

Calculating the $r_{DS(on)}$ necessary to support a 100 mV or 198 mV switch loss, using R = E/I and setting I = 1 A, the 5-V and 3.3-V switches would need to be 100 mΩ and 198 mΩ respectively. One solution would be to pay for a more expensive switch with lower $r_{DS(on)}$. A second, less expensive approach is to increase the headroom of the power supply—for example, to increase the 5 V supply 1.5% or to 5.075 ±2%. Working through the numbers once more, the 2% for the regulator plus 1 % for etch and terminal losses leaves 97% or 4.923 V. The allowable voltage loss across the power distribution switch is now 4.923 V minus 4.750 V or 173 mV. Therefore, a switch with 173 mΩ or less could deliver 1 A or greater. Setting the power supply high is a common practice for delivering voltages to allow for system switch connector and etch losses. This practice has a minimal effect on overall battery life. In the example above, setting the power supply 1.5% high would only decrease a 3-hour battery life by approximately 2.7 minutes, trivial when compared with the decrease in battery life when running a 5-W PC Card.

### heat dissipation

A greater concern in delivering 1 A or 5 W is the ability of the host to dissipate the heat generated by the PC Card. For desktop computers the solution is simpler: locate the PC Card cage such that it receives convection cooling from the forced air of the fan. Notebooks and other handheld equipment will not be able to rely on convection, but on conduction of heat away from the PC Card through the rails into the card cage. This is difficult because PC Card/card cage heat transfer is very poor. A typical design scenario would require the PC Card to be held at 60°C maximum with the host platform operating as high as 50°C. Preliminary testing reveals that a PC Card can have a 20°C rise, exceeding the 10°C differential in the example, when dissipating less than 2 W of continuous power. Sixty degrees centigrade was chosen because it is the maximum operating temperature allowable by PC Card specification. Power handling requirements and temperature rises are topics of concern and are currently being addressed by the PCMCIA committee.

### overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor though, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2202AI takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an added advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2202AI asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

## APPLICATION INFORMATION

### 12-V supply not required

Most PC Card switches use the externally supplied 12-V $V_{pp}$ power for switch-gate drive and other chip functions, which requires that power be present at all times. The TPS2202AI offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V $V_{DD}$ supply; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V inputs when 12-V supply is not in use. Additional power savings are realized by the TPS2202AI during a software shutdown in which quiescent current drops to a maximum of 1 μA.

### voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2202AI is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2202AI offers a selectable $V_{CC}$ and $V_{pp}$ ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between $V_{CC}$ voltages.

### output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of $V_{CC}$ within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100-kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis will reveal that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2202AI is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial controller interface. The TPS2202AI offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

## power-supply considerations

The TPS2202AI has multiple pins for each of its 3.3-V, 5-V, and 12-V power inputs and for the switched $V_{CC}$ outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12-V inputs must be connected for proper $V_{pp}$ switching; it is recommended that all input and output power pins be paralleled for optimum operation. The $V_{DD}$ input lead must be connected to the 5-V input leads.

Although the TPS2202AI is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-μF electrolytic or tantalum capacitor paralleled by a 0.047-μF to 0.1-μF ceramic capacitor. It is strongly recommended that the switched $V_{CC}$ and $V_{pp}$ outputs be bypassed with a 0.1-μF or larger capacitor; doing so improves the immunity of the TPS2202AI to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2202AI and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance.

## APPLICATION INFORMATION

### power-supply considerations (continued)

The TPS2202AI, unlike other PC Card power-interface switches, does not use the 12-V power supply for switching or other chip functions. Instead, an internal charge pump generates the necessary voltage from $V_{DD}$, allowing the 12-V input supply to be shut down except when the $V_{pp}$ programming or erase voltage is needed. Careful system design using this feature reduces power consumption and extends battery lifetime.

The 3.3-V power input should not be taken higher than the 5-V input. Though doing so is nondestructive, this results in high current flow into the device and could result in abnormal operation. In any case, this occurrence indicates a malfunction of one input voltage or both, which should be investigated.

Similarly, no pin should be taken below –0.3 V; forward biasing the parasitic-substrate diode results in substrate currents and unpredictable performance.

### RESET or $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying a low impedance to the $V_{CC}$ and $V_{pp}$ terminals. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The RESET or $\overline{\text{RESET}}$ input will close internal switches S1, S4, S7, and S10 with all other switches left open (see TPS2202AI control-logic table). The TPS2202AI remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. RESET or $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The unused pin is internally pulled up or down and should be left unconnected.

### overcurrent and thermal protection

The TPS2202AI uses sense FETs to check for overcurrent conditions in each of the $V_{CC}$ and $V_{pp}$ outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{\text{OC}}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2202AI controls the rise time of the $V_{CC}$ and $V_{pp}$ outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2202AI engages. If the $V_{CC}$ or $V_{pp}$ outputs are driven below ground, the TPS2202AI may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the $V_{CC}$ outputs is designed to activate, if powered up, into a short in the range of 0.75 A to 1.9 A, typically at about 1.3 A. The $V_{pp}$ outputs limit from 120 mA to 400 mA, typically around 200 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

## APPLICATION INFORMATION

### calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, $T_J$, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate $T_J$, first find $r_{DS(on)}$ from Figures 16, 17, and 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma\ P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

### logic input and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 9-bit (D0 through D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The shutdown bit of the data word places all $V_{CC}$ and $V_{pp}$ outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

The TPS2202AI serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent condition in any of the $V_{CC}$ or $V_{pp}$ outputs as previously discussed.

## APPLICATION INFORMATION

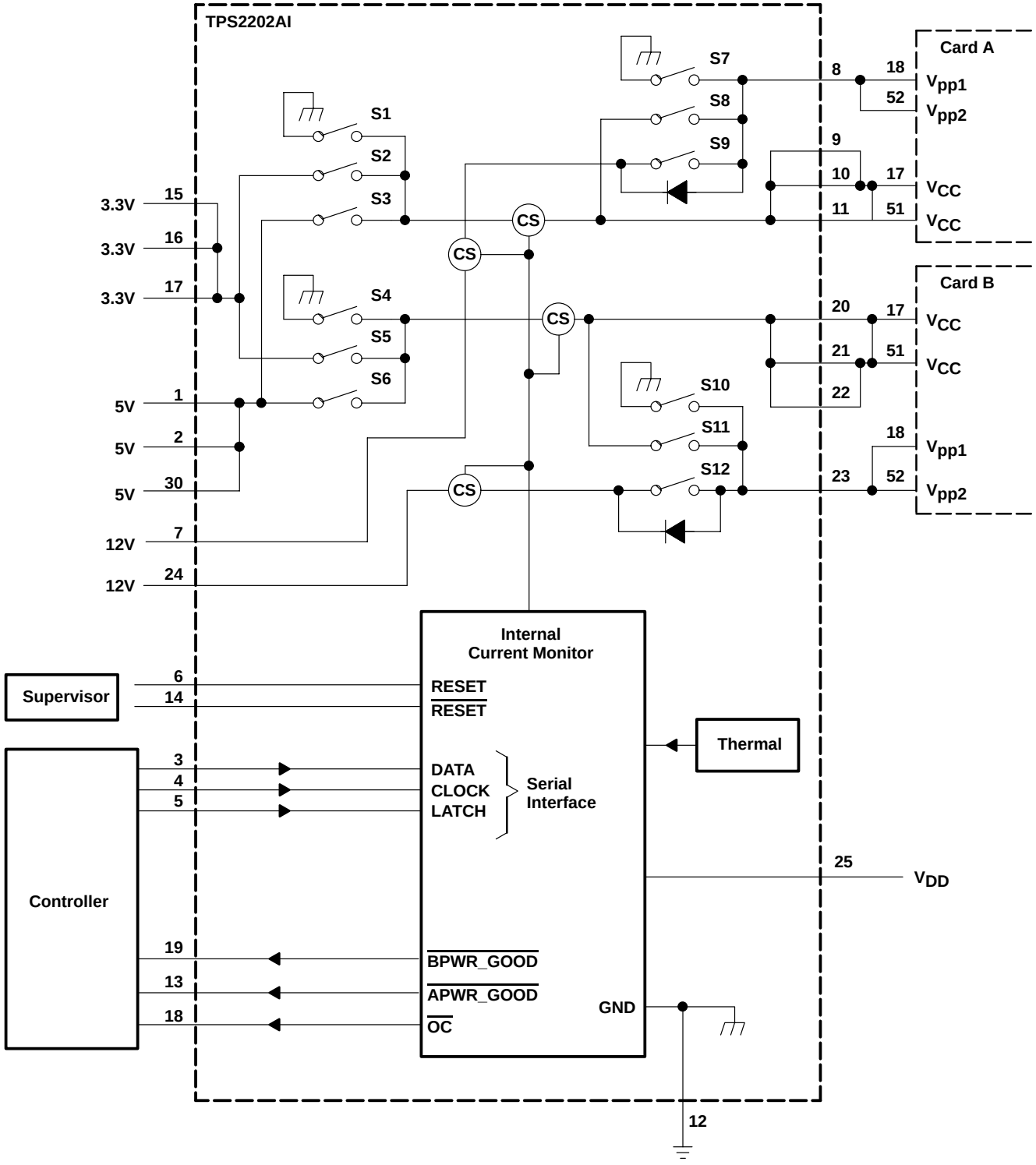



**Figure 24. Internal Switching Matrix**

## APPLICATION INFORMATION

### TPS2202AI control logic

#### AVPP

| CONTROL SIGNALS | | | INTERNAL SWITCH SETTINGS | | | OUTPUT |
|---|---|---|---|---|---|---|
| D8 $\overline{\text{SHDN}}$ | D0 A_VPP_PGM | D1 A_VPP_VCC | S7 | S8 | S9 | VAVPP |
| 1 | 0 | 0 | CLOSED | OPEN | OPEN | 0 V |
| 1 | 0 | 1 | OPEN | CLOSED | OPEN | VCC† |
| 1 | 1 | 0 | OPEN | OPEN | CLOSED | VPP(12 V) |
| 1 | 1 | 1 | OPEN | OPEN | OPEN | Hi-Z |
| 0 | X | X | OPEN | OPEN | OPEN | Hi-Z |

#### BVPP

| CONTROL SIGNALS | | | INTERNAL SWITCH SETTINGS | | | OUTPUT |
|---|---|---|---|---|---|---|
| D8 $\overline{\text{SHDN}}$ | D4 B_VPP_PGM | D5 B_VPP_VCC | S10 | S11 | S12 | VBVPP |
| 1 | 0 | 0 | CLOSED | OPEN | OPEN | 0 V |
| 1 | 0 | 1 | OPEN | CLOSED | OPEN | VCC‡ |
| 1 | 1 | 0 | OPEN | OPEN | CLOSED | VPP(12 V) |
| 1 | 1 | 1 | OPEN | OPEN | OPEN | Hi-Z |
| 0 | X | X | OPEN | OPEN | OPEN | Hi-Z |

#### AVCC

| CONTROL SIGNALS | | | INTERNAL SWITCH SETTINGS | | | OUTPUT |
|---|---|---|---|---|---|---|
| D8 $\overline{\text{SHDN}}$ | D3 $\overline{\text{A\_VCC3}}$ | D2 $\overline{\text{A\_VCC5}}$ | S1 | S2 | S3 | VAVCC |
| 1 | 0 | 0 | CLOSED | OPEN | OPEN | 0 V |
| 1 | 0 | 1 | OPEN | CLOSED | OPEN | 3.3 V |
| 1 | 1 | 0 | OPEN | OPEN | CLOSED | 5 V |
| 1 | 1 | 1 | CLOSED | OPEN | OPEN | 0 V |
| 0 | X | X | OPEN | OPEN | OPEN | Hi-Z |

#### BVCC

| CONTROL SIGNALS | | | INTERNAL SWITCH SETTINGS | | | OUTPUT |
|---|---|---|---|---|---|---|
| D8 $\overline{\text{SHDN}}$ | D6 $\overline{\text{B\_VCC3}}$ | D7 $\overline{\text{B\_VCC5}}$ | S4 | S5 | S6 | VBVCC |
| 1 | 0 | 0 | CLOSED | OPEN | OPEN | 0 V |
| 1 | 0 | 1 | OPEN | CLOSED | OPEN | 3.3 V |
| 1 | 1 | 0 | OPEN | OPEN | CLOSED | 5 V |
| 1 | 1 | 1 | CLOSED | OPEN | OPEN | 0 V |
| 0 | X | X | OPEN | OPEN | OPEN | Hi-Z |

† Output depends on AVCC
‡ Output depends on BVCC

### ESD protection

All TPS2202AI inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The $V_{CC}$ and $V_{pp}$ outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

## APPLICATION INFORMATION

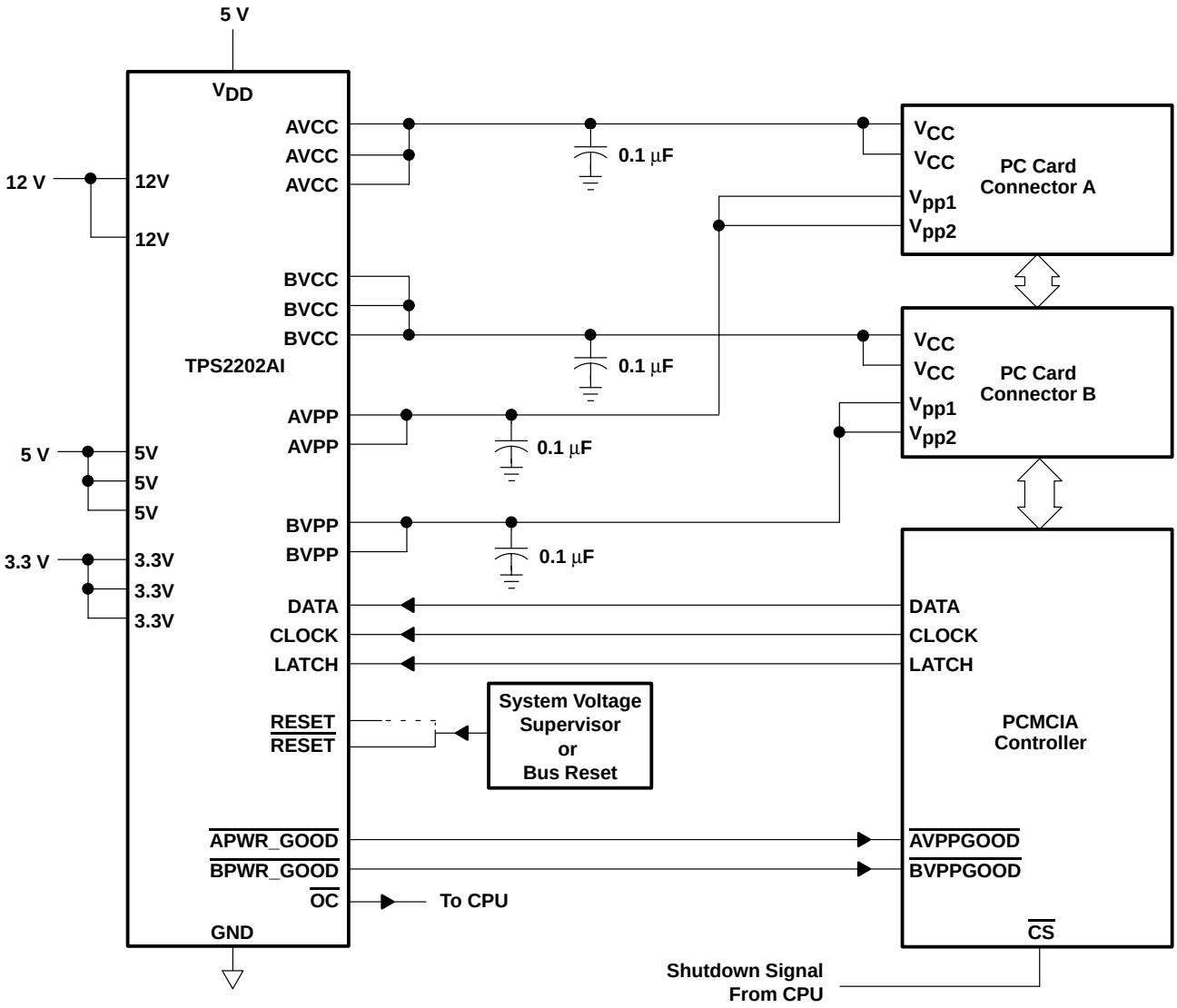



**Figure 25. Detailed Interconnections and Capacitor Recommendations**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2202AIDB | LIFEBUY | SSOP | DB | 30 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPS2202AI | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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