



PC CARD™ POWER-INTERFACE SWITCH WITH RESET FOR SERIAL PCMCIA CONTROLLER

FEATURES

- Fully Integrated V_{CC} and V_{PP} Switching for Single-Slot or Dual-Slot PC Card™ Interface
- P²C™ 3-Lead Serial Interface Compatible With CardBus™ Controller
- Meets PC Card Standard
- RESET for System Initialization of PC Cards
- 12-V Supplies Can Be Disabled Except During 12-V Flash Programming
- Short-Circuit and Thermal Protection
- 24-Pin HTSSOP (PWP), 30-Pin SSOP (DB), and 32-Pin TSSOP (DAP) Packages
- Compatible With 3.3-V, 5-V, and 12-V PC Cards
- Low $r_{DS(on)}$ (95-m Ω , 5-V V_{CC} Switch; 85-m Ω 3.3-V V_{CC} Switch)
- Single-Slot Switch: TPS2210A
Dual-Slot Switch: TPS2204A and TPS2206A
- Break-Before-Make Switching

APPLICATIONS

- Notebook and Desktop Computers
- Set-Top Boxes
- Personal Digital Assistants(PDAs)
- Digital Cameras
- Bar Code Scanners

DESCRIPTION

The TPS2204A and TPS2206A PC CardBus™ power-interface switches provide an integrated power-management solution for two PC Card™ sockets. The TPS2210A is a single-slot option for this family of devices. These devices allow the controlled distribution of 3.3 V, 5 V, and 12 V to each card slot. The current-limiting and thermal-protection features eliminate the need for fuses. Current-limit reporting helps the user isolate a system fault. The switch $r_{DS(on)}$ and current-limit values are set for the peak and average current requirements stated in the PC Card™ specification, and are optimized for cost.

The TPS2206A is pin and/or functionally compatible with the TPS2206, TPS2216, TPS2216A, TPS2226, TPS2226A, and TPS2228 with a few exceptions, as shown in the Available Options table.

AVAILABLE OPTIONS OF THE TPS2206A PIN COMPATIBLE SWITCHES

PART NUMBER	INDEPENDENT V_{PP} SWITCHING	PIN VARIATION					INPUT VOLTAGES
		RESET	RESET	SHDN	MODE	STBY	
TPS2206	No	Yes	Yes	No	No	No	3.3 V, 5 V, 12 V
TPS2206A	No	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2216	Yes/No ⁽¹⁾	Yes	Yes	No	Yes	Yes	3.3 V, 5 V, 12 V
TPS2216A	Yes/No ⁽¹⁾	Yes	Yes	No	Yes	Yes	3.3 V, 5 V, 12 V
TPS2226	Yes	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2226A	Yes	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2228	Yes	Yes	No	Yes	No	No	1.8 V, 3.3 V, 5 V

⁽¹⁾ Selected by MODE pin.



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PC Card and CardBus are trademarks of PCMCIA (Personal Computer Memory Card International Association).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGED DEVICES		
	PLASTIC SMALL OUTLINE (DB)	POWERPAD™ PLASTIC SMALL OUTLINE (DAP-32)	POWERPAD™ PLASTIC SMALL OUTLINE (PWP-24)
-40°C to 85°C	TPS2206ADB	TPS2206ADAP	TPS2204APWP TPS2210APWP

(1) The DB, PWP, and DAP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2206ADBR) for taped and reeled.

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DB (30)	821.46 mW	10.95 mW/°C	328.58 mW	164.29 mW
DAP (32)	3191.4 mW	42.55 mW/°C	1276.5 mW	638.29 mW
PWP (24)	2491.6 mW	33.22 mW/°C	996.67 mW	498.33 mW

(1) These devices are mounted on an JEDEC low-k board (2-oz. traces on surface).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		UNITS
Input voltage range for card power	V _I (3.3V)	-0.3 V to 5.5 V
	V _I (5V)	-0.3 V to 5.5 V
	V _I (12V)	-0.3 V to 14 V
Logic input/output voltage		-0.3 V to 6 V
Output voltage	V _O (xVCC)	-0.3 V to 6 V
	V _O (xVPP)	-0.3 V to 14 V
Continuous total power dissipation		See Dissipation Rating Table
Output current	I _O (xVCC)	Internally Limited
	I _O (xVPP)	Internally Limited
Operating virtual junction temperature range, T _J		-40°C to 100 °C
Storage temperature range, T _{STG}		-55°C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260 °C
\overline{OC} sink current		10 mA

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage, $V_I(3.3V)$ is required for all circuit operations. 5 V and 12 V are only required for their respective functions.	$V_I(3.3V)(1)$	3	3.6	V
	$V_I(5V)$	3	5.5	
	$V_I(12V)$	7	13.5	
Output current, I_O	$I_O(xVCC)$ at $T_J = 100^\circ C$		1	A
	$I_O(xVPP)$ at $T_J = 100^\circ C$		100	mA
Clock frequency, $f_{(clock)}$			2.5	MHz
Pulse duration, t_w	Data		200	ns
	Latch		250	
	Clock		100	
	Reset		100	
Data-to-clock hold time, t_H (see Figure 2)			100	ns
Data-to-clock setup time, t_{SU} (see Figure 2)			100	ns
Latch delay time, $t_{d(latch)}$ (see Figure 2)			100	ns
Clock delay time, $t_{d(clock)}$ (see Figure 2)			250	ns
Operating virtual junction temperature, T_J (maximum to be calculated at worst case P_D at $85^\circ C$ ambient)		-40	100	$^\circ C$

(1) It is understood that for $V_I(3.3V) < 3V$, voltages within the absolute maximum ratings applied to pin 5 V or pin 12 V will not damage the IC.

ELECTRICAL CHARACTERISTICS

$T_J = 25^\circ C$, $V_I(5V) = 5V$, $V_I(3.3V) = 3.3V$, $V_I(12V) = 12V$, all outputs unloaded (unless otherwise noted)

POWER SWITCH							
PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	3.3V to $xVCC$ (2)	$I_O = 750$ mA each		85	110	m Ω
			$I_O = 750$ mA each, $T_J = 100^\circ C$		110	140	
	5V to $xVCC$ (2)	$I_O = 500$ mA each		95	130	Ω	
		$I_O = 500$ mA each, $T_J = 100^\circ C$		120	160		
	3.3V or 5V to $xVPP$ (2)	$I_O = 50$ mA each		0.8	1	Ω	
		$I_O = 50$ mA each, $T_J = 100^\circ C$		1	1.3		
12V to $xVPP$ (2)	$I_O = 50$ mA each		2	2.5	Ω		
	$I_O = 50$ mA each, $T_J = 100^\circ C$		2.5	3.4			
Output discharge resistance	Discharge at $xVCC$	$I_O(disc) = 1$ mA		0.5	0.7	1	k Ω
	Discharge at $xVPP$	$I_O(disc) = 1$ mA		0.2	0.4	0.5	
I_{OS}	Short-circuit output current	Limit (steady-state value), output powered into a short circuit	$I_{OS}(xVCC)$	1	1.4	2	A
			$I_{OS}(xVPP)$	120	200	300	mA
		Limit (steady-state value), output powered into a short circuit, $T_J = 100^\circ C$	$I_{OS}(xVCC)$	1	1.4	2	A
			$I_{OS}(xVPP)$	120	200	300	mA
Thermal shutdown temperature(2)	Thermal trip point, T_J	Rising temperature		135			$^\circ C$
	Hysteresis, T_J			10			
Current-limit response time (3)(4)		5V to $xVCC = 5V$, with 100-m Ω short to GND		10			μs
		5V to $xVPP = 5V$, with 100-m Ω short to GND		3			

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

(2) TPS2204A and TPS2206A: two switches on. TPS2210A: one switch on.

(3) Specified by design; not tested in production.

(4) From application of short to 110% of final current limit.

ELECTRICAL CHARACTERISTICS Continued

$T_J = 25^\circ\text{C}$, $V_{I(5V)} = 5\text{ V}$, $V_{I(3.3V)} = 3.3\text{ V}$, $V_{I(12V)} = 12\text{ V}$, all outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Normal operation	$I_{I(3.3V)}$	$V_O(xVCC) = V_O(xVPP) = 3.3\text{ V}$ and also for $\overline{\text{RESET}} = 0\text{ V}$		140	200	μA
		$I_{I(5V)}$			8	12	
		$I_{I(12V)}$			100	180	
	Shutdown mode	$I_{I(3.3V)}$	$V_O(xVCC) = V_O(xVPP) = \text{Hi-Z}$		0.3	2	
		$I_{I(5V)}$			0.1	2	
		$I_{I(12V)}$			0.3	2	
I_{lkg}	Shutdown mode	$V_O(xVCC) = 5\text{ V}$, $V_{I(5V)} = V_{I(12V)} = 0\text{ V}$	$T_J = 100^\circ\text{C}$			10	μA
						50	
		$V_O(xVPP) = 12\text{ V}$, $V_{I(5V)} = V_{I(12V)} = 0\text{ V}$	$T_J = 100^\circ\text{C}$			10	
						50	

LOGIC SECTION (CLOCK, DATA, LATCH, $\overline{\text{RESET}}$, $\overline{\text{SHDN}}$, $\overline{\text{OC}}$)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
I_I	$I_{I(\overline{\text{RESET}})}^{(1)}$	$\overline{\text{RESET}} = 5.5\text{ V}$		-1		1	μA	
		$\overline{\text{RESET}} = 0\text{ V}$		-30	-20	-10		
	$I_{I(\overline{\text{SHDN}})}^{(1)}$	$\overline{\text{SHDN}} = 5.5\text{ V}$		-1		1		
		$\overline{\text{SHDN}} = 0\text{ V}$		-50		-3		
	$I_{I(\text{LATCH})}^{(1)}$	$\text{LATCH} = 5.5\text{ V}$						50
		$\text{LATCH} = 0\text{ V}$		-1				1
$I_{I(\text{CLOCK, DATA})}$	$0\text{ V to } 5.5\text{ V}$		-1			1		
V_{IH}	High-level input voltage, logic			2			V	
V_{IL}	Low-level input voltage, logic					0.8	V	
$V_{O(\text{sat})}$	Output saturation voltage at $\overline{\text{OC}}$	$I_O = 2\text{ mA}$			0.14	0.4	V	
I_{lkg}	Leakage current at $\overline{\text{OC}}$	$V_{O(\overline{\text{OC}})} = 5.5\text{ V}$			0	1	μA	

(1) LATCH has low current pulldown. $\overline{\text{RESET}}$ and $\overline{\text{SHDN}}$ have low-current pullup.

UVLO AND POR (POWER-ON RESET)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(3.3V)}$	Input voltage at 3.3V pin, UVLO	3.3-V level below which all switches are Hi-Z		2.4	2.7	2.9	V
$V_{hys(3.3V)}$	UVLO hysteresis voltage at V_A (1)				100		mV
$V_{I(5V)}$	Input voltage at 5V pin, UVLO	5-V level below which only 5V switches are Hi-Z		2.3	2.5	2.9	V
$V_{hys(5V)}$	UVLO hysteresis voltage at 5 V(1)				100		mV
t_{df}	Delay time for falling response, UVLO(1)	Delay from voltage hit (step from 3 V to 2.3 V) to Hi-Z control (90% V_G to GND)			4		μs
$V_{I(\text{POR})}$	Input voltage, power-on reset(1)	3.3-V voltage below which POR is asserted causing a $\overline{\text{RESET}}$ internally with all line switches open and all discharge switches closed.				1.7	V

(1) Specified by design; not tested in production.

SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{I(3.3V)} = 3.3\text{ V}$, $V_{I(5V)} = 5\text{ V}$, $V_{I(12)} = 12\text{ V}$ (not applicable for TPS2223A) all outputs unloaded (unless otherwise noted)

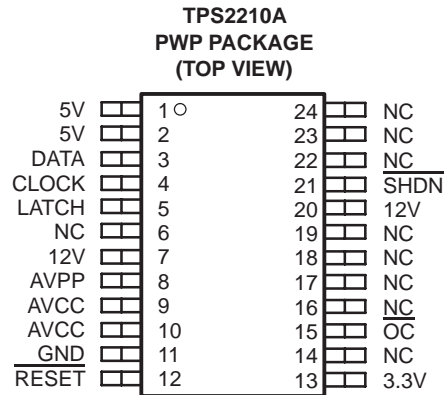
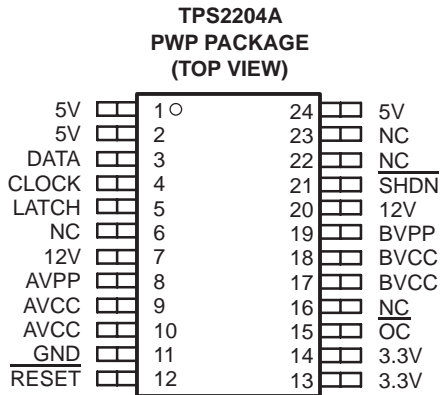
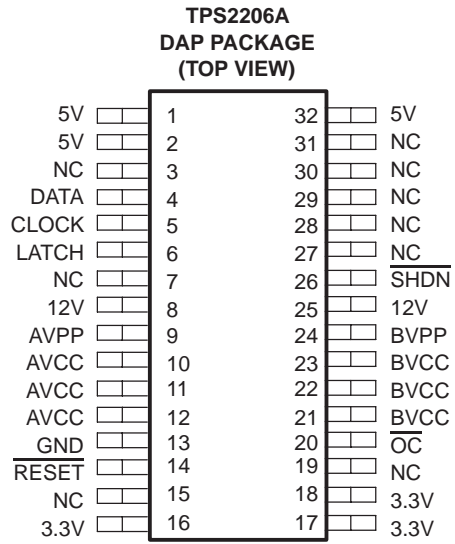
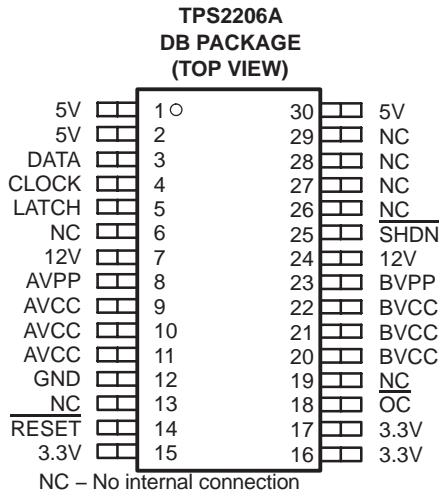
PARAMETER(1)	LOAD CONDITION	TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT	
t_r Output rise times(3)	$C_L(xVCC) = 0.1\ \mu\text{F}$, $C_L(xVPP) = 0.1\ \mu\text{F}$, $I_{O(xVCC)} = 0\ \text{A}$, $I_{O(xVPP)} = 0\ \text{A}$	$V_{O(xVCC)} = 5\ \text{V}$		0.9		ms	
		$V_{O(xVPP)} = 12\ \text{V}$		0.26			
	$C_L(xVCC) = 150\ \mu\text{F}$, $C_L(xVPP) = 10\ \mu\text{F}$, $I_{O(xVCC)} = 0.75\ \text{A}$, $I_{O(xVPP)} = 50\ \text{mA}$	$V_{O(xVCC)} = 5\ \text{V}$		1.1			
		$V_{O(xVPP)} = 12\ \text{V}$		0.6			
t_f Output fall times(3)	$C_L(xVCC) = 0.1\ \mu\text{F}$, $C_L(xVPP) = 0.1\ \mu\text{F}$, $I_{O(xVCC)} = 0\ \text{A}$, $I_{O(xVPP)} = 0\ \text{A}$	$V_{O(xVCC)} = 5\ \text{V}$, Discharge switches ON		0.5		ms	
		$V_{O(xVPP)} = 12\ \text{V}$, Discharge switches ON		0.2			
	$C_L(xVCC) = 150\ \mu\text{F}$, $C_L(xVPP) = 10\ \mu\text{F}$, $I_{O(xVCC)} = 0.75\ \text{A}$, $I_{O(xVPP)} = 50\ \text{mA}$	$V_{O(xVCC)} = 5\ \text{V}$		2.35			
		$V_{O(xVPP)} = 12\ \text{V}$		3.9			
t_{pd} Propagation delay times(3)	$C_L(xVCC) = 0.1\ \mu\text{F}$, $C_L(xVPP) = 0.1\ \mu\text{F}$, $I_{O(xVCC)} = 0\ \text{A}$, $I_{O(xVPP)} = 0\ \text{A}$	Latch \uparrow to xVPP (12 V)	t_{pdon}		2	ms	
			t_{pdoff}		0.62		
		Latch \uparrow to xVPP (5 V)	t_{pdon}		0.77		
			t_{pdoff}		0.51		
		Latch \uparrow to xVPP (3.3 V)	t_{pdon}		0.75		
			t_{pdoff}		0.52		
	Latch \uparrow to xVCC (5 V)	t_{pdon}		0.3			
		t_{pdoff}		2.5			
	Latch \uparrow to xVCC (3.3V)	t_{pdon}		0.3			
		t_{pdoff}		2.8			
	$C_L(xVCC) = 150\ \mu\text{F}$, $C_L(xVPP) = 10\ \mu\text{F}$, $I_{O(xVCC)} = 0.75\ \text{A}$, $I_{O(xVPP)} = 50\ \text{mA}$	Latch \uparrow to xVPP (12 V)	t_{pdon}		2.2		ms
			t_{pdoff}		0.8		
Latch \uparrow to xVPP (5 V)		t_{pdon}		0.8			
		t_{pdoff}		0.6			
Latch \uparrow to xVPP (3.3 V)		t_{pdon}		0.8			
		t_{pdoff}		0.6			
Latch \uparrow to xVCC (5 V)	t_{pdon}		0.6				
	t_{pdoff}		2.5				
Latch \uparrow to xVCC (3.3V)	t_{pdon}		0.5				
	t_{pdoff}		2.6				

(1) Refer to Parameter Measurement Information in Figure 1.

(2) No card inserted, assumes a 0.1- μF output capacitor (see Figure 1).

(3) Specified by design; not tested in production.

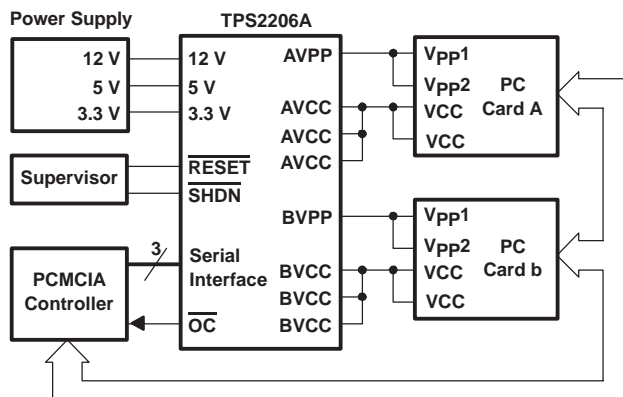
PIN ASSIGNMENTS



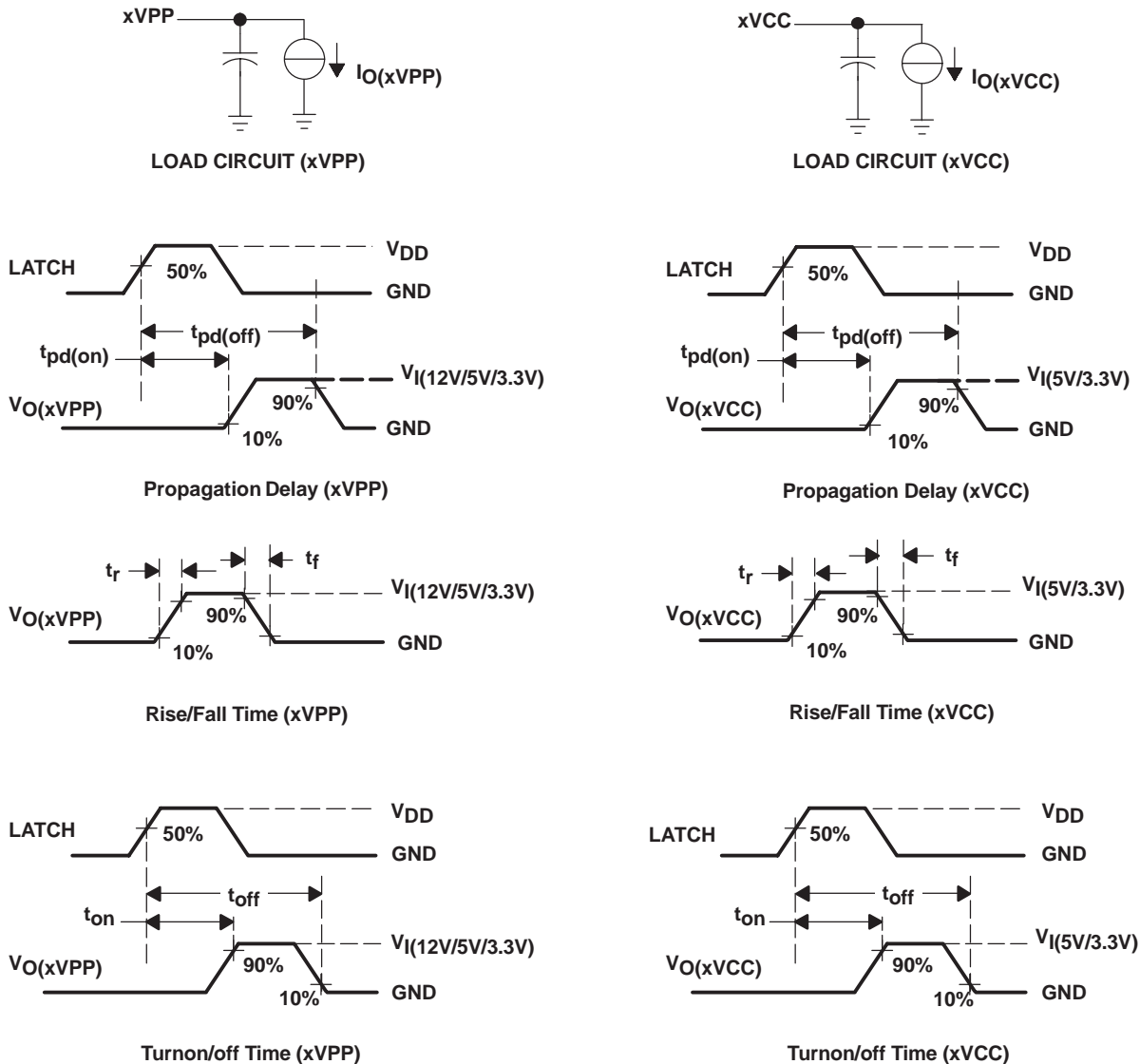
TERMINAL FUNCTIONS

NAME	TERMINAL NUMBER				I/O	DESCRIPTION
	NUMBER					
	TPS2204A	TPS2206A		TPS2210A		
	PWP	DB	DAP	PWP		
3.3V	13, 14	15, 16, 17	16, 17, 18	13	I	3.3-V input for card power and chip power
5V	1, 2, 24	1, 2, 30	1, 2, 32	1, 2	I	5-V V _{CC} input for card power
12V	7, 20	7, 24	8, 25	7, 20	I	12-V V _{PP} input for card power (xV _{PP}). The two 12-V pins must be externally connected.
AVCC	9, 10	9, 10, 11	10, 11, 12	9, 10	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card.
AVPP	8	8	9	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance to card.
BVCC	17, 18	20, 21, 22	21, 22, 23	---	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance.
BVPP	19	23	24	---	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance.
CLOCK	4	4	5	4	I	Logic-level clock for serial data word
DATA	3	3	4	3	I	Logic-level serial data word
GND	11	12	13	11		Ground
LATCH	5	5	6	5	I	Logic-level latch for serial data word, internal pulldown
NC	6, 16, 22, 23	13, 19, 26–29	3, 7, 15, 19, 27–31	6, 14, 16–19, 22–24		No internal connection
$\overline{\text{OC}}$	15	18	20	15	O	Open-drain overcurrent reporting output that goes low when an overcurrent condition exists. An external pullup is required.
$\overline{\text{SHDN}}$	21	25	26	21	I	Hi-Z (open) all switches. Identical function to serial D8. Asynchronous active-low command, internal pullup
$\overline{\text{RESET}}$	12	14	14	12	I	Logic-level RESET input active low. Do not connect if terminal 6 is used.

TYPICAL PC CARD POWER-DISTRIBUTION APPLICATION

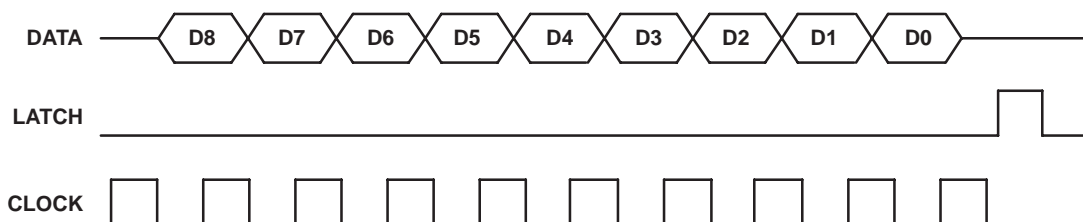


PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

Figure 1. Test Circuits and Voltage Waveforms



NOTE: Data is clocked in on the positive edge of the clock. The latch should occur before the next positive leading edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 2. Serial-Interface Timing for TPS2206A

TABLE OF GRAPHS

		FIGURE
Short-circuit response, short applied to powered-on 5-V xVCC-switch output	vs Time	3
Short-circuit response, short applied to powered-on 12-V xVPP-switch output	vs Time	4
\overline{OC} response with ramped overcurrent-limit load on 5-V xVCC-switch output	vs Time	5
\overline{OC} response with ramped overcurrent-limit load on 12-V xVPP-switch output	vs Time	6
Turnon propagation delay time, xVCC ($C_L = 150 \mu\text{F}$)	vs Junction temperature	7
Turnoff propagation delay time, xVCC ($C_L = 150 \mu\text{F}$)	vs Junction temperature	8
Turnon propagation delay time, xVPP ($C_L = 10 \mu\text{F}$)	vs Junction temperature	9
Turnoff propagation delay time, xVPP ($C_L = 10 \mu\text{F}$)	vs Junction temperature	10
Turnon propagation delay time, xVCC ($T_J = 25^\circ\text{C}$)	vs Load capacitance	11
Turnoff propagation delay time, xVCC ($T_J = 25^\circ\text{C}$)	vs Load capacitance	12
Turnon propagation delay time, xVPP ($T_J = 25^\circ\text{C}$)	vs Load capacitance	13
Turnoff propagation delay time, xVPP ($T_J = 25^\circ\text{C}$)	vs Load capacitance	14
Rise time, xVCC ($C_L = 150 \mu\text{F}$)	vs Junction temperature	15
Fall time, xVCC ($C_L = 150 \mu\text{F}$)	vs Junction temperature	16
Rise time, xVPP ($C_L = 10 \mu\text{F}$)	vs Junction temperature	17
Fall time, xVPP ($C_L = 10 \mu\text{F}$)	vs Junction temperature	18
Rise time, xVCC ($T_J = 25^\circ\text{C}$)	vs Load capacitance	19
Fall time, xVCC ($T_J = 25^\circ\text{C}$)	vs Load capacitance	20
Rise time, xVPP ($T_J = 25^\circ\text{C}$)	vs Load capacitance	21
Fall time, xVPP ($T_J = 25^\circ\text{C}$)	vs Load capacitance	22

SHORT-CIRCUIT RESPONSE,
SHORT APPLIED TO POWERED-ON 5-V
xVCC-SWITCH OUTPUT

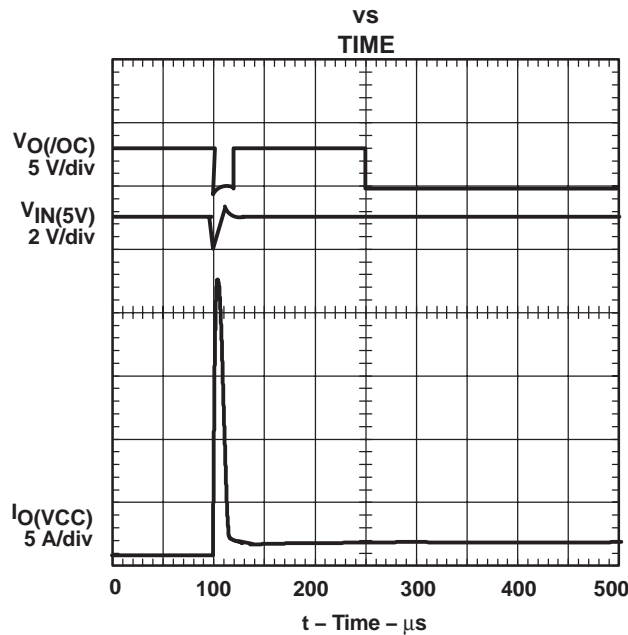


Figure 3

SHORT-CIRCUIT RESPONSE,
SHORT APPLIED TO POWERED-ON 12-V
xVPP-SWITCH OUTPUT

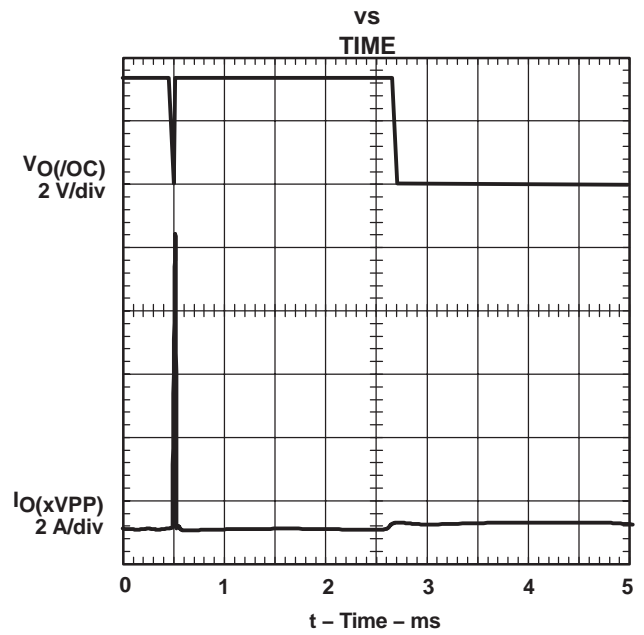


Figure 4

**OC RESPONSE WITH RAMPED
 OVERCURRENT-LIMIT LOAD ON 5-V
 xVCC-SWITCH OUTPUT**

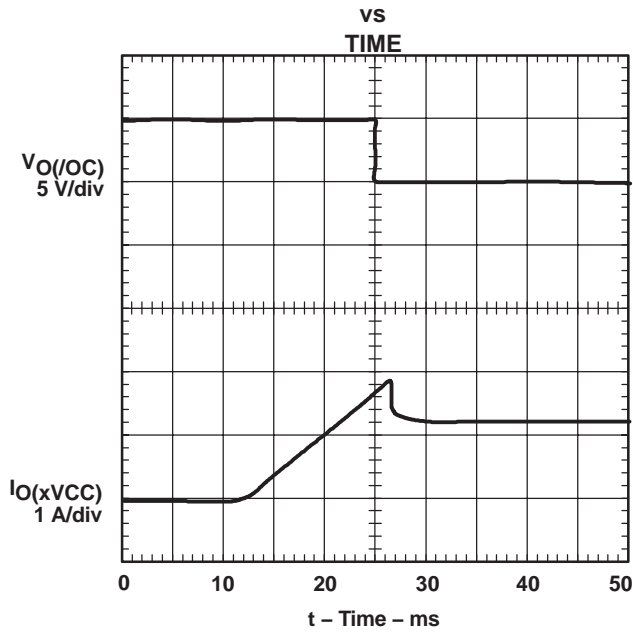


Figure 5

**OC RESPONSE WITH RAMPED
 OVERCURRENT-LIMIT LOAD ON 12-V
 xVPP-SWITCH OUTPUT**

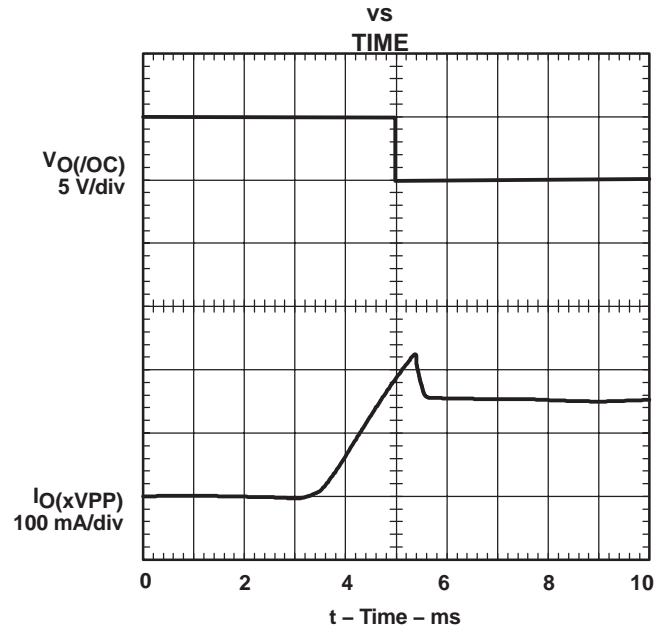


Figure 6

**TURNON PROPAGATION DELAY TIME, xVCC
 vs
 JUNCTION TEMPERATURE**

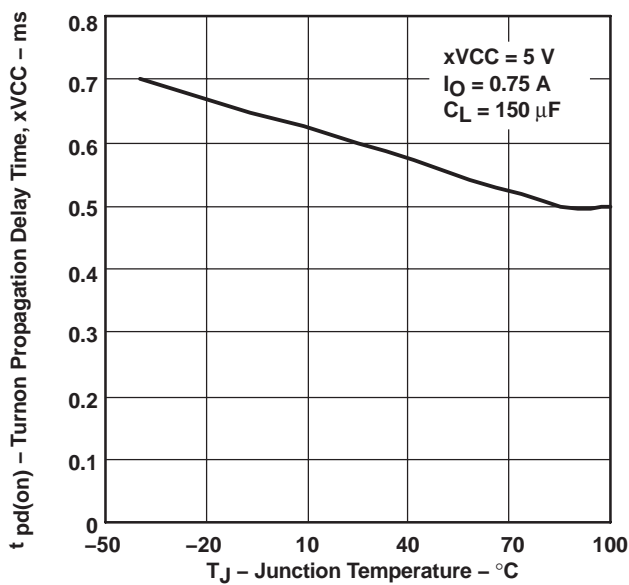


Figure 7

**TURNOFF PROPAGATION DELAY TIME, xVCC
 vs
 JUNCTION TEMPERATURE**

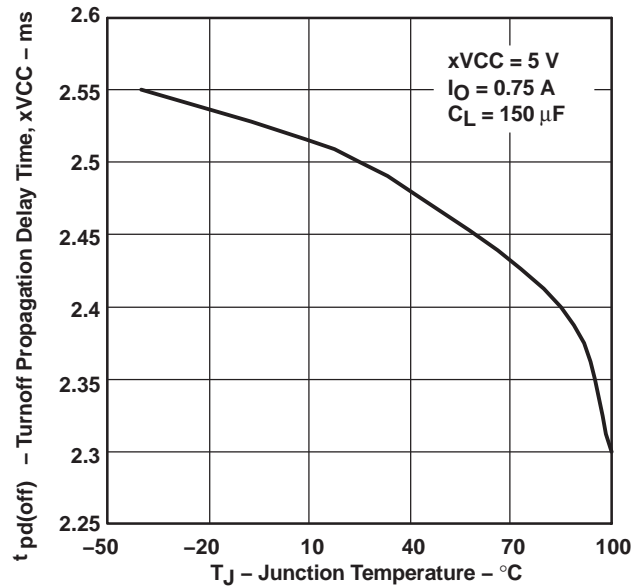
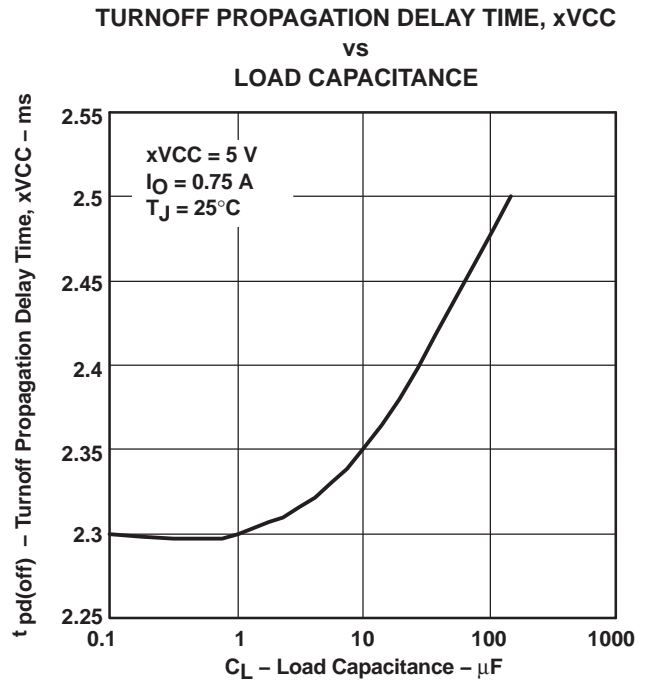
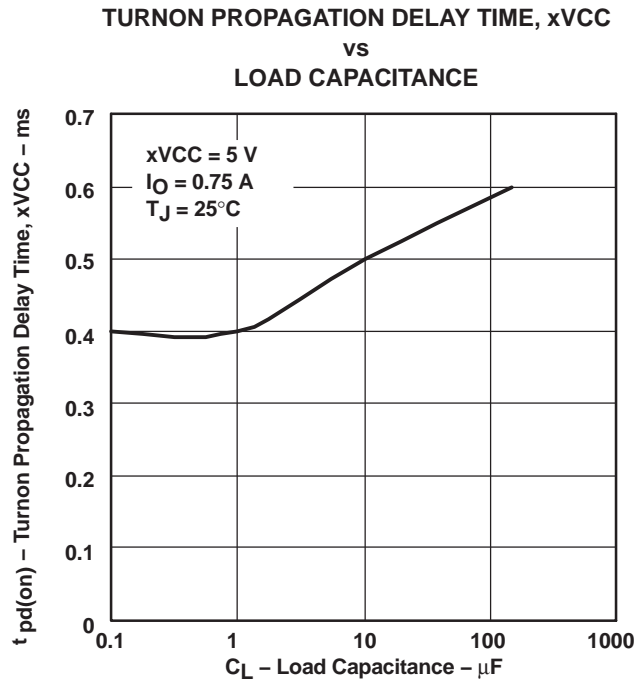
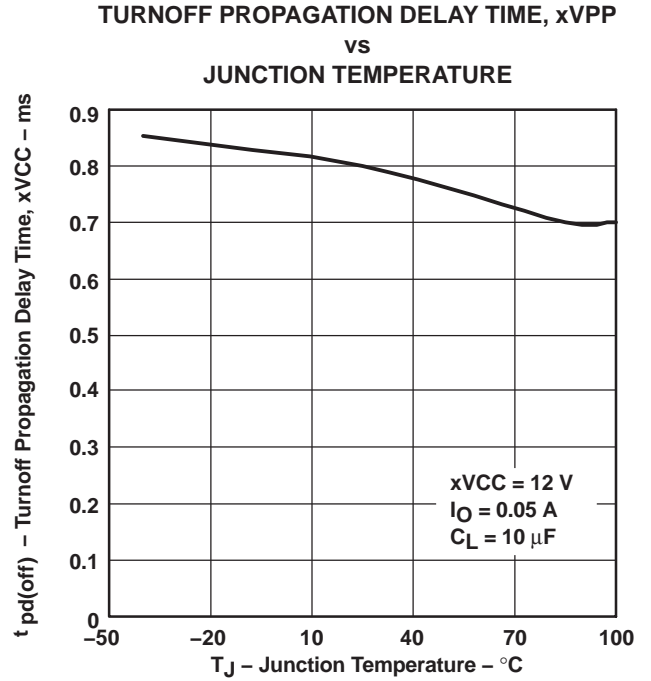
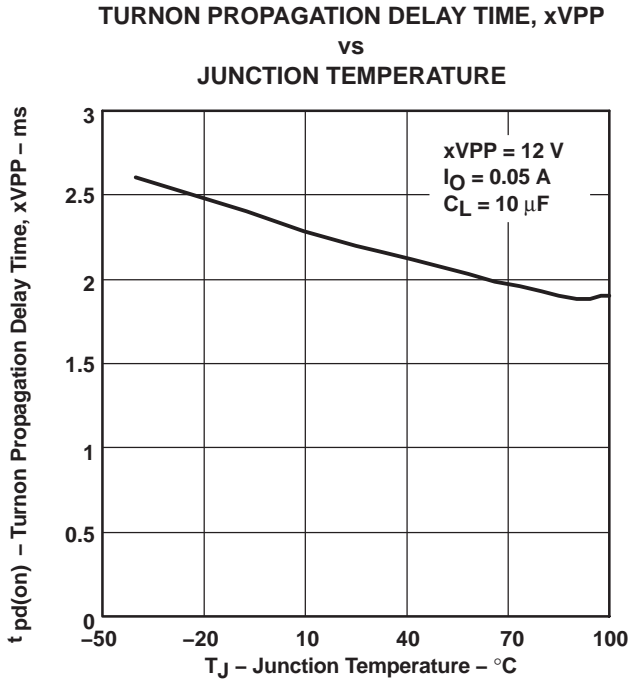


Figure 8



TURNON PROPAGATION DELAY TIME, xVPP
 VS
 LOAD CAPACITANCE

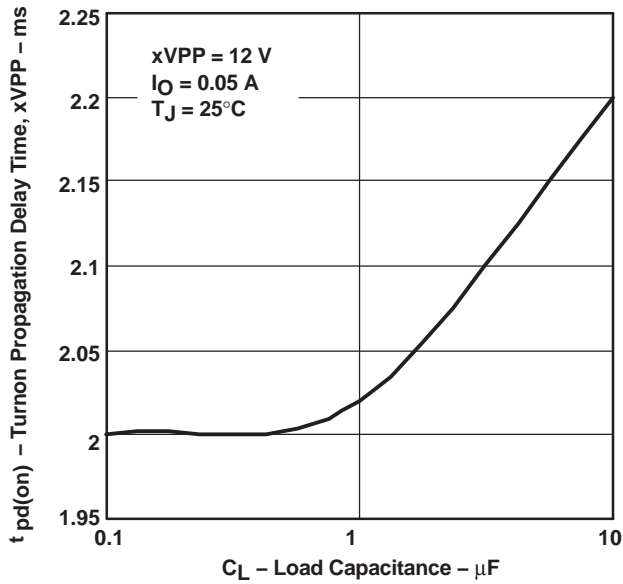


Figure 13

TURNOFF PROPAGATION DELAY TIME, xVPP
 VS
 LOAD CAPACITANCE

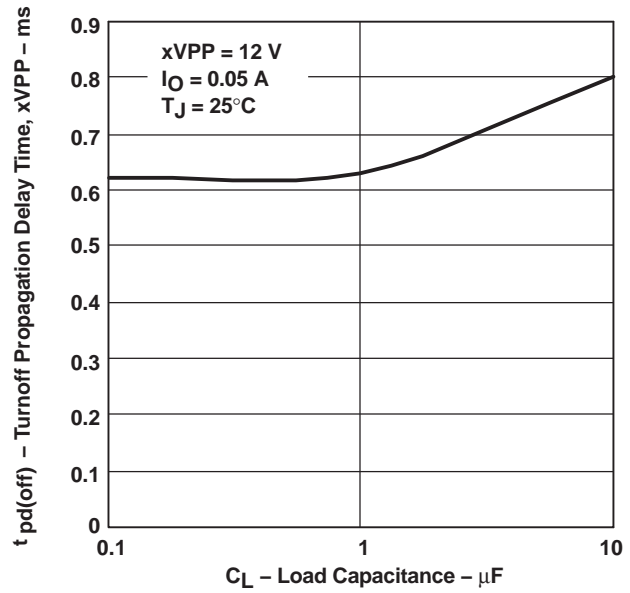


Figure 14

RISE TIME, xVCC
 VS
 JUNCTION TEMPERATURE

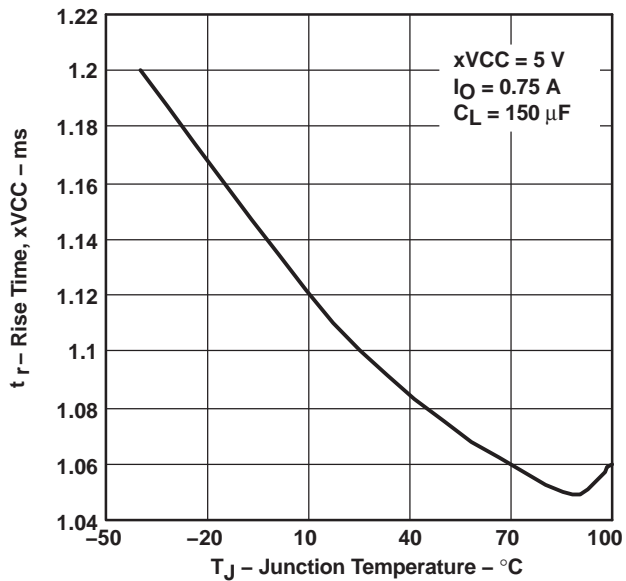


Figure 15

FALL TIME, xVCC
 VS
 JUNCTION TEMPERATURE

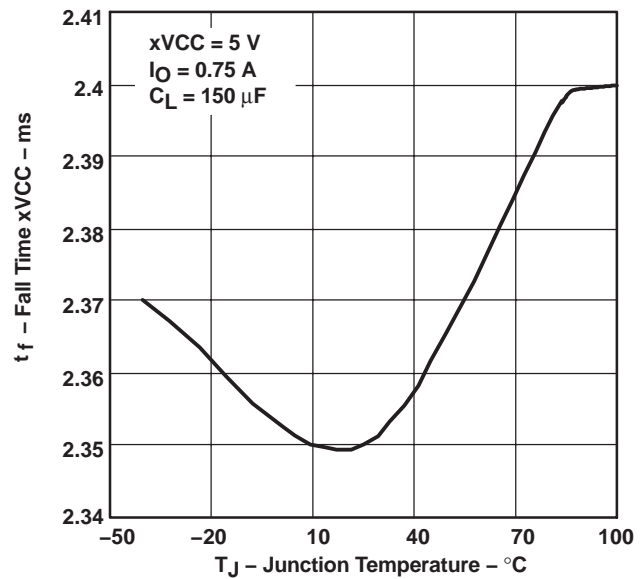


Figure 16

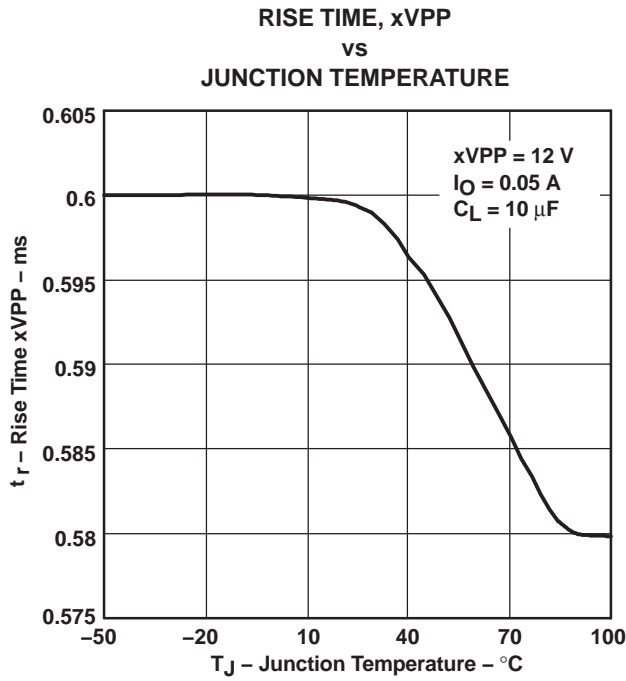


Figure 17

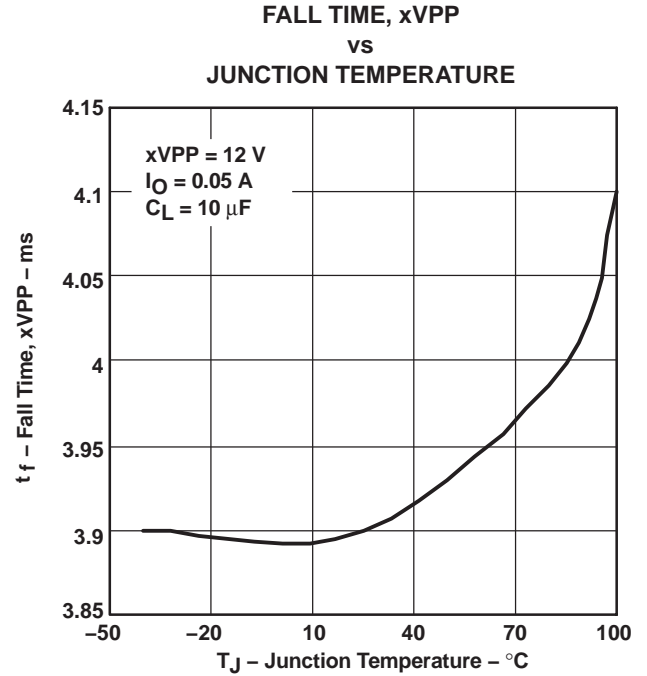


Figure 18

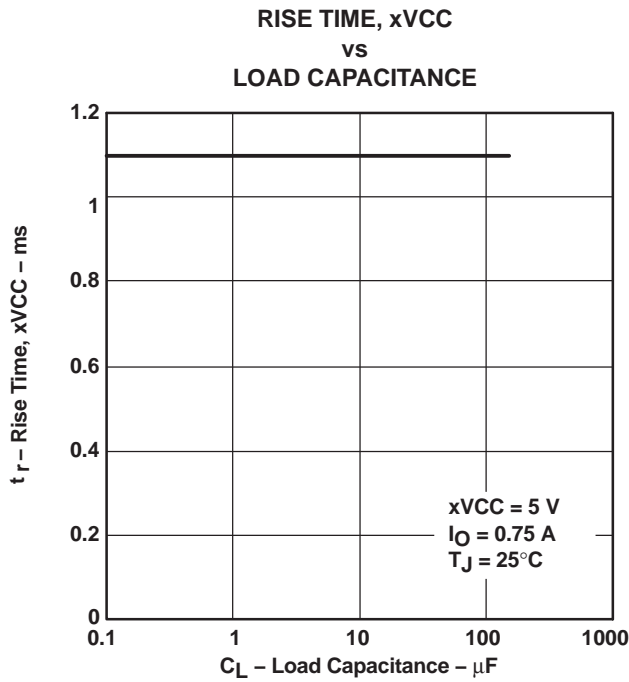


Figure 19

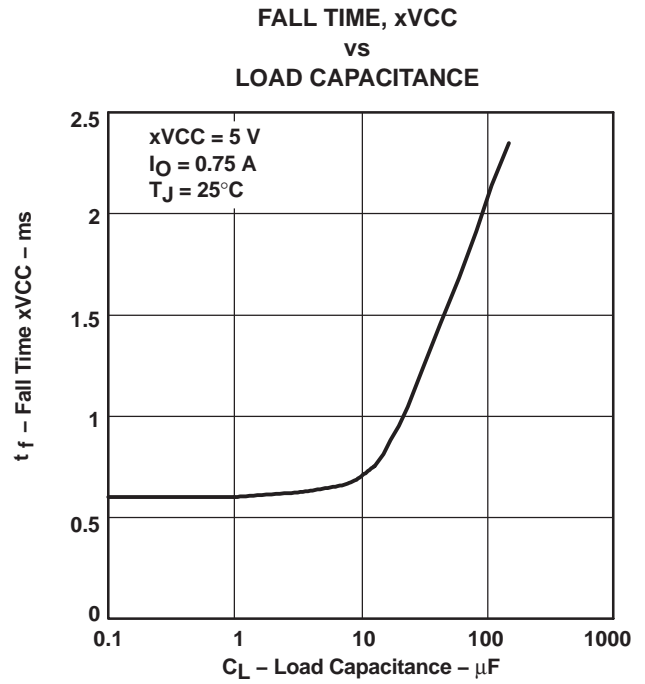


Figure 20

RISE TIME, xVPP
 VS
 LOAD CAPACITANCE

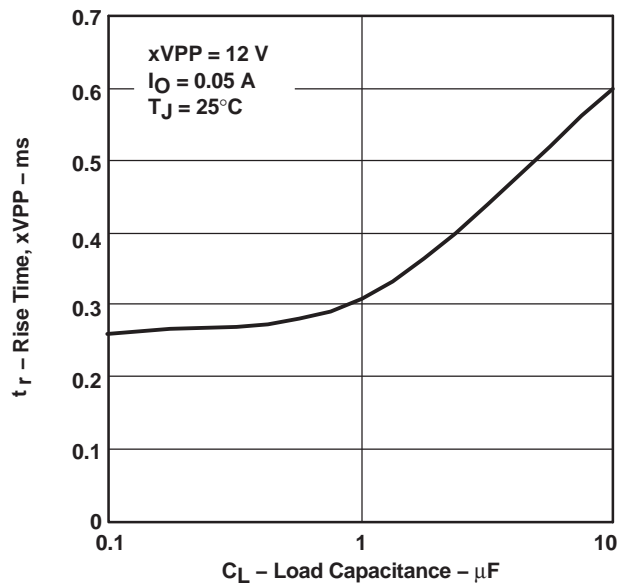


Figure 21

FALL TIME, xVPP
 VS
 LOAD CAPACITANCE

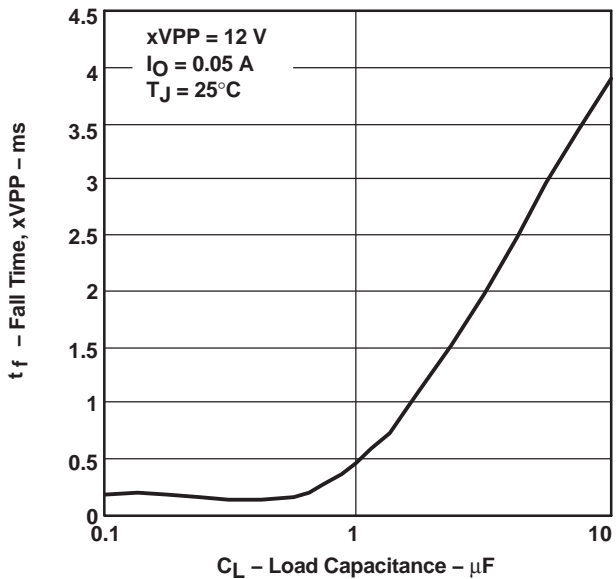


Figure 22

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
I_I	Input current, xVCC = 3.3 V	vs Junction temperature	23
	Input current, xVCC = 5 V		24
	Input current, xVPP = 12 V		25
$r_{DS(on)}$	Static drain-source on-state resistance, 3.3 V to xVCC switch	vs Junction temperature	26
	Static drain-source on-state resistance, 5 V to xVCC switch		27
	Static drain-source on-state resistance, 12 V to xVPP switch		28
V_O	xVCC switch voltage drop, 3.3-V input	vs Load current	29
	xVCC switch voltage drop, 5-V input		30
	xVPP switch voltage drop, 12-V input		31
I_{OS}	Short-circuit current limit, 3.3 V to xVCC	vs Junction temperature	32
	Short-circuit current limit, 5 V to xVCC		33
	Short-circuit current limit, 12 V to xVPP		34

INPUT CURRENT, xVCC = 3.3 V
vs
JUNCTION TEMPERATURE

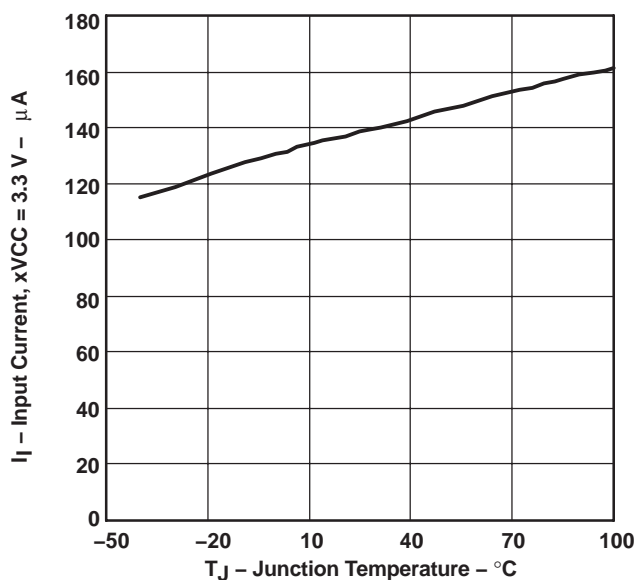


Figure 23

INPUT CURRENT, xVCC = 5 V
vs
JUNCTION TEMPERATURE

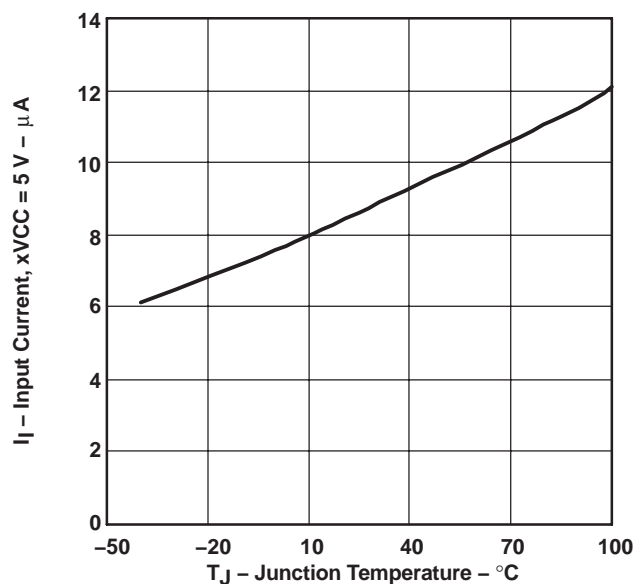


Figure 24

INPUT CURRENT, xVPP = 12 V
 VS
 JUNCTION TEMPERATURE

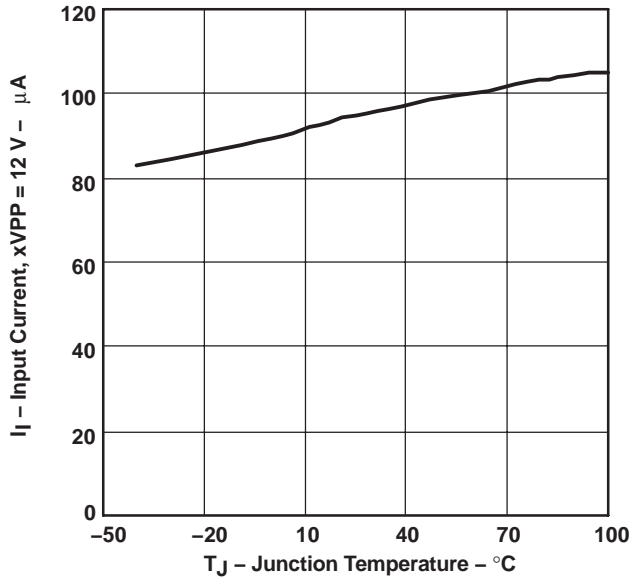


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
 3.3 V TO xVCC SWITCH
 VS
 JUNCTION TEMPERATURE

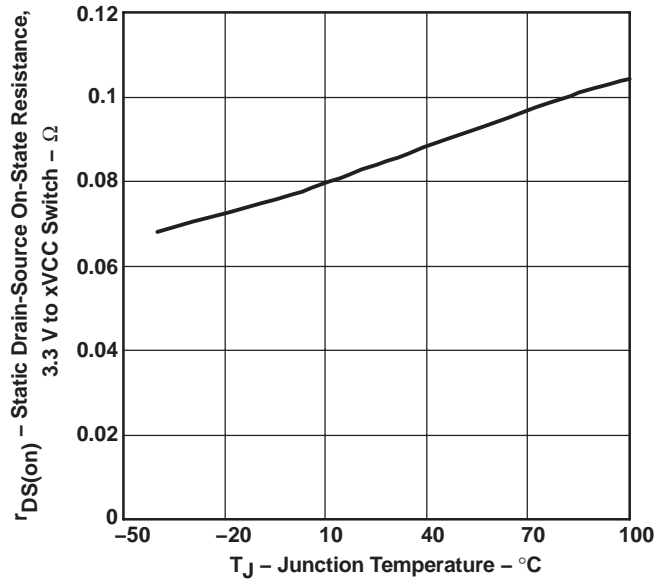


Figure 26

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
 5 V TO xVCC SWITCH
 VS
 JUNCTION TEMPERATURE

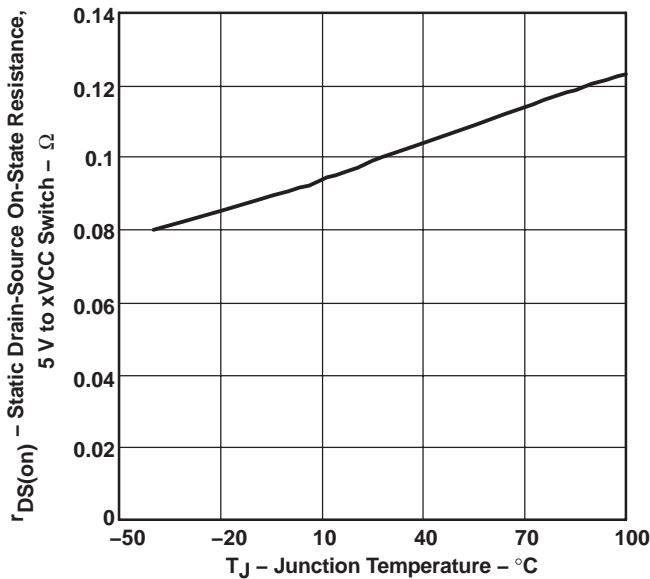


Figure 27

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
 12 V TO xVPP SWITCH
 VS
 JUNCTION TEMPERATURE

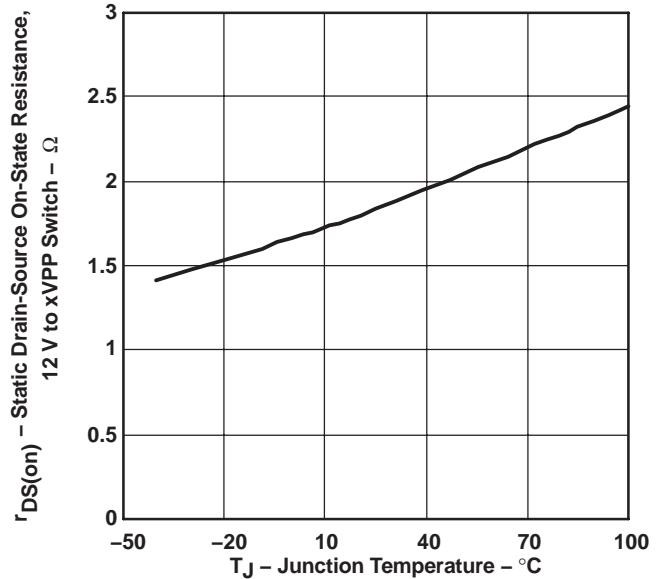


Figure 28

**xVCC SWITCH VOLTAGE DROP, 3.3-V INPUT
VS
LOAD CURRENT**

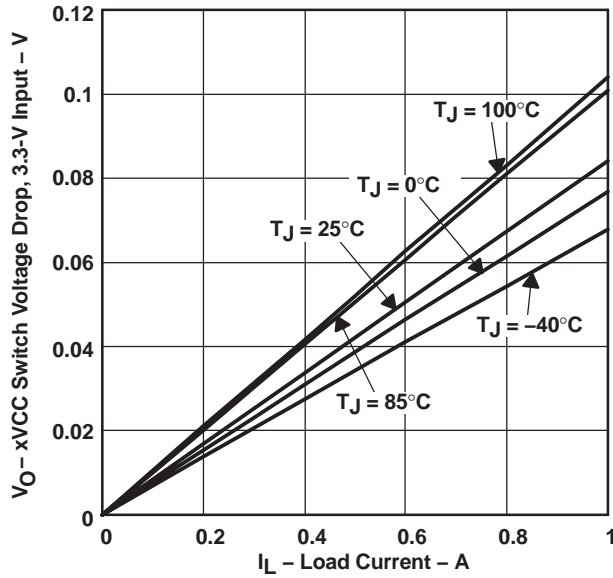


Figure 29

**xVCC SWITCH VOLTAGE DROP, 5-V INPUT
VS
LOAD CURRENT**

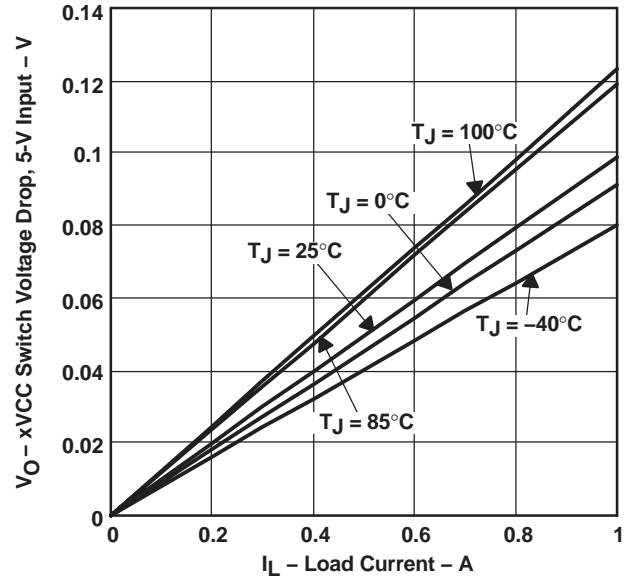


Figure 30

**xVPP SWITCH VOLTAGE DROP, 12-V INPUT
VS
LOAD CURRENT**

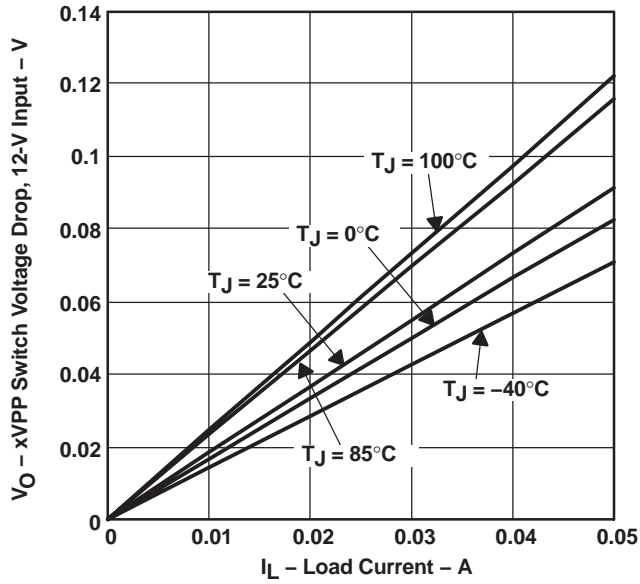


Figure 31

**SHORT-CIRCUIT CURRENT LIMIT, 3.3 V TO xVCC
VS
JUNCTION TEMPERATURE**

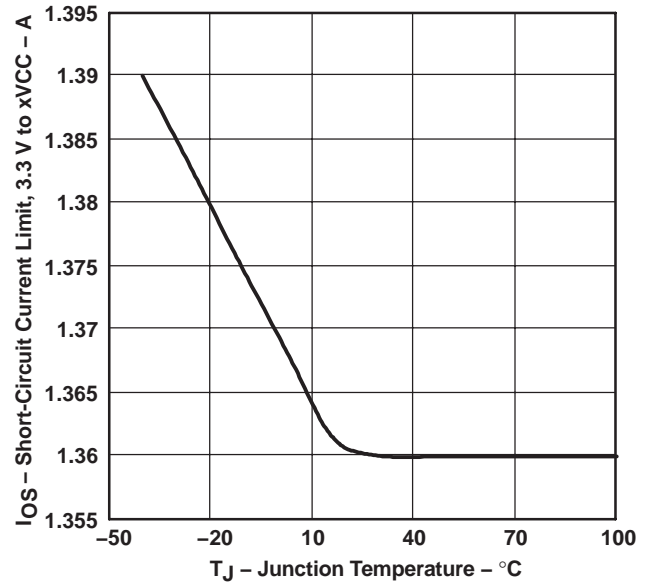


Figure 32

SHORT-CIRCUIT CURRENT LIMIT, 5 V TO xVCC
 VS
 JUNCTION TEMPERATURE

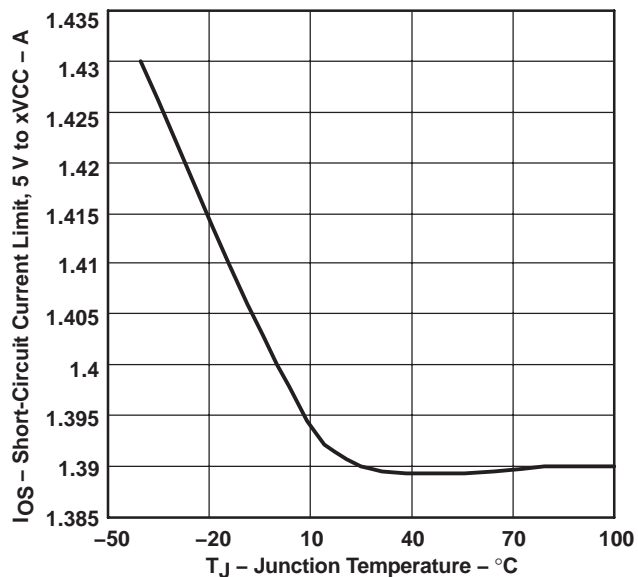


Figure 33

SHORT-CIRCUIT CURRENT LIMIT, 12 V TO xVPP
 VS
 JUNCTION TEMPERATURE

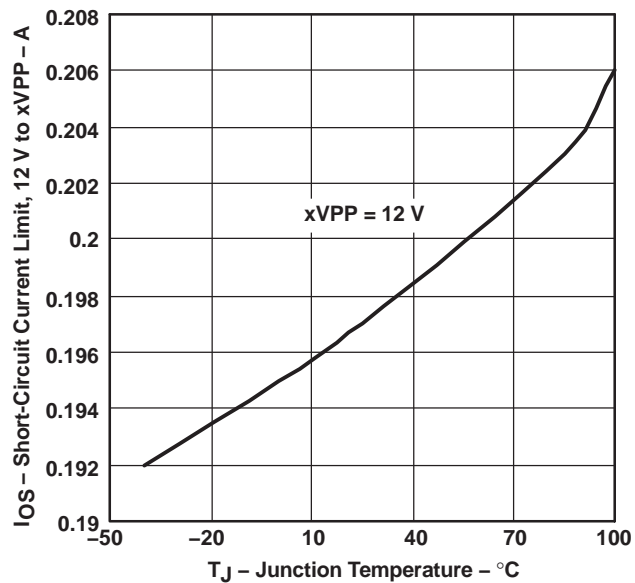


Figure 34

APPLICATION INFORMATION

OVERVIEW

PC Cards were initially introduced as a means to add flash memory to portable computers. The idea of add-in cards quickly took hold, and modems, wireless LANs, global positioning satellite system (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprising members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, so that cards and hosts from different vendors would be transparently compatible.

PC CARD POWER SPECIFICATION

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC} , two V_{pp} , and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are normally tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage are supplied through the V_{pp} terminals.

DESIGNING FOR VOLTAGE REGULATION

The current PCMCIA specification for output voltage regulation, $V_{O(\text{reg})}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(\text{reg})}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card results from resistive losses, V_{PCB} , in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS} , for the device would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(\text{reg})} - V_{PS(\text{reg})} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2204A, TPS2206A, or TPS2210A. The voltage drop is the output current multiplied by the switch resistance of the device. Therefore, the maximum output current, $I_{O \text{ max}}$, that can be delivered to the PC Card in regulation is the allowable voltage drop across the device, divided by the output-switch resistance.

$$I_{O \text{ max}} = \frac{V_{DS}}{r_{DS(\text{on})}}$$

The xVCC outputs have been designed to deliver the peak and average currents defined by the PC Card specification within regulation over the operating temperature range. The xVPP outputs have been designed to deliver 100 mA continuously.

OVERCURRENT AND OVERTEMPERATURE PROTECTION

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even extremely robust systems could undergo rapid battery discharge into a damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. The reliability of fused systems is poor, in comparison, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2204A, TPS2206A, and TPS2210A take a two-pronged approach to overcurrent protection. Overcurrent protection is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 100 mA to 250 mA, typically around 200 mA.

Second, when an overcurrent condition is detected, the device asserts an active low \overline{OC} signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. If an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis. Thermal limiting prevents destruction of the IC from overheating beyond the package power-dissipation ratings.

During power up, the devices control the rise times of the xVCC and xVPP outputs and limit the inrush current into a large load capacitance, faulty card, or connector.

12-V SUPPLY NOT REQUIRED

Some PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The TPS2204A, TPS2206A, and TPS2210A offer considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 3.3-V input. Therefore, the external 12-V supply can be disabled except when needed by the PC Card in the slot, thereby extending battery lifetime. A special feature in the 12-V circuitry actually helps to reduce the supply current demanded from the 3.3-V input. When 12 V is supplied and requested at the V_{pp} output, a voltage selection circuit draws the charge-pump drive current for the 12-V FETs from the 12-V input. This selection is automatic and effectively reduces demand fluctuations on the normal 3.3-V V_{CC} rail. For proper operation of this feature, a minimum 3.3-V input capacitance of 4.7 μ F is recommended, and a minimum 12-V input ramp-up rate of 12 V/50 ms (240 V/s) is required. Additional power savings are realized during a software shutdown in which quiescent current drops to a maximum of 1 μ A.

BACKWARD COMPATIBILITY

The TPS2206A is backward compatible with the TPS2206 product, with the following considerations. An active low /SHDN is added to provide fast shutdown capability. Also, the TPS2206A does not have the active-high RESET input, which is left as no connect.

3.3-V input is required for device operation of TPS2206A.

VOLTAGE-TRANSITIONING REQUIREMENT

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2204A, TPS2206A, and TPS2210A meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power \overline{RESET} . PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance cannot be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The devices include discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

SHUTDOWN MODE

In the shutdown mode, which can be controlled by $\overline{\text{SHDN}}$ or bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is reduced to 1 μA or less to conserve battery power.

POWER-SUPPLY CONSIDERATIONS

These switches have multiple pins for each 3.3-V (except for the TPS2210A) and 5-V power input and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and power loss. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2204A, TPS2206A, and TPS2210A, the power-supply inputs should be bypassed with at least a 4.7- μF electrolytic or tantalum capacitor paralleled by a 0.047- μF to 0.1- μF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1- μF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the devices and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below -0.3 V .

RESET INPUT

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low-impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active low $\overline{\text{RESET}}$ input closes internal ground switches S1, S4, S7, and S11 with all other switches left open. The devices remain in the low-impedance output state until the signal is deasserted and new data is clocked in and latched. The input serial data cannot be latched during reset mode. $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use an active-low reset voltage supervisor. The $\overline{\text{RESET}}$ pin has an internal 150-k Ω pullup resistor.

CALCULATING JUNCTION TEMPERATURE

The switch resistance, $r_{\text{DS(on)}}$, is dependent on the junction temperature, T_J , of the die. The junction temperature is dependent on both $r_{\text{DS(on)}}$ and the current through the switch. To calculate T_J , first find $r_{\text{DS(on)}}$ from Figures 26 through 28, using an initial temperature estimate about 30°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{\text{DS(on)}} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta\text{JA}} \right) + T_A, R_{\theta\text{JA}} = 108^\circ\text{C/W}$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

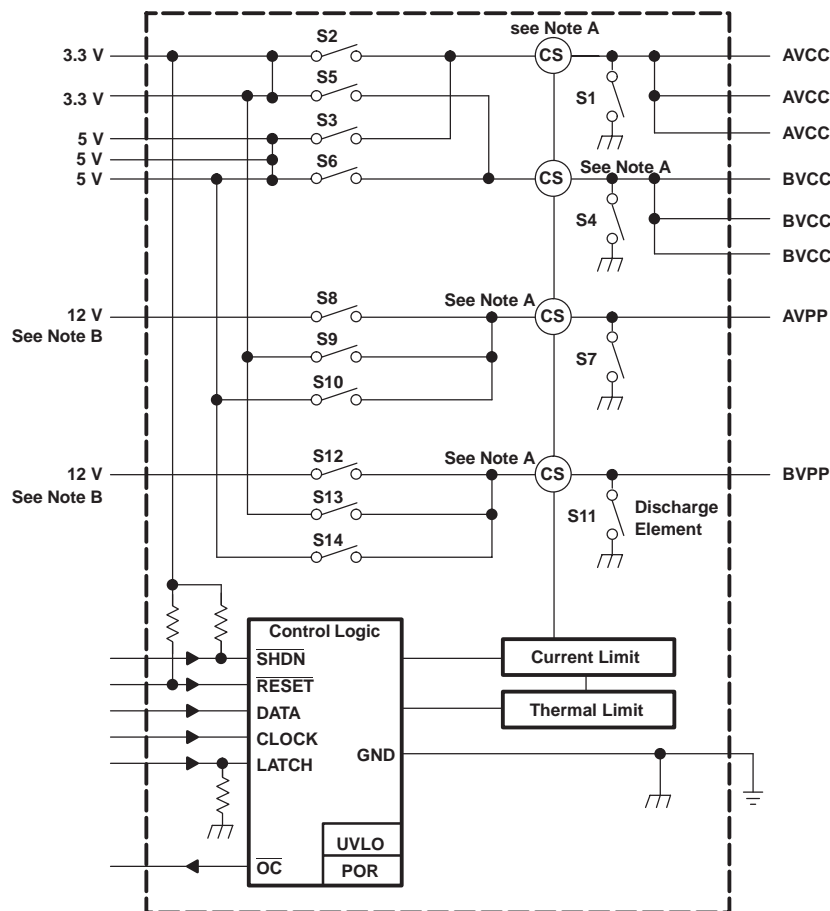
LOGIC INPUTS AND OUTPUTS

The serial interface consists of the DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figure 2). The 9-bit (D0–D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{PP} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

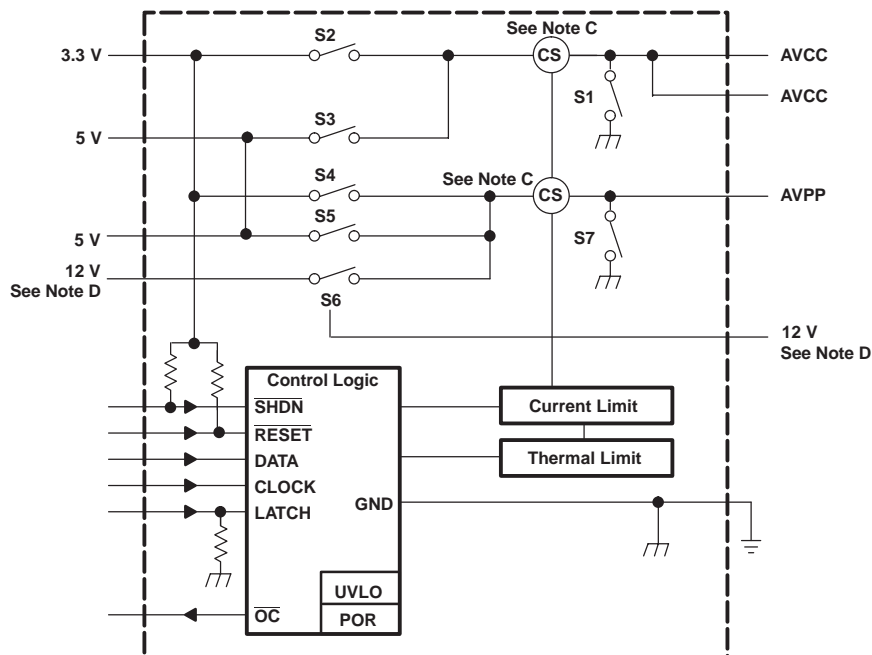
The serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent or overtemperature condition in any of the V_{CC} and V_{PP} outputs as previously discussed.



- NOTES: A. Current sense
 B. The two 12-V pins must be externally connected.

Figure 35. Internal Switching Matrix, TPS2204A and TPS2206A



NOTES: C. Current sense
D. The two 12-V pins must be externally connected.

Figure 36. Internal Switching Matrix, TPS2210A

CONTROL LOGIC

AVPP

CONTROL SIGNALS			OUTPUT	CONTROL SIGNALS			OUTPUT
D8 (SHDN)	D0	D1	VAVPP	D8 (SHDN)	D4	D5	VBVPP
1	0	0	0 V	1	0	0	0 V
1	0	1	AVCC ⁽¹⁾	1	0	1	BVCC ⁽²⁾
1	1	0	12 V	1	1	0	12 V
1	1	1	Hi-Z	1	1	1	Hi-Z
0	X	X	Hi-Z	0	X	X	Hi-Z

⁽¹⁾ Output depends on AVCC

⁽²⁾ Output depends on BVCC

AVCC

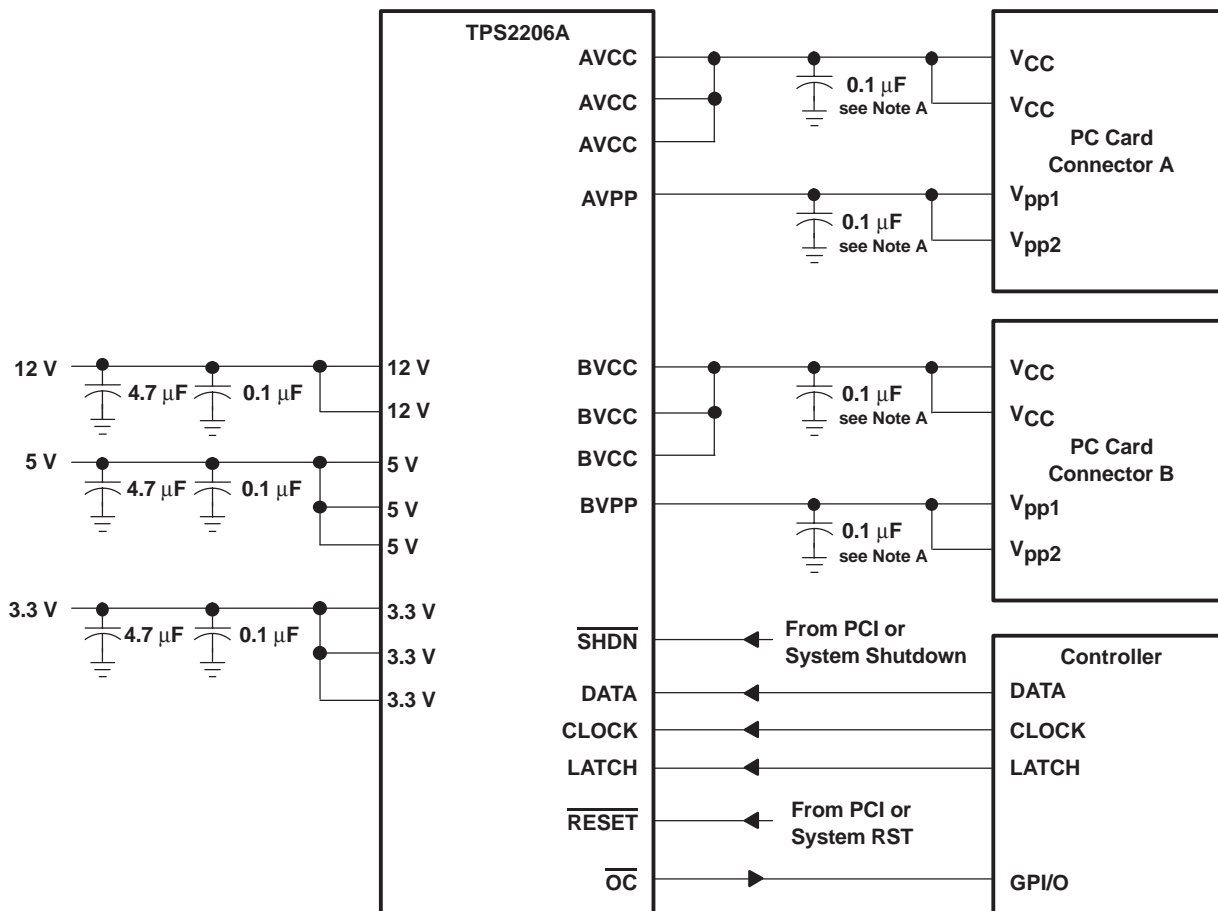
CONTROL SIGNALS			OUTPUT	CONTROL SIGNALS			OUTPUT
D8 (SHDN)	D3	D2	VAVCC	D8 (SHDN)	D6	D7	VBVCC
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

USING THE DEVICES WITH 11-BIT SERIAL DATA INTERFACE CONTROLLERS

Even though the control logic table only shows a 9-bit interface, it can be used with most 11-bit serial data interface controllers. With the use of the latch input, the TPS2204A, TPS2206A, and TPS2210A only latch the last 9 bits from the serial stream. This means that for an 11-bit serial stream, bits 9 and 10 are ignored. 11-bit serial interface controllers use bits 9 and 10 for independent voltage selection of 3.3 V and 5 V between xV_{CC} and xV_{PP} .

ESD PROTECTIONS (see FIGURE 37)

All TPS2206A inputs and outputs of these devices incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xV_{CC} and xV_{PP} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1- μ F capacitors protects the devices from discharges up to 10 kV.



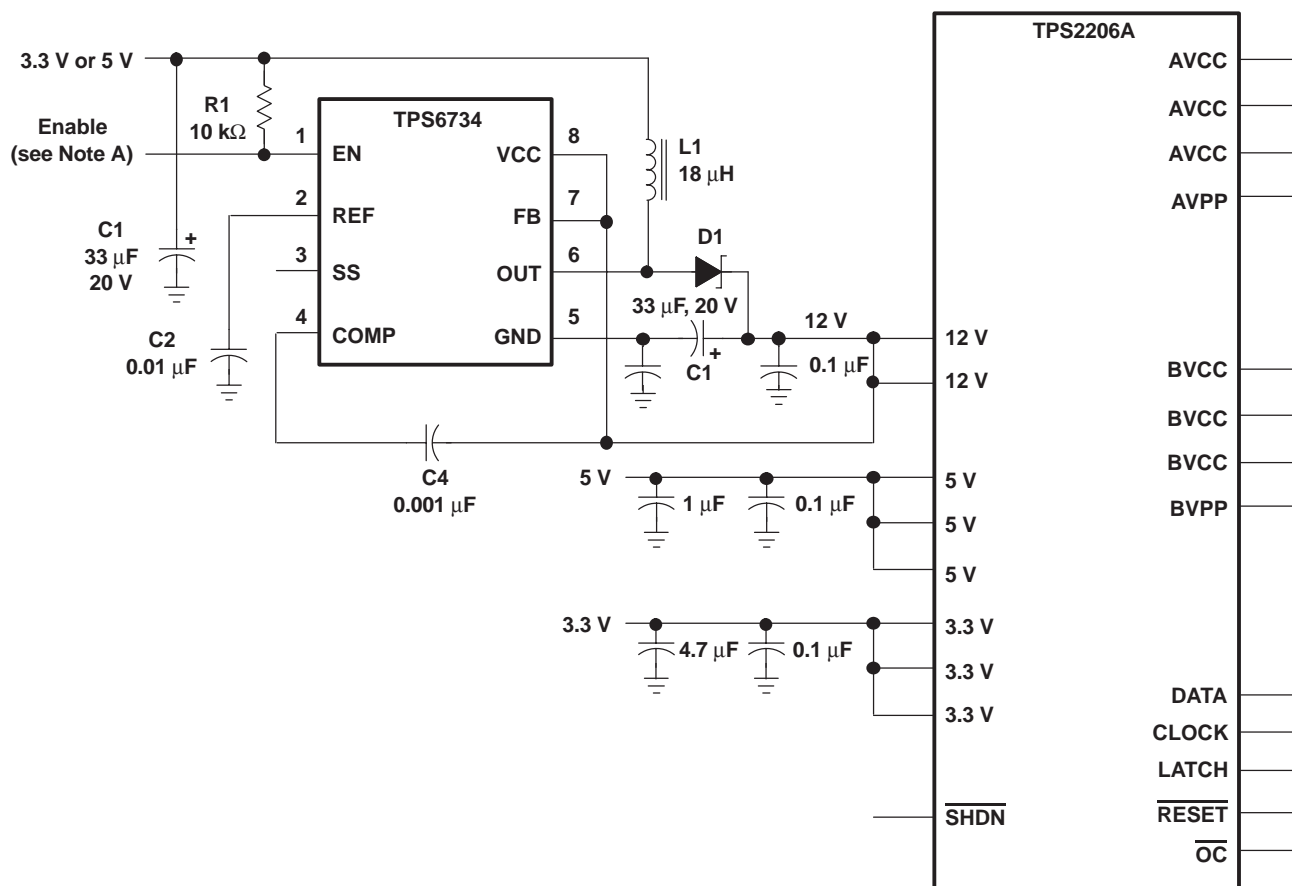
NOTE A: Maximum recommended output capacitance for xV_{CC} is 220 μ F including card capacitance, and for xV_{PP} is 10 μ F, without \overline{OC} glitch when switches are powered on.

Figure 37. Detailed Interconnections and Capacitor Recommendations

12-V FLASH MEMORY SUPPLY

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 36, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in² of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μ A when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7- Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference, pin 2 of TPS6734, is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 38. TPS2206A With TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2206ADB	ACTIVE	SSOP	DB	30	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2206A	Samples
TPS2210APWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2210A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

GENERIC PACKAGE VIEW

PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

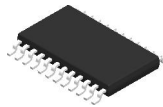
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

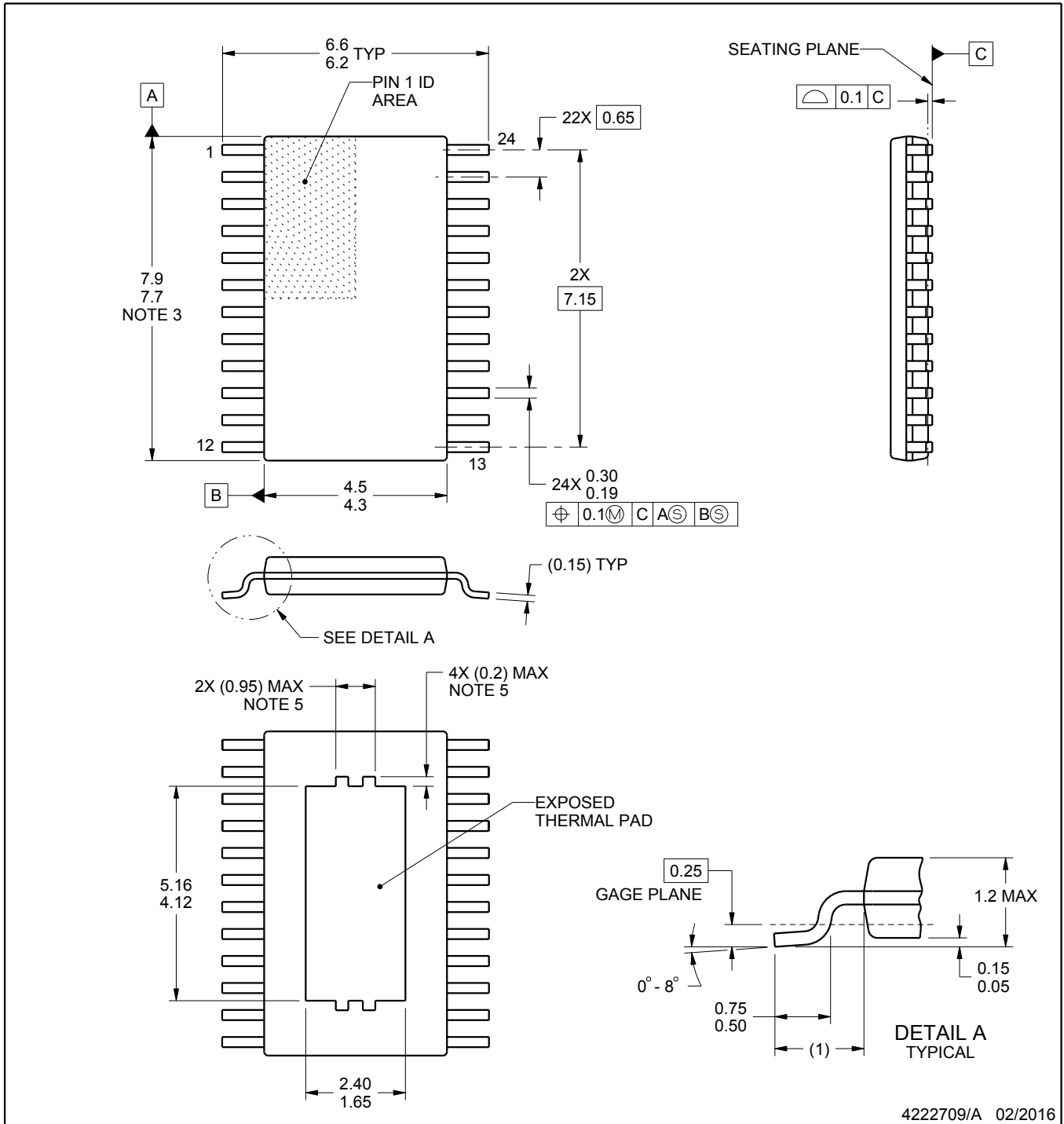


PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



4222709/A 02/2016

NOTES:

PowerPAD is a trademark of Texas Instruments.

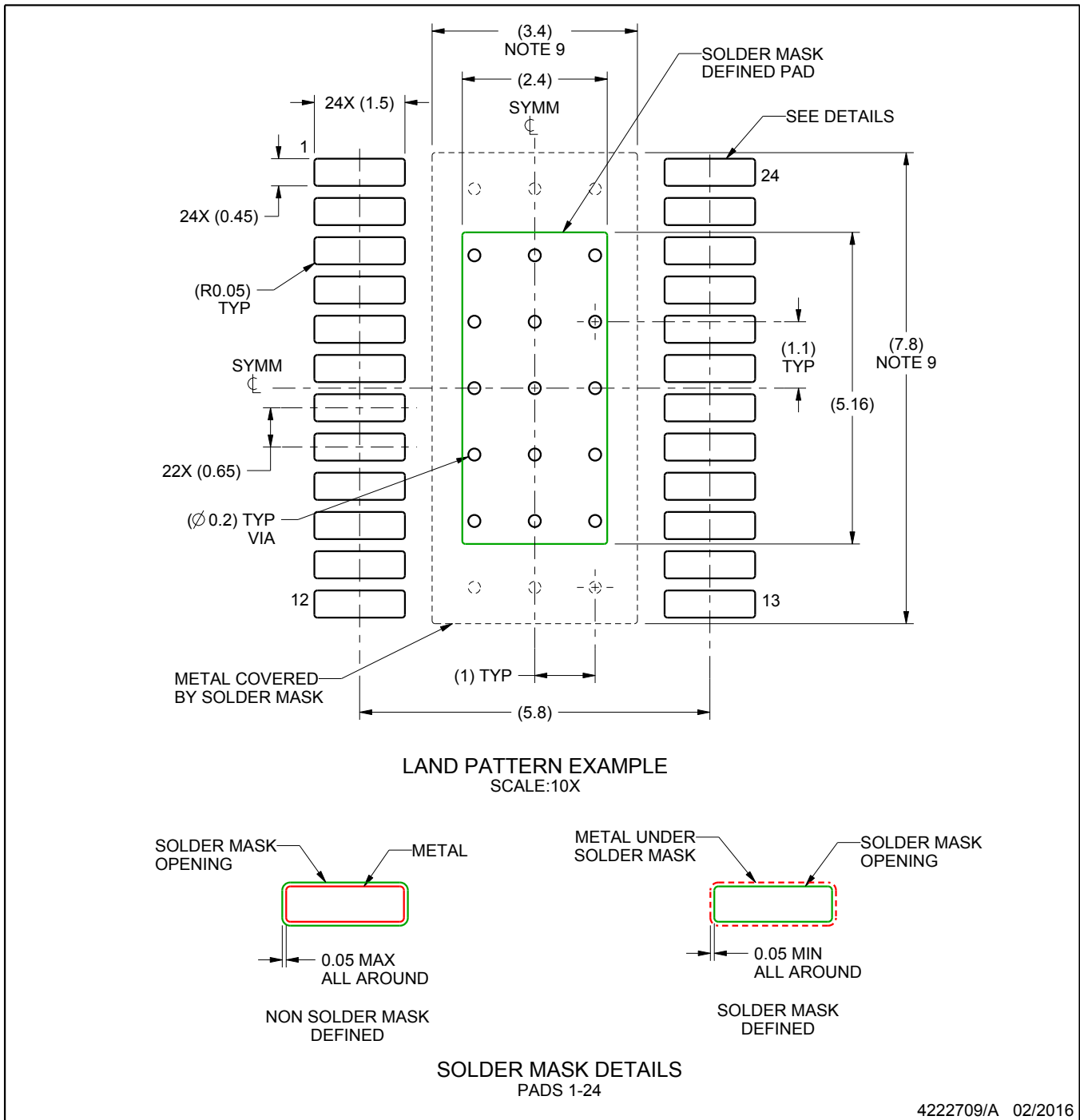
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.

EXAMPLE BOARD LAYOUT

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

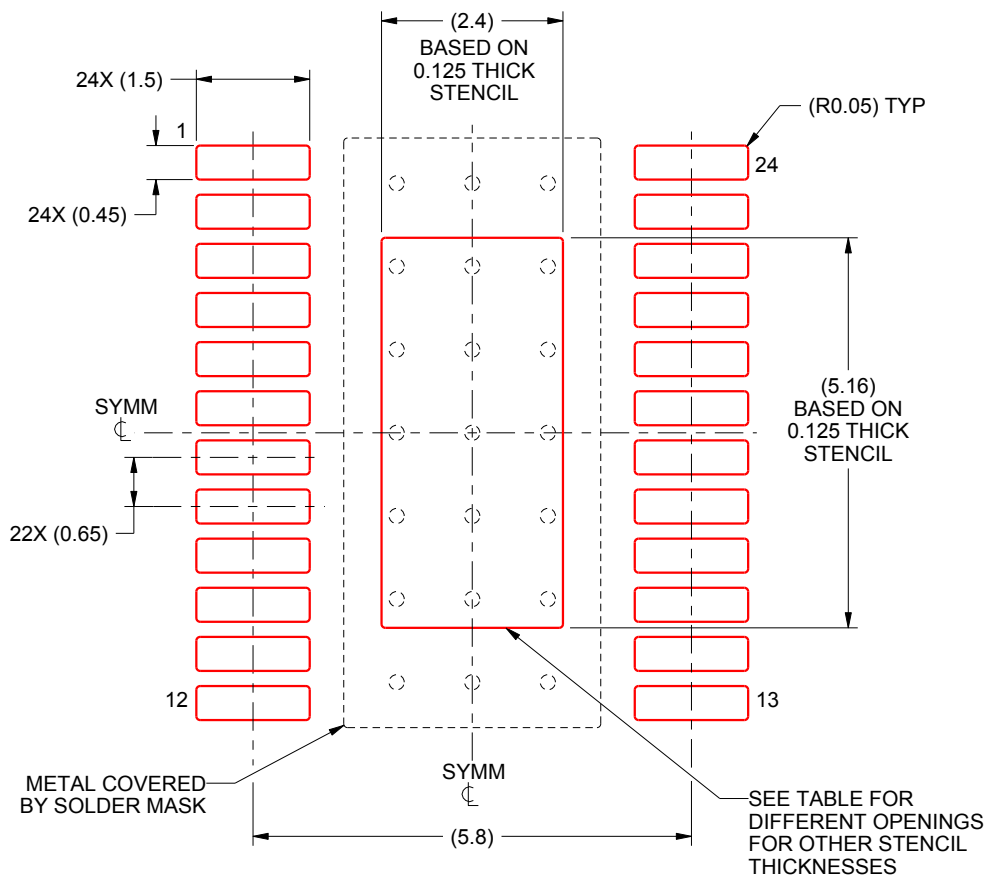
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
 EXPOSED PAD
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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