# TPS22981 3.3-V to 18-V Thunderbolt™ Power Mux

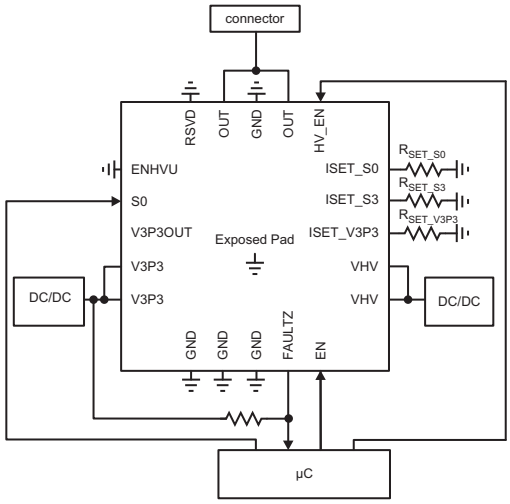
## 1 Features

- Powered from 3.3 V
- 4.5-V to 19.8-V High-Voltage Switch
- 3-V to 3.6-V Switch
- Adjustable Current Limit
- Thermal Shutdown
- Make Before Break Switch
- High-Voltage Discharge Before Low-Voltage Make
- Reverse Current Blocking

## 2 Applications

- Notebook Computers
- Desktop Computers
- Power Management Systems

### Typical Application




## 3 Description

The TPS22981 device is a current-limited power mux providing a connection to a peripheral device from either a low-voltage supply (3 V to 3.6 V) or a high-voltage supply (4.5 V to 19.8 V). The desired output is selected by digital control signals.

The high-voltage (VHV) and low-voltage (V3P3) switch current limits are set with external resistance. Once the current limit is reached, the TPS22981 will control the switch to maintain the current at this limit.

When the high-voltage supply is not present, the TPS22981 will maintain the connection to the output from the low-voltage supply. Upon the presence of a high-voltage line and high-voltage enable signal, the high-voltage switch is turned on in conjunction with the low-voltage switch until a reverse current is detected through the low-voltage switch, allowing a seamless transition from low voltage to the high-voltage supply with minimal droop and shoot-through current.

To prevent current backflow during a switch over from a VHV connection to a V3P3 connection, the TPS22981 will break the VHV connection, discharge the output to approximately 3.3 V and then make the V3P3 connection. The output may transition to 0 V when a load is present, before returning to 3.3 V.

The TPS22981 is available in a 4 mm × 4 mm × 1 mm VQFN package.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS22981 | VQFN (20) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (September 2013) to Revision B** **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Replaced all the equations links needed to calculate resistor values in the table to the correct equation, Equation 1 ... 3
- Changed V3P3OUT pinout 'capacitor' to 'capacitor to GND' throughout the data sheet ... 3
- Added labels to all pins in the *Functional Block Diagram* ... 8
- Changed *Input Inductive Bounce at Short Circuit* section title to *Input Inductive Bounce* ... 15
- Updated Figure 9 to show the EN pin as a device input ... 15

**Changes from Original (December 2012) to Revision A** **Page**

- Removed *Ordering Information* table. ... 3
- Added $R_{OUTDIS}$ parameter to the Electrical Characteristics table ... 5
- Updated UVLO ENABLE section ... 13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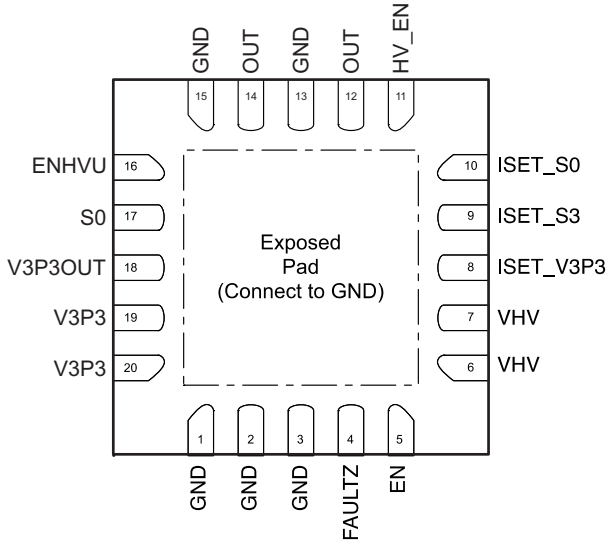
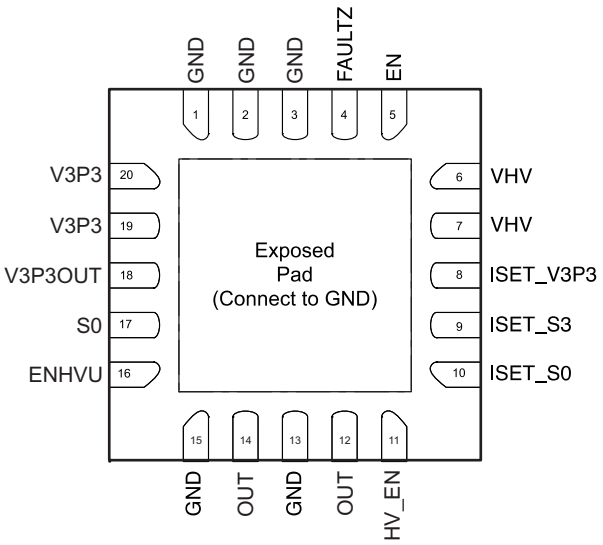
# 5 Pin Configuration and Functions

**RGP Package**
**VQFN With Exposed Thermal Pad**
**Top View**




**RGP Package**
**VQFN With Exposed Thermal Pad**
**Bottom View**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 5 | I | Device active-high enable. |
| ENHVU | 16 | I | Enable VHV UVLO control of device enable. When asserted high, both V3P3 and VHV must be present for device enable. When low, only V3P3 must be present for device enable. |
| FAULTZ | 4 | O | Fault condition output. This pin is an open-drain pulldown indicating a fault condition. Place a pullup resistance ($R_{FAULTZ}$) between this pin and V3P3. Float pin or tie pin to GND if unused. |
| GND | 1, 2, 3, 13, 15 | P | Device ground. All GND pins must be connected to board ground. |
| GND | EP | P | Exposed pad must be connected to device GND. |
| HV_EN | 11 | I | Active-high voltage output enable. |
| ISET_S0 | 10 | I | Sets the current limit for VHV in S0 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value. |
| ISET_S3 | 9 | I | Sets the current limit for VHV in S3 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value. |
| ISET_V3P3 | 8 | I | Sets the current limit for V3P3. Place resistor between this pin and GND. See Equation 1 to calculate resistor value. |
| OUT | 12, 14 | O | Power output. Place a minimum of 1-µF capacitor to GND as close to this pin as possible. |
| S0 | 17 | I | When this pin is asserted, the device is put in S0 mode. Otherwise the device operates in S3 mode. |
| V3P3 | 19, 20 | P | 3.3-V power supply input. Place a minimum of 0.1-µF capacitor to GND as close to this pin as possible. |
| V3P3OUT | 18 | O | 3.3-V bypass output. When ENHVU is low, this path is enabled by EN and the V3P3 UVLO. When ENHVU is high, this path is enabled by EN and both the V3P3 UVLO and the VHV UVLO. Place a minimum 0.1-uF capacitor to GND as close to this pin as possible. |
| VHV | 6, 7 | P | High voltage power supply input. See the *Input Inductive Bounce* section for more information. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_I$ | Input voltage on V3P3 (VDD)(2) | –0.3 | 3.6 | V |
| | Input voltage on EN, HV_EN, ENHVU, ISET_V3P3, ISET_S0, ISET_S3, S0(2) | –0.3 | V3P3 + 0.3 | |
| | Output voltage on FAULTZ | –0.3 | V3P3 + 0.3 | |
| | Input voltage on VHV(2) | –0.3 | 20 | |
| | Output voltage at OUT(2) | –0.3 | 20 | |
| | Voltage between VHV and OUT ($V_{VHV} – V_{OUT}$) | –7 | 20 | |
| | Output voltage at V3P3OUT(2) | –0.3 | V3P3 + 0.3 | |
| $T_A$ | Operating ambient temperature(3) | –40 | 85 | °C |
| $T_{J\ (MAX)}$ | Maximum operating junction temperature | | 110 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [TA(max)] is dependent on the maximum operating junction temperature [TJ(max)], the maximum power dissipation of the device in the application [PD(max)], and the junction-to-ambient thermal resistance of the part/package in the application (θJA), as given by the following equation: TA(max) = TJ(max) – (θJA × PD(max))

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{3P3}$ | Supply voltage | | 3 | 3.6 | V |
| $V_{HV}$ | | | 4.5 | 19.8 | V |
| $I_{LIM3P3OUT}$ | V3P3OUT switch current | | 0 | 500 | mA |
| $V_{IH}$ | Input logic high | EN, HV_EN, ENHVU, S0 | V3P3 – 0.6 | V3P3 | V |
| $V_{IL}$ | Input logic low | EN, HV_EN, ENHVU, S0 | 0 | 0.6 | V |
| $R_{SET\_V3P3}$ | 3.3-V switch current limit set resistance | | 26.7 | 402 | kΩ |
| $R_{SET\_S0}$ | VHV switch current limit in S0 mode set resistance | | 26.7 | 402 | kΩ |
| $R_{SET\_S3}$ | VHV switch current limit in S3 mode set resistance | | 26.7 | 402 | kΩ |
| $R_{FAULTZ}$ | FAULTZ pullup resistance to V3P3 | | 30 | | kΩ |


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS22981 RGP (VQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 39.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Unless otherwise noted the specification applies over the $V_{DD}$ range and operating junction temp –40°C ≤ $T_J$ ≤ 85°C. Typical values are for $V_{3P3}$ = 3.3 V, $V_{HV}$ = 15 V, and $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES AND CURRENTS** | | | | | | |
| $V_{3P3}$ | V3P3 input voltage range | | 3 | 3.3 | 3.6 | V |
| $V_{HV}$ | VHV input voltage range | | 4.5 | | 19.8 | V |
| $I_{VHVACT}$ | Active quiescent current from VHV | HV_EN = 1, EN = 1 | | | 150 | µA |
| $I_{VHVSD}$ | Shutdown leakage current from VHV | HV_EN = 0, EN = 0 or 1 | | | 60 | µA |
| $I_{DDACT}$ | Active quiescent current from V3P3 | EN = 1, HV_EN = 0 | | | 500 | µA |
| $I_{DDACTHV}$ | | EN = 1, HV_EN = 1 | | | 500 | µA |
| $I_{DDSD}$ | Shutdown quiescent current from V3P3 | EN = 0, OUT = 0 V | | | 30 | µA |
| $I_{DIS}$ | OUT discharge current | EN = 1, $V_{HV}$ = 5V, HV_EN = 1→0 | 5 | | 10 | mA |
| $I_{IN}$ | HV_EN, EN, ENHVU, S0, S3 input pin leakage | V = 0 V | | | 1 | µA |
| | | V = V3P3 | | | 1 | |
| **SWITCH AND RESISTANCE CHARACTERISTICS** | | | | | | |
| $R_{SHV}$ | VHV switch resistance | $V_{HV}$ = 5V to 18V, $I_{VHV}$ = 0.9A | | | 250 | mΩ |
| $R_{S3P3}$ | V3P3 switch resistance | $V_{3P3}$ = 3.3 V, $I_{V3P3}$ = 0.9 A | | | 125 | mΩ |
| $R_{S3P3BYP}$ | V3P3 bypass switch resistance | $V_{3P3}$ = 3.3 V, $I_{V3P3}$ = 500 mA | | | 500 | mΩ |
| $R_{OUTDIS}$ | OUT pulldown resistance when disabled | EN = 0 | 1.5 | 2.5 | 4 | kΩ |
| $V_{OLFAULTZ}$ | FAULTZ VOL | $I_{FAULTZ}$ = 250 µA | | | 0.6 | V |
| **VOLTAGE THRESHOLDS** | | | | | | |
| $V_{HVUVLO}$ | VHV undervoltage lockout | VHV Input falling | 3.6 | 4 | | V |
| | | VHV Input rising | | 4 | 4.3 | |
| $V_{3P3UVLO}$ | V3P3 undervoltage lockout | V3P3 Input falling | 1.8 | 2.25 | | V |
| | | V3P3 Input rising | | 2.25 | 2.5 | |
| $V_{FAULTZVAL}$ | V3P3 voltage for valid FAULTZ | EN = 1 | 1.8 | | | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Shutdown temperature | | 110 | 120 | 130 | °C |
| $T_{SDHYST}$ | Shutdown hysteresis | | | 10 | | °C |
| **CURRENT LIMIT** | | | | | | |
| $I_{LIMHV}$ | VHV switch current limit state S0 or S3 | $R_{SET\_S0,3}$ = 402 kΩ(1) | 80 | 100 | 120 | mA |
| | | $R_{SET\_S0,3}$ = 80.6 kΩ(1) | 446 | 496 | 546 | |
| | | $R_{SET\_S0,3}$ = 26.7 kΩ(1) | 1423 | 1498 | 1573 | |
| $I_{LIMVHVMAX}$ | Maximum VHV switch current limit | $R_{SET\_S0,3}$ = 0 Ω | 1.8 | 2.4 | 3.1 | A |
| $I_{LIM3P3}$ | V3P3 switch current limit | $R_{SET\_V3P3}$ = 402 kΩ(1) | 80 | 100 | 120 | mA |
| | | $R_{SET\_V3P3}$ = 80.6 kΩ(1) | 446 | 496 | 546 | |
| | | $R_{SET\_V3P3}$ = 26.7 kΩ(1) | 1423 | 1498 | 1573 | |
| $I_{LIM3P3MAX}$ | Maximum V3P3 switch current limit | $R_{SET\_V3P3}$ = 0Ω | 1.8 | 2.4 | 3.1 | A |
| $I_{REV3P3}$ | V3P3 switch reverse current limit | | 10 | 40 | 85 | mA |
| $T_{V3P3RC}$ | V3P3 switch reverse current response time | $V_{OUT}$ = $V_{3P3}$→$V_{3P3}$ + 20 mV | | | 100 | µs |
| $T_{VHVSC}$ | VHV switch short circuit response time | $C_{OUT}$ ≤ 20 pF | | 8 | | µs |
| $T_{V3P3SC}$ | V3P3 switch short circuit response time | $C_{OUT}$ ≤ 20 pF | | 8 | | µs |

(1) Equation 1 is used to calculate the required resistance for a given minimum $I_{LIM}$. The nearest 1% resistance is chosen and the corresponding $I_{LIM}$ variance is shown.

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## Electrical Characteristics (continued)

Unless otherwise noted the specification applies over the $V_{DD}$ range and operating junction temp –40°C ≤ $T_J$ ≤ 85°C. Typical values are for $V_{3P3}$ = 3.3 V, $V_{HV}$ = 15 V, and $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TRANSITION DELAYS** | | | | | | |
| $T_{3P3OFF}$ | VHV to V3P3 OFF-time | $C_{OUT}$ = 1.1 µF, EN = 1, HV_EN = 1→0 | | | 6 | ms |
| $T_{0\text{-}3.3V}$ | 0-V to 3.3-V ramp time | $C_{OUT}$ ≤ 20 pF | | | 6 | ms |
| $T_{3.3V\text{-}VHV}$ | 3.3-V to VHV ramp time | $C_{OUT}$ ≤ 20 pF | | | 6 | ms |
| $T_{VHV\text{-}3.3V}$ | VHV to 3.3-V ramp time | $C_{OUT}$ ≤ 20 pF | | | 23 | ms |
| $T_{LIM}$ | Overcurrent response time | $C_{OUT}$ ≤ 20 pF, $I_{OUT}$ = 6 A | | | 0.5 | ms |

## 6.6 Dissipation Ratings

| PACKAGE | POWER RATING(1) $T_A$ = 25°C | POWER RATING(1) $T_A$ = 70°C | DERATING FACTOR ABOVE(2) $T_A$ = 25°C |
|---|---|---|---|
| RGP | 2.16 W | 1.02 W | 25.4 mW/°C |

(1) Simulated with high-K board
(2) Maximum power dissipation is a function of $T_{J(max)}$, $\theta_{JA}$ and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$.


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# 7 Detailed Description

## 7.1 Overview

TPS22981 is a power mux designed for Thunderbolt™ and Thunderbolt II™ applications (based on the Mini DisplayPort connector). Thunderbolt and Thunderbolt II provide options for different voltage levels to be supplied to an external Thunderbolt cable, and on to a device or host connected on the far end of that cable. Thunderbolt and Thunderbolt II initiate operation with a nominal 3.3-V voltage (3-V to 3.6-V range is supported by TPS22981), but can be configured through the interface protocol to enable a high-voltage mode (TPS22981 supports the range of 4.5 V to 19.8 V). In operation, transition from the 3.3-V mode to the high-voltage mode requires that system brownout not occur. The TPS22981 achieves this by enabling the high-voltage path (when a high-voltage input is available and HV_EN is asserted) and monitoring for reverse current though the low-voltage switch back to V3P3. When reverse current is detected, the low-voltage path is disabled. Similarly, when switching from high voltage back to low voltage, it is normally undesirable for the system output voltage to brownout. TPS22981 avoids brownout by breaking the high-voltage connection and discharging the output until it reaches approximately 3.3 V, at which point the low-voltage path is enabled to avoid excessive droop of the output voltage. However, if the output voltage (on the OUT pins) is loaded, the output voltage may transition to 0 V before returning to 3.3 V (see *Transition Delays*).

TPS22981 also provides resistor-controlled current limiting, undervoltage lockout (UVLO), and thermal protection. The high-voltage path on TPS22981 may be current limited to two independently controlled current-limiting levels, with the current-limiting level selected through the S0 input pin. A system host processor may be alerted to fault conditions with the FAULTZ pin (see Table 3).

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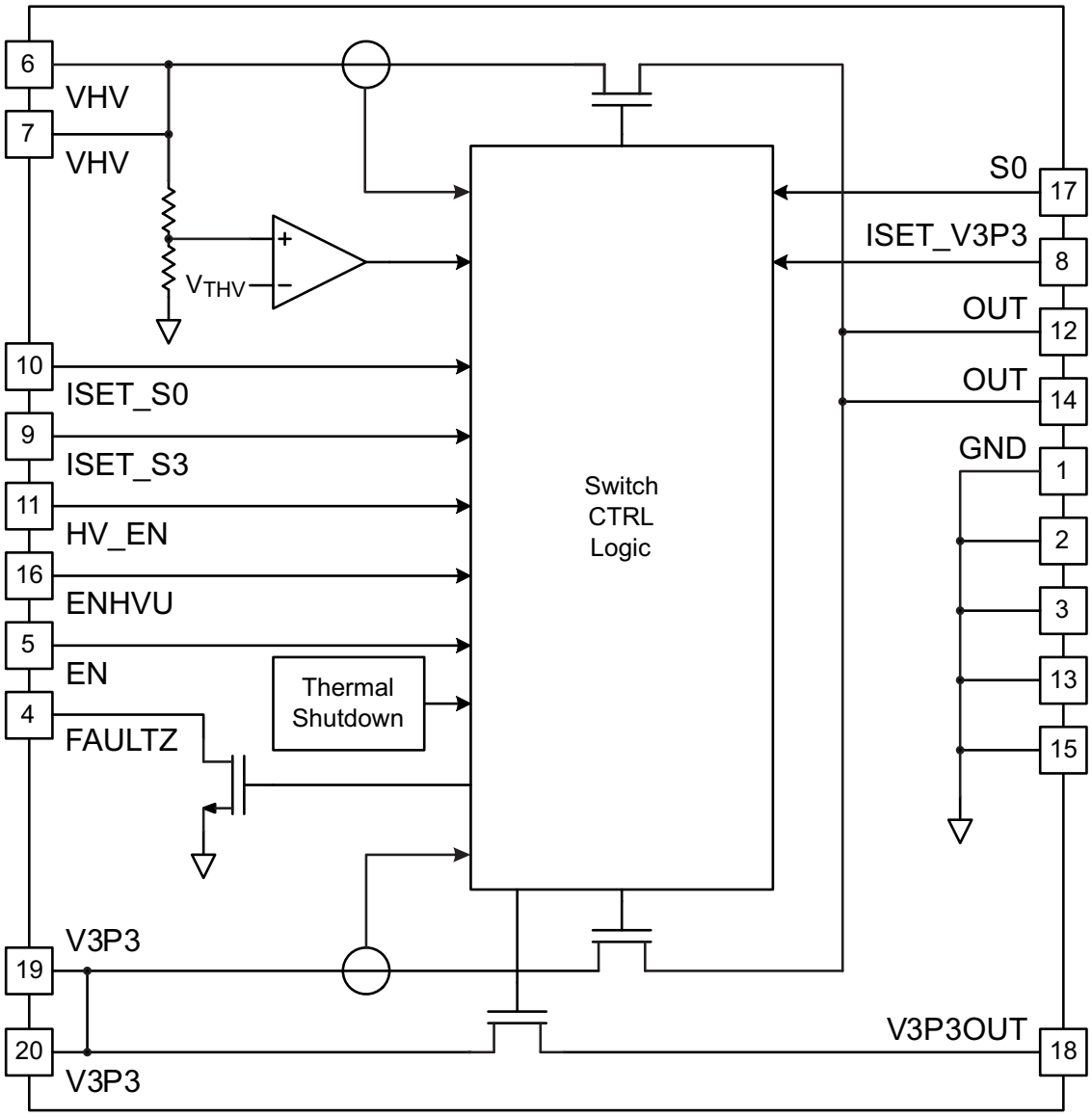
## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Current Limit

Figure 1 shows a simplified view of the TPS22981 current limit function. Both the high-voltage supply current limit and the V3P3 supply current limit are adjustable by external resistors.

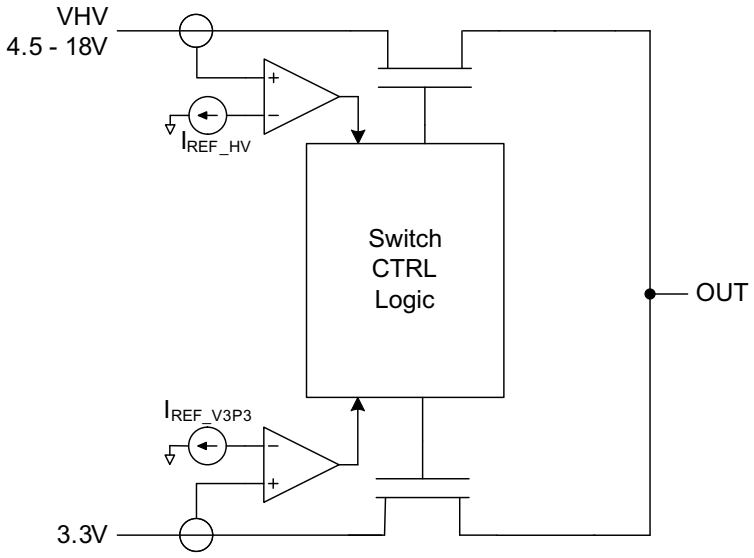


**Figure 1. Simplified Current Limit Diagram**

The current $I_{REF\_HV}$ and $I_{REF\_V3P3}$ that set the current limit threshold are set with three external resistors as shown in Figure 2. When the TPS22981 is passing the V3P3 voltage, the current limit is set by $R_{SET\_V3P3}$. The VHV path has two modes that allow setting two different current limits. The S0 pin determines which current limit is used. When S0 is asserted high, $R_{SET\_S0}$ sets the current limit. When S0 is low, $R_{SET\_S3}$ sets the current limit. This allows the system to have two separate VHV current limits for different modes such as active and sleep.

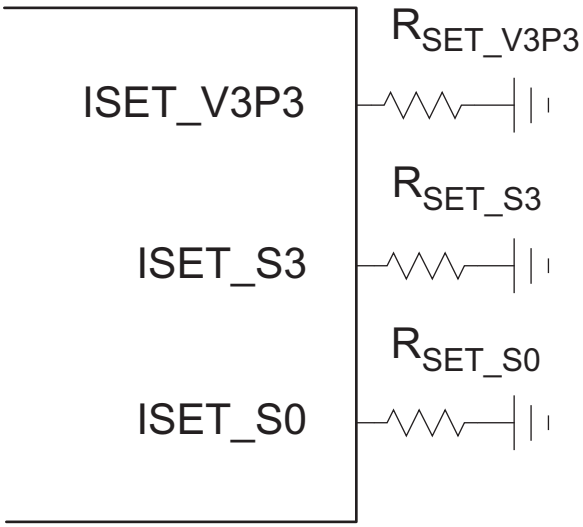


**Figure 2. External $R_{SET}$ Resistance to Set Current Limits**

## Feature Description (continued)

### 7.3.2 Current Limit Threshold

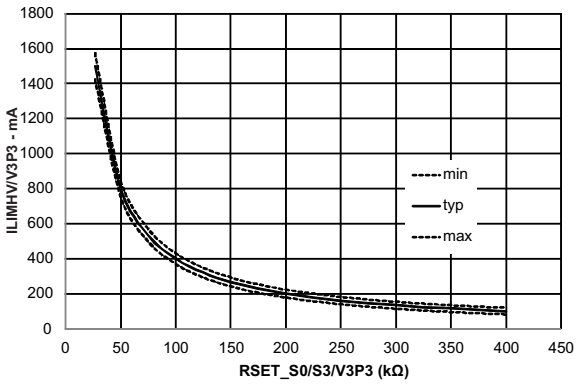


**Figure 3. $I_{LIM}$ vs $R_{SET}$ for VHV and V3P3**

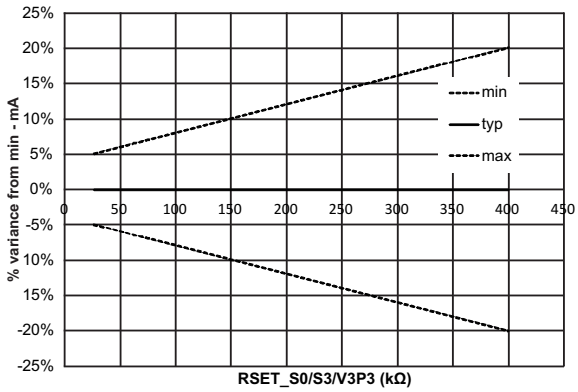


**Figure 4. % Variance from Minimum $I_{LIM}$ vs $R_{SET}$**

Figure 3 shows the minimum, typical, and maximum current limit for either supply versus its corresponding $R_{SET}$ value. Equation 1 is used to determine the RSET needed to set a typical $I_{LIM}$ for a given supply and mode. Figure 4 shows the percent variation from the typical $I_{LIM}$ value to the minimum and maximum $I_{LIM}$ values.

$$R_{SET} = \frac{40\ k\Omega \times Amps}{I_{LIMTYP}}$$

where

- $R_{SET}$ = external resistor used to set the current limit for V3P3, VHV (S0), or VHV (S3)
- $I_{LIMTYP}$ = typical current limit for V3P3, VHV (S0), or VHV (S3) set by the external $R_{SET}$ resistor. (1)

Each resistor is placed between the corresponding ISET pin and GND, as shown in Figure 2, providing a minimum current limit between 100mA and 1.5A. For a given $R_{SET}$ the minimum current limit and the maximum current limit are determined by Equation 2 and Equation 3.

$$I_{LIMMIN} = \frac{38429}{R_{SET}} - 0.0161\ A \quad (2)$$

$$I_{LIMMAX} = \frac{41571}{R_{SET}} + 0.0161\ A \quad (3)$$

### 7.3.3 Maximum Current Limit Threshold

The TPS22981 has a maximum current limit $I_{LIMVHVMAX}$ and $I_{LIM3P3MAX}$. This prevents excessive current in the case of an ISET pin being shorted to ground.

### 7.3.4 Transition Delays

Output transitions of the TPS22981 voltages are shown in Figure 5. When the device transitions from $V_{HV}$ to $V_{3P3}$ at the output, the power switches both turn off until the output falls to near the $V_{3P3}$ voltage. During this time, a discharge current of $I_{DIS}$ pulls OUT down. If a load is also pulling current from OUT, the output will drop to near 0 V due to the switch OFF-time of $T_{3P3OFF}$.


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## Feature Description (continued)

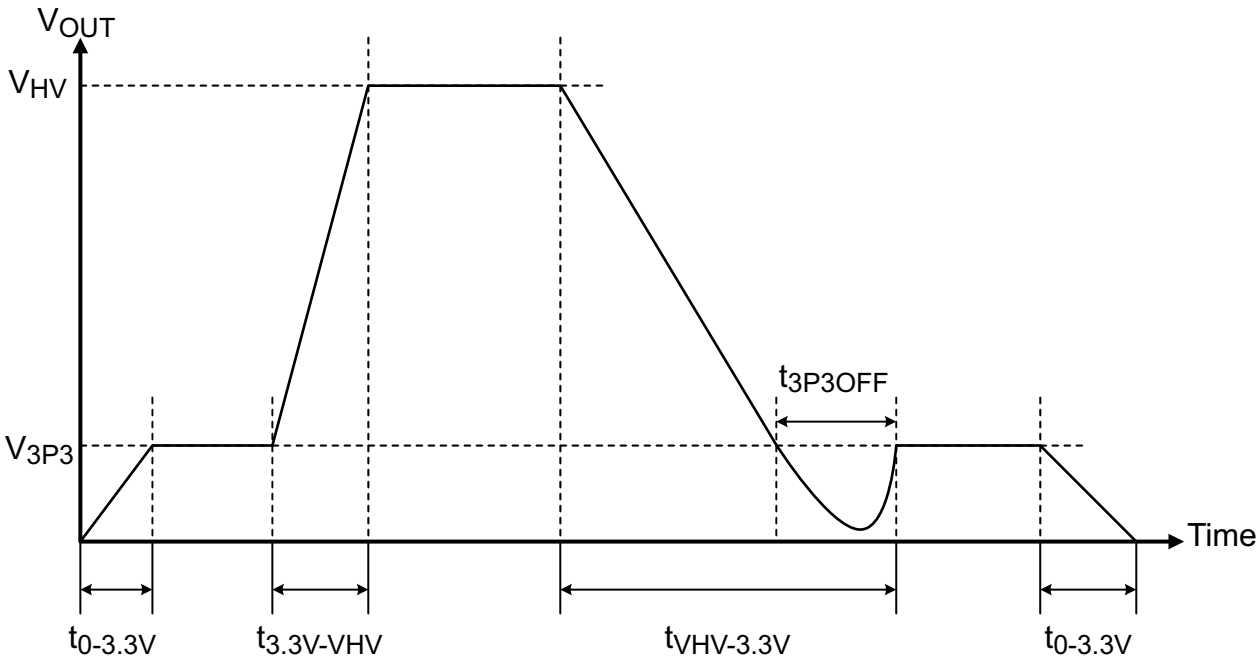


**Figure 5. Output Voltage Transitions (Timing Transitions are 10% to > 90%)**

### 7.3.5 Digital Control Signals

The voltage at OUT is controlled by two input digital logic signals, EN and HV_EN. HV_EN controls the state of the VHV switch and EN controls the state of V3P3 switch. Table 1 lists the possible output states given the conditions of the digital logic signals and the device is not in UVLO. See Table 2 for a more complete description including both UVLO conditions.

**Table 1. Output State of OUT Given the States EN and HV_EN**

| EN | HV_EN | OUT |
|---|---|---|
| 0 | 0 | OPEN |
| 0 | 1 | OPEN |
| 1 | 0 | V3P3 |
| 1 | 1 | VHV |

Figure 6 shows possible combinations of EN and HV_EN controlling OUT of the TPS22981.

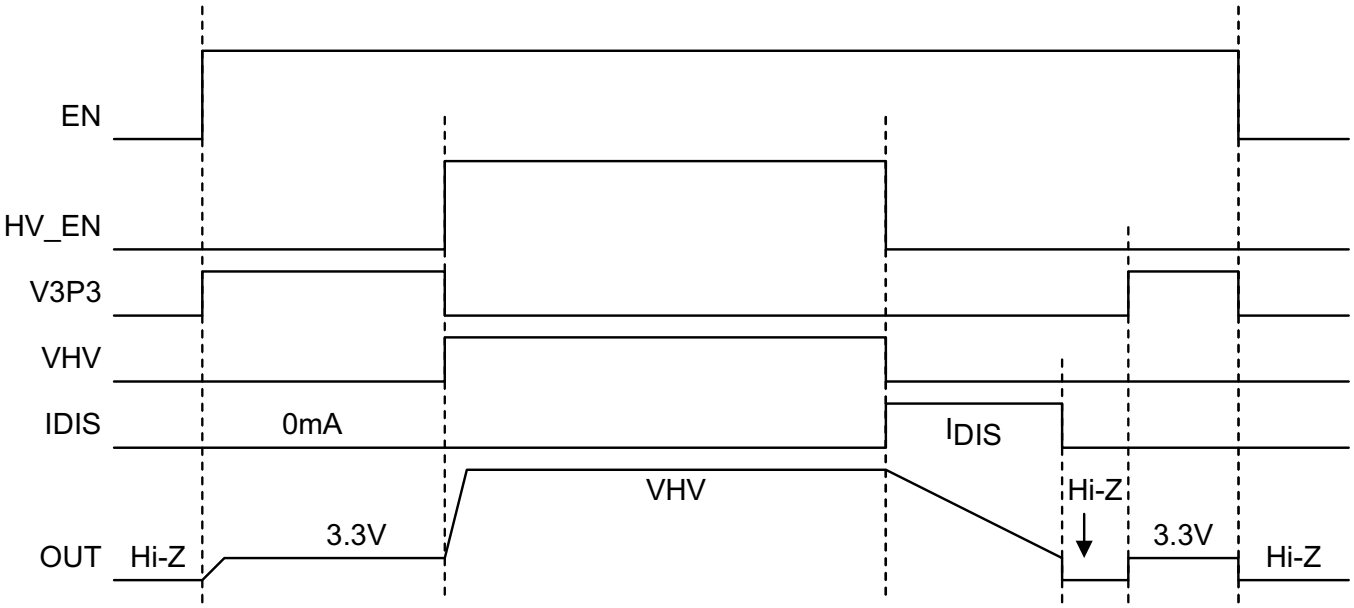


**Figure 6. Logic Waveforms Displaying the Transition Between VHV and V3P3**

### 7.3.6 Overcurrent Limit and Short-Circuit Protection

When the load at OUT attempts to draw more current than the limit set by the external $R_{SET}$ resistors for the V3P3 switch and VHV switch (for both S0 and S3 modes), the device will operate in a constant-current mode while lowering the output voltage. Figure 7 shows the delay, $t_{LIM}$, which occurs from the instance an overcurrent fault is detected until the output current is lowered to $I_{LIMHV}$ tolerances for VHV or $I_{LIM3V3}$ tolerances for V3P3 shown in Figure 3. Figure 8 shows the response time versus a resistance shorted across the output.

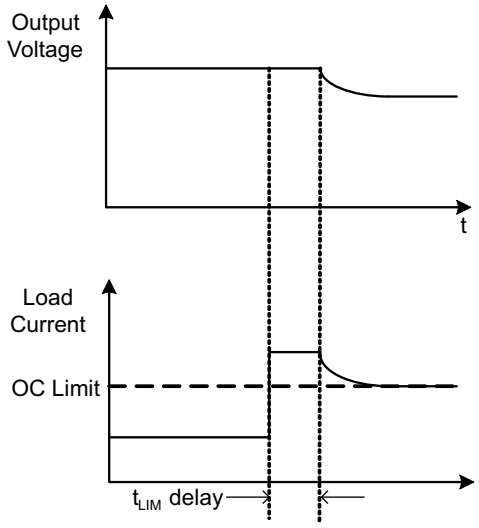


**Figure 7. Overcurrent Output Response**


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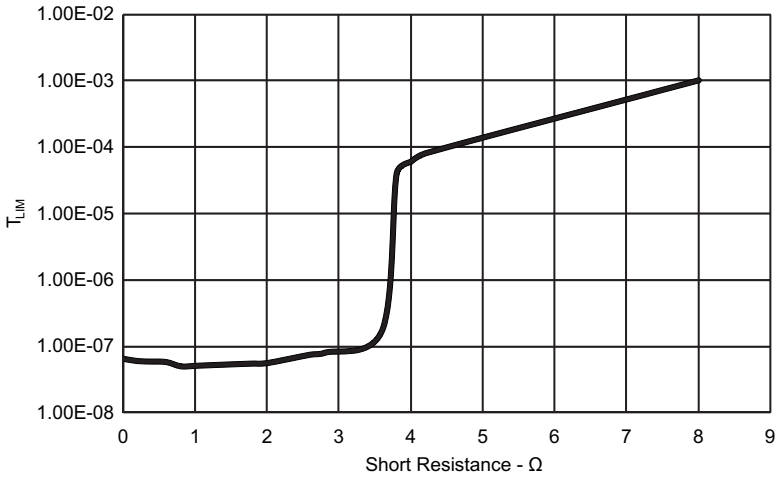


**Figure 8. Overcurrent Response Time vs Short Resistance**

All short-circuit conditions are treated as overcurrent conditions. In the event of a short circuit, the device will limit the output current to the corresponding $R_{SET}$ value and continue to do so until thermal shutdown is encountered or the short-circuit condition is removed.

### 7.3.7 Reverse Current Protection

Reverse current protection for the V3P3 supply to OUT triggers at $I_{REV3P3}$ causing the V3P3 supply switch to open. When the HV_EN signal is not asserted and reverse current protection is triggered, a discharge current source is turned on to bring the output voltage to near the V3P3 voltage.

### 7.3.8 Reverse Current Blocking

The VHV switch blocks reverse current flow from OUT to VHV when the switch is off.

### 7.3.9 Thermal Shutdown

The device enters thermal shutdown when junction temperature reaches $T_{SD}$. The device will resume previous state on power up once the junction temperature has dropped by 10°C. Connect thermal vias to the exposed GND pad underneath the device package for improved thermal diffusion.

## 7.4 Device Functional Modes

### 7.4.1 UVLO and Enable

When ENHVU is low, the TPS22981 is enabled by the logical AND of the EN input, the V3P3 UVLO, and the Thermal Shutdown. When the V3P3 UVLO threshold has been crossed, the device is not in thermal shutdown, and the EN input is high, the device will enable. When the V3P3 UVLO triggers, regardless of the states of any digital logic controls, the device will open all switches.

ENHVU adds the VHV UVLO to the logical decision enabling the device. When ENHVU is high, the TPS22981 is enabled by the logical AND of the EN input, the V3P3 UVLO, the VHV UVLO, and the thermal shutdown. When both UVLO thresholds have been crossed, the device is not in thermal shutdown, and the EN input is high, the device will enable. When either UVLO triggers, regardless of the states of any digital logic controls, the device will open all switches. Table 2 shows the pin and voltage configurations for enabling the device.

**NOTE**

A 1 for the UVLO columns means the device is in a UVLO condition. A PD indicates a pulldown resistance of $R_{OUTDIS}$ to GND.

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**Table 2. Device Enable Control (When in an Undervoltage Condition, UVLO = 1)**

| EN | ENHVU | HV_EN | V3P3 UVLO | VHV UVLO | OUT |
|---|---|---|---|---|---|
| 0 | X | X | X | X | PD |
| 1 | X | X | 1 | X | PD |
| 1 | 1 | X | 0 | X | OPEN |
| 1 | 1 | X | 1 | X | PD |
| 1 | 0 | 0 | 0 | X | V3P3 |
| 1 | 1 | 0 | 0 | 0 | V3P3 |
| 1 | X | 1 | 0 | 0 | VHV |
| 1 | 0 | 1 | 0 | 1 | V3P3 |

### 7.4.2 FAULTZ Output

The TPS22981 has an open-drain FAULTZ output. When the device is in a fault condition, the FAULTZ output will pull low. Connect FAULTZ through a pullup resistance to V3P3. A Fault occurs during any of the following conditions.

- EN = 1 and V3P3 is in UVLO (device enabled and V3P3 is in an undervoltage condition)
- EN = 1 and in thermal shutdown condition
- EN = 1, HV_EN = 1, and VHV is in UVLO (device enabled, high voltage enabled, and VHV is in an undervoltage condition)

Table 3 shows these conditions and the resulting FAULTZ output. Note, when V3P3 is below the UVLO threshold, FAULTZ will be 0 when EN=1 or 1 when EN=0. However, when V3P3 falls below $V_{FAULTZVAL}$, the FAULTZ output is unknown.

**Table 3. FAULTZ Output Conditions (when in an undervoltage condition, UVLO = 1)**

| EN | HV_EN | Thermal Shutdown | V3P3 UVLO | VHV UVLO | FAULTZ (Active Low) |
|---|---|---|---|---|---|
| 0 | X | X | X | X | 1 |
| 1 | X | X | 1 | X | 0 |
| 1 | X | Yes | 0 | X | 0 |
| 1 | 0 | No | 0 | 1 | 1 |
| 1 | 1 | No | 0 | 1 | 0 |
| 1 | X | No | 0 | 0 | 1 |

TI recommends that the pullup resistance on FAULTZ be 100 kΩ and must be greater than or equal to 30 kΩ.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Input Inductive Bounce

When a significant inductance is seen at the VHV input, suddenly turning off large current through the device may produce a large enough inductive voltage bounce on the VHV pin to exceed the maximum safe operating condition and damage the TPS22981. To prevent this, reduce any inductance at the VHV input.

## 8.2 Typical Application

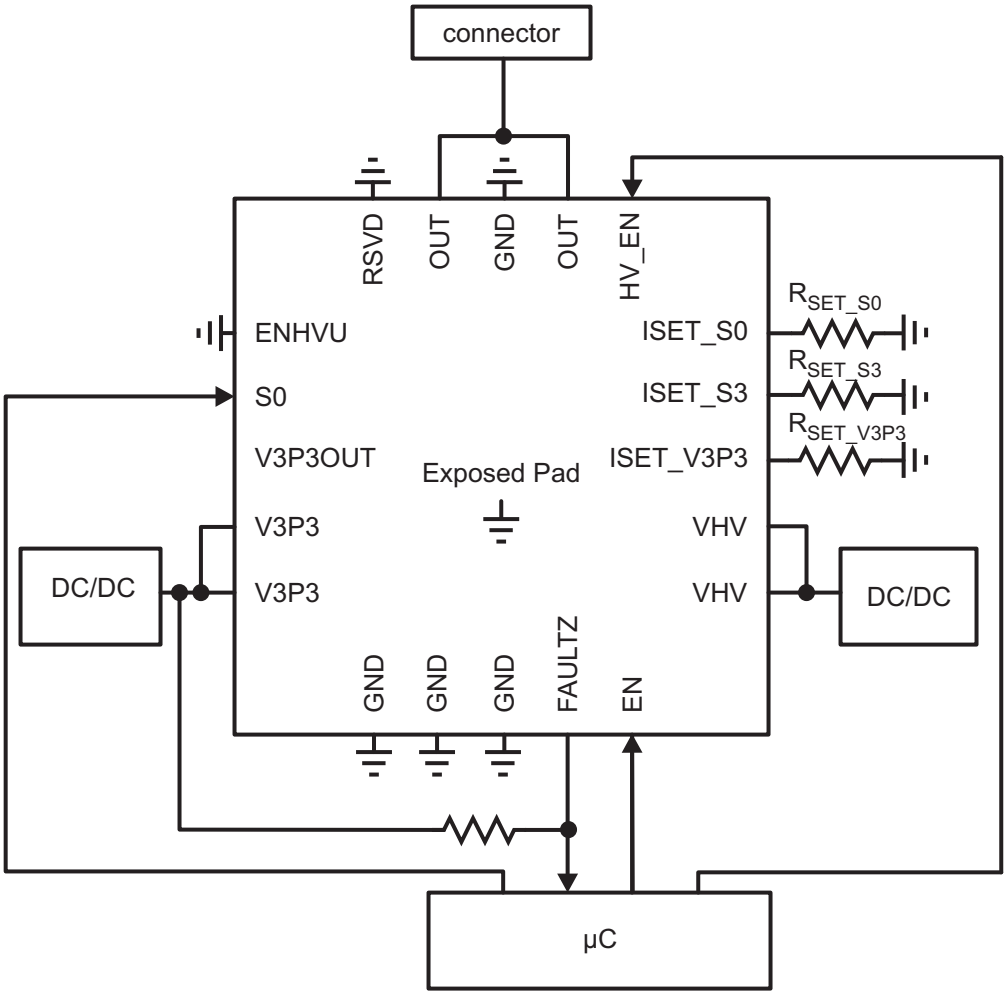


**Figure 9. Typical Application Schematic**

## Typical Application (continued)

### 8.2.1 Design Requirements

As the TPS22981 switches high-current levels, it is essential that all parallel output, power, and ground pins be connected. For example, ground connections must be provided on all ground pins including pins 1, 2, 3, 13, 15, and EP (the exposed package pad); both OUT pins (pins 12 and 14) must be connected; and so forth. RSET_S0, RSET_S3, and RSET_V3P3 must be determined using Equation 1. Unused inputs may not be left floating and should be connected to either ground or V3P3 depending on desired behavior.

### 8.2.2 Detailed Design Procedure

Design with TPS22981 is recommended as follows:

- Determine suitable current limits for the low-voltage and high-voltage output levels (output provided on the OUT pin). If S0 is being used, determine both high-voltage output levels and current-limiting values.
- Determine values for the resistors to be applied to pins ISET_V3P3, ISET_S3, and ISET_S0 using Equation 1 and the desired current limits determined above.
- If the FAULTZ output is being used, place a minimum 30-kΩ resistor (100-kΩ recommended) between FAULTZ and the V3P3.

## 9 Power Supply Recommendations

Power supply current capability should be suitable with respect to the maximum current limit levels selected (and programmed with pins ISET_V3P3, ISET_S3, and ISET_S0).

VHV and V3P3 must be properly decoupled. A minimum 0.1-µF capacitor to ground is recommended as close to the V3P3 pin as possible. VHV should be suitably decoupled based on the supply compliance and maximum current levels anticipated. Inductance in the VHV line can result in overvoltage situations on the VHV pin when loads are disconnected. Refer to the *Input Inductive Bounce* section and ensure that inductance levels, capacitive decoupling, and current switching levels are designed to keep power supply voltage levels within recommended operating conditions at all times.


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# 10 Layout

## 10.1 Layout Guidelines

- Ensure decoupling capacitors on the OUT, V3P3, and V3P3OUT pins are tied directly to a solid ground plane or ground connection, and are placed as close to each respective pin as possible.
- Route the VHV input to minimize total inductance between the source for this power supply and the VHV pin. See *Input Inductive Bounce* regarding inductance in the VHV input potentially causing damaging voltage levels if large currents are suddenly turned off in the course of system operation.
- Layout trace width should be checked to ensure adequate current carrying ability and suitable resistive voltage drops in view of peak current levels.

Figure 10 shows the schematic used for the layout provided in the *Layout Example* section.

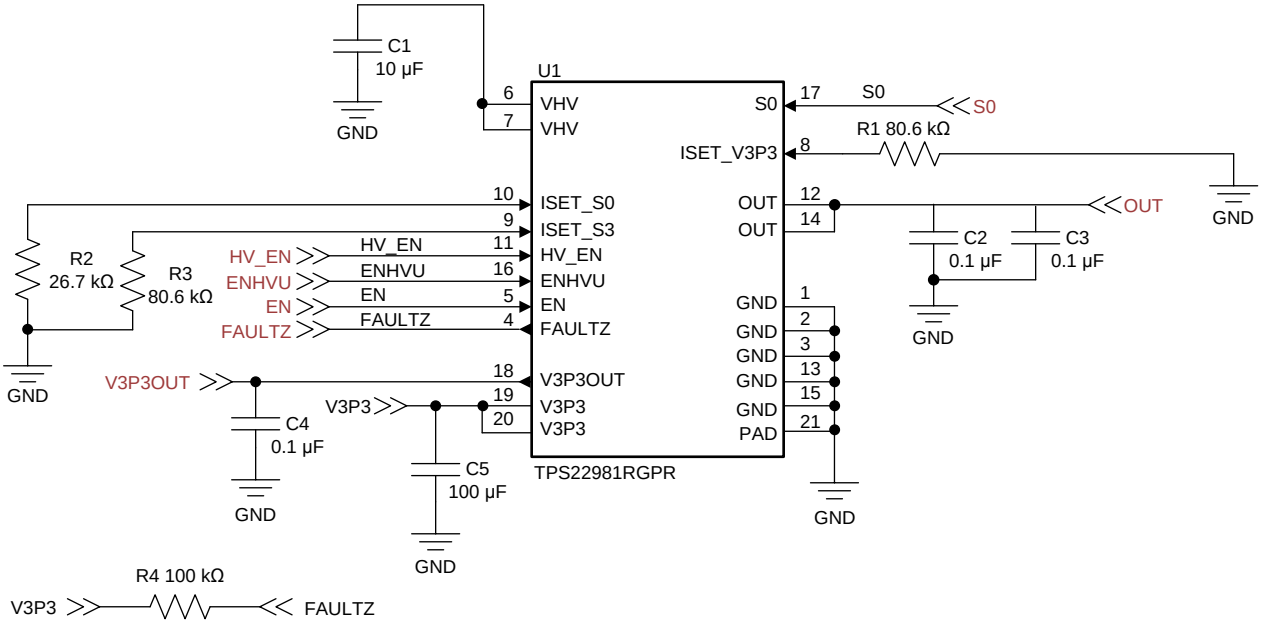


**Figure 10. Layout Example Schematic**

The TPS22981 can be placed on the same layer as its components. The layout can be a smaller area when the bottom is used for component placement. In this design example, the components and the TPS22981 are placed on the top layer. Figure 11 and Figure 12 show the suggested placement of the components.

For the nets V3P3, OUT, and VHV, TI recommends to use Thunderbolt three 8-mil or 16-mil vias when moving from layer to layer. A 40-mil trace or pour will allow roughly 2 A to pass current carrying capability with 0.5-oz. copper. Two 8-mil or 16-mil vias and 12-mil traces are sufficient for V3P3OUT. All of the other signals can be routed using a 10-mil trace with an 8-mil or 16-mil via. Figure 13 and Figure 14 show the suggested power and signal routing with and without a GND pour on the top layer. TI recommends that the capacitors and the GND pad on the TPS22981 are connected on the same plane.

The remaining signals can be routed through the bottom layer or other internal layer. Figure 15 shows the bottom routing.

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## 10.2 Layout Example

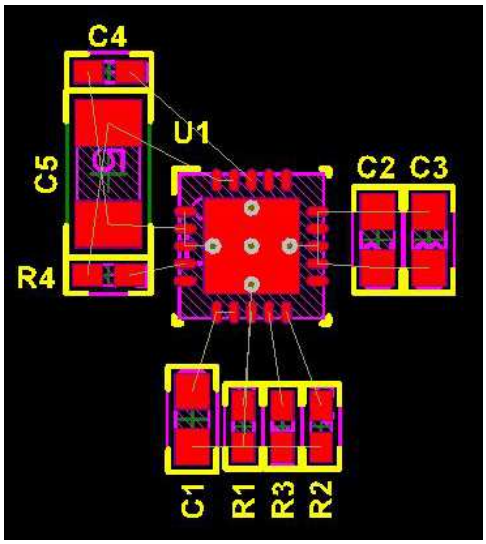


**Figure 11. Top Layer 2D View**

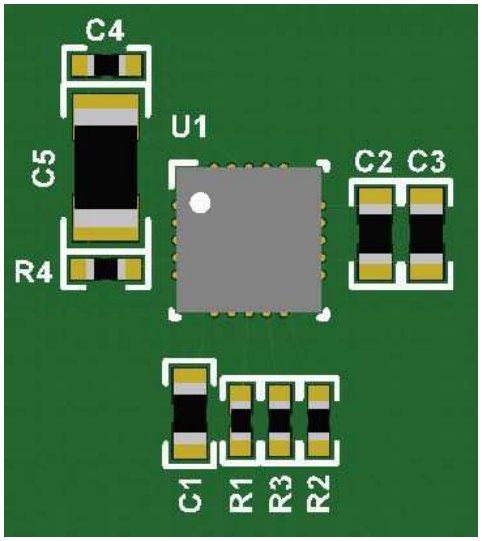


**Figure 12. Top Layer 3D View**

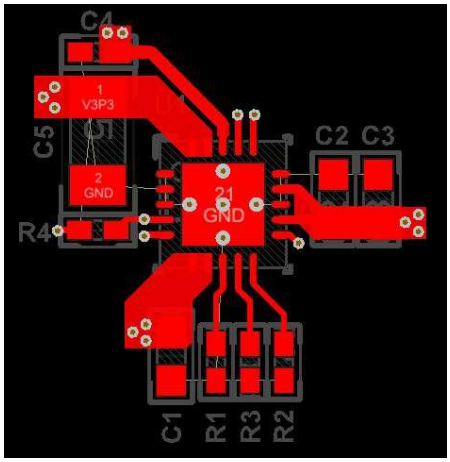


**Figure 13. Power/Signal Routing Without GND Pour**

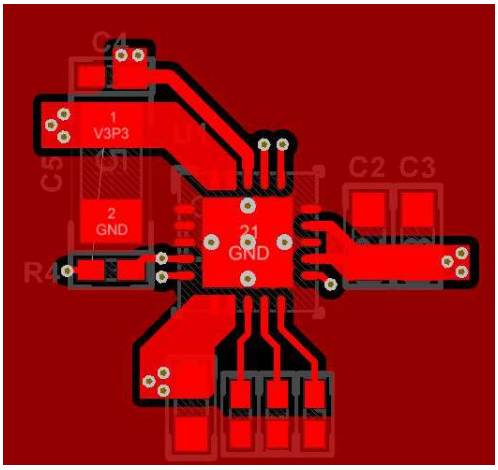


**Figure 14. Power/Signal Routing With GND Pour**

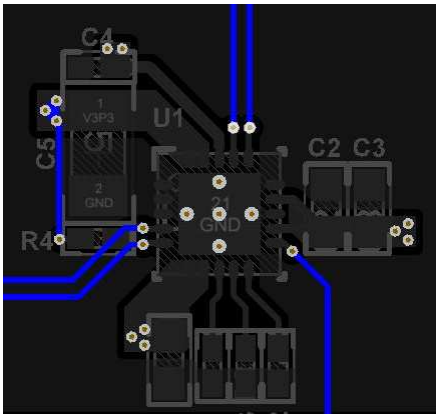


**Figure 15. Bottom Layer Routing**


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# 11 Device and Documentation Support

## 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.2 Trademarks

E2E is a trademark of Texas Instruments.
Thunderbolt, Thunderbolt II are trademarks of Intel Corporation.
All other trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22981RGPR | ACTIVE | QFN | RGP | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS22981 | Samples |
| TPS22981RGPT | ACTIVE | QFN | RGP | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS22981 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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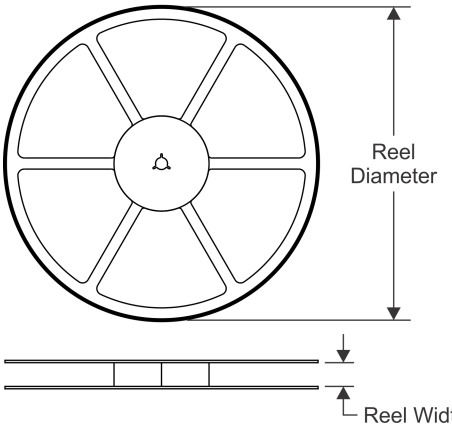
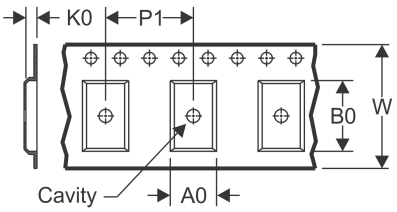
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

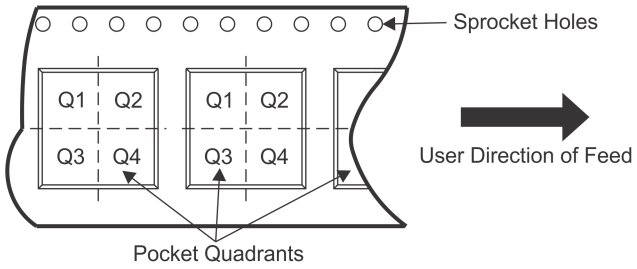



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

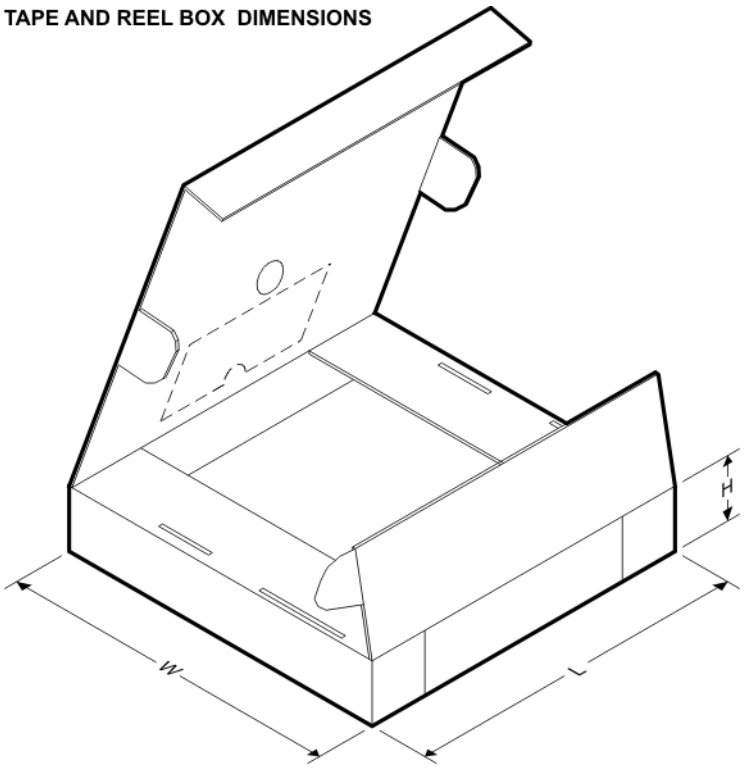
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22981RGPR | QFN | RGP | 20 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS22981RGPT | QFN | RGP | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

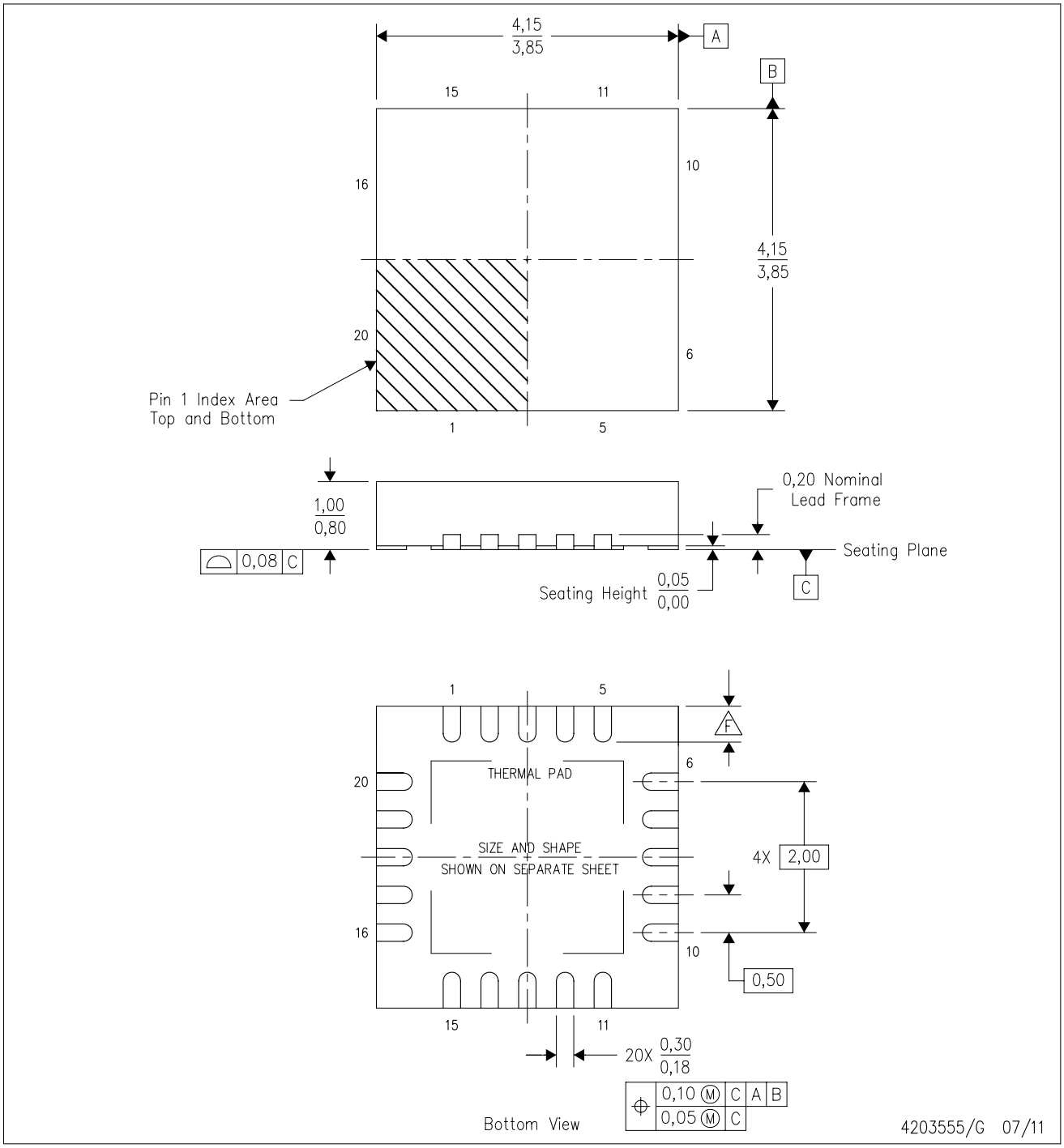
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS22981RGPR | QFN | RGP | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS22981RGPT | QFN | RGP | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

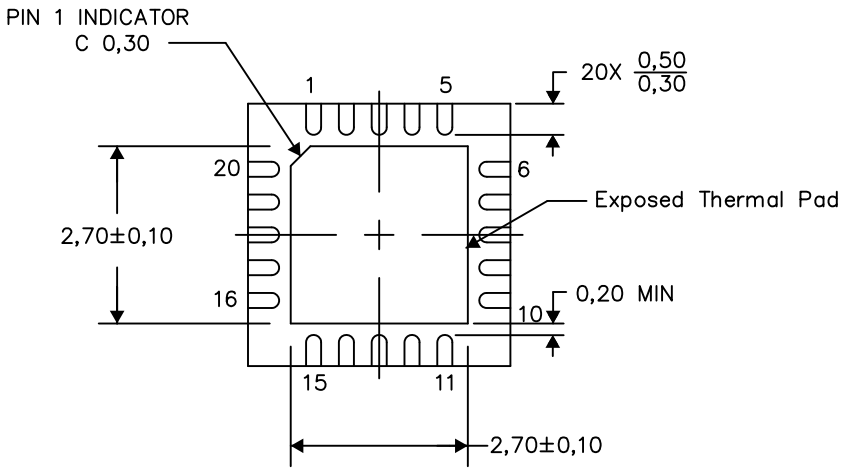
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



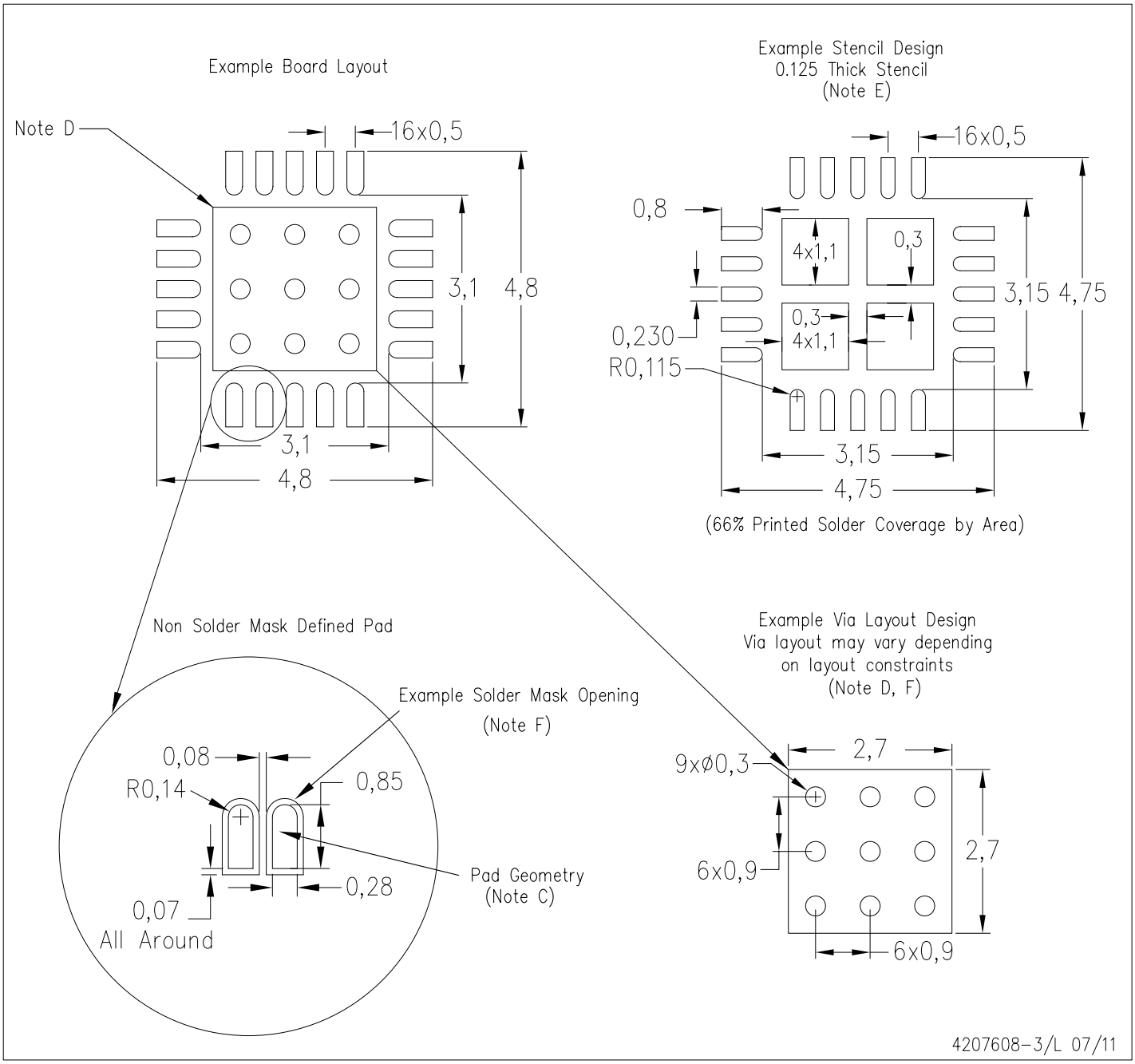

Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

# RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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