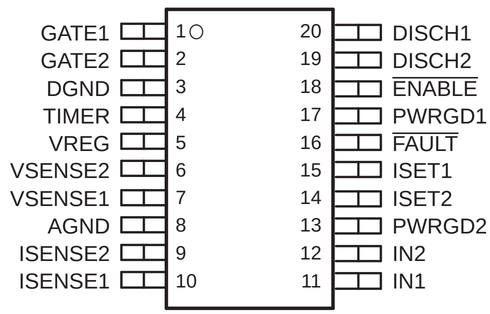
DUAL HOT-SWAP POWER CONTROLLERS WITH INDEPENDENT CIRCUIT BREAKER AND POWER-GOOD REPORTING

Check for Samples: TPS2300, TPS2301

FEATURES

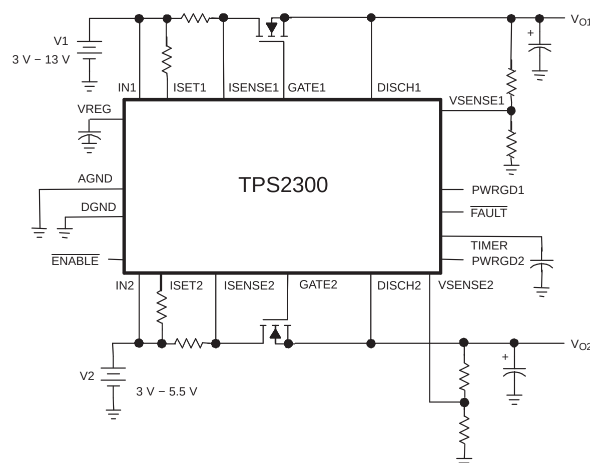
- **Dual-Channel High-Side MOSFET Drivers**
- **IN1: 3 V to 13 V; IN2: 3 V to 5.5 V**
- **Output dV/dt Control Limits Inrush Current**
- **Circuit-Breaker With Programmable Overcurrent Threshold and Transient Timer**
- **Power-Good Reporting With Transient Filter**
- **CMOS- and TTL-Compatible Enable Input**
- **Low, 5-μA Standby Supply Current (Max)**
- **Available in 20-Pin TSSOP Package**
- **40°C to 85°C Ambient Temperature Range**
- **Electrostatic Discharge Protection**

PW PACKAGE
(TOP VIEW)



NOTE: Terminal 18 is active high on TPS2301.

typical application



APPLICATIONS

- **Hot-Swap/Plug/Dock Power Management**
- **Hot-Plug PCI, Device Bay**
- **Electronic Circuit Breaker**

DESCRIPTION

The TPS2300 and TPS2301 are dual-channel hot-swap controllers that use external N-channel MOSFETs as high-side switches in power applications. Features of these devices, such as overcurrent protection (OCP), inrush current control, output-power status reporting, and the ability to discriminate between load transients and faults, are critical requirements for hot-swap applications.

The TPS2300/01 devices incorporate undervoltage lockout (UVLO) and power-good (PG) reporting to ensure the device is off at start-up and confirm the status of the output voltage rails during operation. Each internal charge pump, capable of driving multiple MOSFETs, provides enough gate-drive voltage to fully enhance the N-channel MOSFETs. The charge pumps control both the rise times and fall times (dv/dt) of the MOSFETs, reducing power transients during power up/down. The circuit-breaker functionality combines the ability to sense overcurrent conditions with a timer function; this allows designs such as DSPs, that may have high peak currents during power-state transitions, to disregard transients for a programmable period.

Table 1. AVAILABLE OPTIONS

T_A	HOT-SWAP CONTROLLER DESCRIPTION	PIN COUNT	TSSOP PACKAGES (PW, PWR)[(1)]	
			$\overline{\text{ENABLE}}$	ENABLE
40°C to 85°C	Dual-channel with independent OCP and adjustable PG	20	TPS2300IPW	TPS2301IPW
	Dual-channel with interdependent OCP and adjustable PG	20	TPS2310IPW	TPS2311IPW
	Dual-channel with independent OCP	16	TPS2320IPW	TPS2321IPW
	Single-channel with OCP and adjustable PG	14	TPS2330IPW	TPS2331IPW

(1) The packages are available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TPS2301IPWR).

FUNCTIONAL BLOCK DIAGRAM

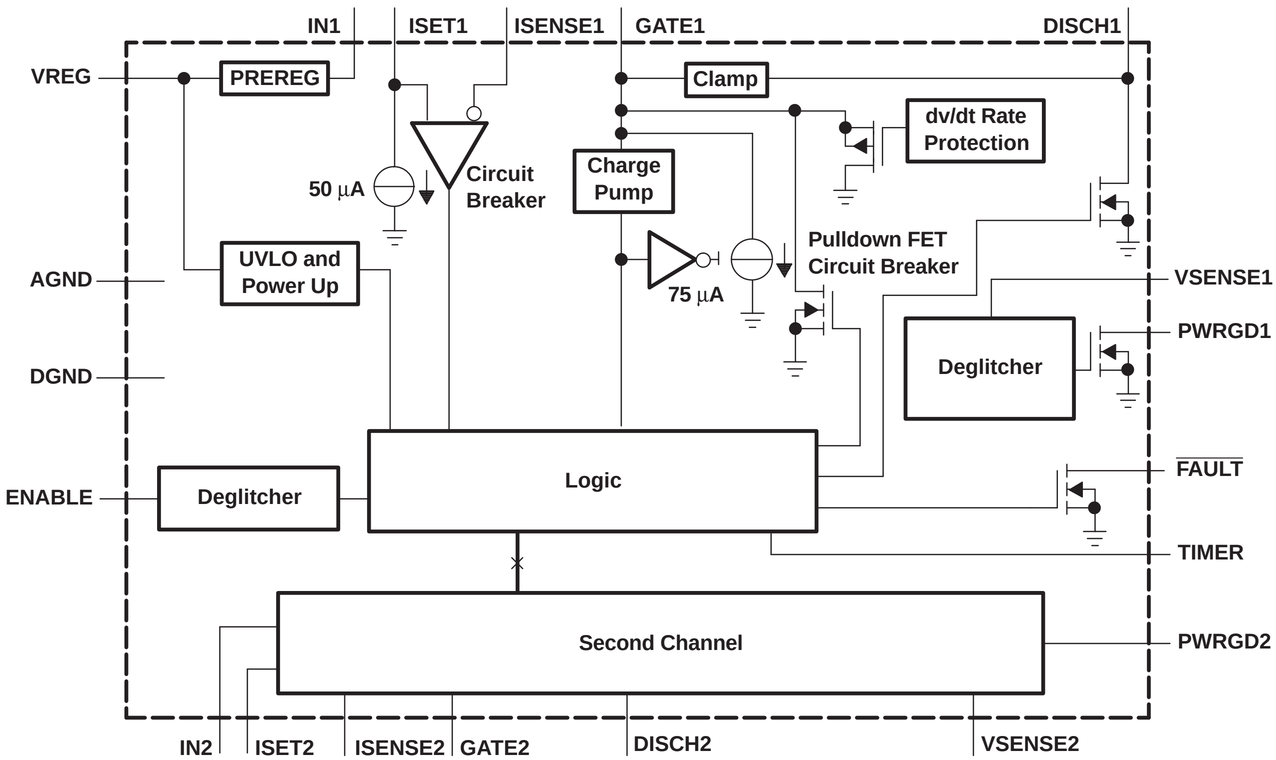


Table 2. Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	8	I	Analog ground, connects to DGND as close as possible
DGND	3	I	Digital ground
DISCH1	20	O	Discharge transistor 1
DISCH2	19	O	Discharge transistor 2
$\overline{\text{ENABLE}}$/ ENABLE	18	I	Active low (TPS2300) or active high enable (TPS2301)
$\overline{\text{FAULT}}$	16	O	Overcurrent fault, open-drain output
GATE1	1	O	Connects to gate of channel 1 high-side MOSFET
GATE2	2	O	Connects to gate of channel 2 high-side MOSFET
IN1	11	I	Input voltage for channel 1
IN2	12	I	Input voltage for channel 2
ISENSE1	10	I	Current-sense input channel 1
ISENSE2	9	I	Current-sense input channel 2
ISET1	15	I	Adjusts circuit-breaker threshold with resistor connected to IN1

Table 2. Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ISET2	14	I	Adjusts circuit-breaker threshold with resistor connected to IN2
PWRGD1	17	O	Open-drain output, asserted low when VSENSE1 voltage is less than reference.
PWRGD2	13	O	Open-drain output, asserted low when VSENSE2 voltage is less than reference.
TIMER	4	O	Adjusts circuit-breaker deglitch time
VREG	5	O	Connects to bypass capacitor, for stable operation
VSENSE1	7	I	Power-good sense input channel 1
VSENSE2	6	I	Power-good sense input channel 2

DETAILED DESCRIPTION

DISCH1, DISCH2 – DISCH1 and DISCH2 should be connected to the sources of the external N-channel MOSFET transistors connected to GATE1 and GATE2, respectively. These pins discharge the loads when the MOSFET transistors are disabled. They also serve as reference-voltage connections for internal gate voltage-clamp circuitry.

$\overline{\text{ENABLE}}$ or ENABLE – $\overline{\text{ENABLE}}$ for TPS2300 is active-low. ENABLE for TPS2301 is active-high. When the controller is enabled, both GATE1 and GATE2 voltages powers up to turn on the external MOSFETs. When the $\overline{\text{ENABLE}}$ pin is pulled high for TPS2300 or the ENABLE pin is pulled low for TPS2301 for more than 50 µs, the gate of the MOSFET is discharged at a controlled rate by a current source, and a transistor is enabled to discharge the output bulk capacitance. In addition, the device turns on the internal regulator PREREG (see VREG) when enabled and shuts down PREREG when disabled so that total supply current is less than 5 µA.

$\overline{\text{FAULT}}$ – $\overline{\text{FAULT}}$ is an open-drain overcurrent flag output. When an overcurrent condition in either channel is sustained long enough to charge TIMER to 0.5 V, the overcurrent channel latches off and pulls this pin low. The other channel runs normally if not in overcurrent. In order to turn the channel back on, either the enable pin has to be toggled or the input power has to be cycled.

GATE1, GATE2 – GATE1 and GATE2 connect to the gates of external N-channel MOSFET transistors. When the device is enabled, internal charge-pump circuitry pulls these pins up by sourcing approximately 15 µA to each. The turnon slew rates depend upon the capacitance present at the GATE1 and GATE2 terminals. If desired, the turnon slew rates can be further reduced by connecting capacitors between these pins and ground. These capacitors also reduce inrush current and protect the device from false overcurrent triggering during power up. The charge-pump circuitry generates gate-to-source voltages of 9 V–12 V across the external MOSFET transistors.

IN1, IN2 – IN1 and IN2 should be connected to the power sources driving the external N-channel MOSFET transistors connected to GATE1 and GATE2, respectively. The TPS2300/TPS2301 draws its operating current from IN1, and both channels remains disabled until the IN1 power supply has been established. The IN1 channel has been constructed to support 3-V, 5-V, or 12-V operation, while the IN2 channel has been constructed to support 3-V or 5-V operation

ISENSE1, ISENSE2, ISET1, ISET2 – ISENSE1 and ISENSE2, in combination with ISET1 and ISET2, implement overcurrent sensing for GATE1 and GATE2. ISET1 and ISET2 set the magnitude of the current that generates an overcurrent fault, through external resistors connected to ISET1 and ISET2. An internal current source draws 50 µA from ISET1 and ISET2. With a sense resistor from IN1 to ISENSE1 or from IN2 to ISENSE2, which is also connected to the drains of external MOSFETs, the voltage on the sense resistor reflects the load current. An overcurrent condition is assumed to exist if ISENSE1 is pulled below ISET1 or if ISENSE2 is pulled below ISET2. To ensure proper circuit breaker operation, $V_{I(ISENSE1)}$ and $V_{I(ISET1)}$ should never exceed $V_{I(IN1)}$. Similarly, $V_{I(ISENSE2)}$ and $V_{I(ISET2)}$ should never exceed $V_{I(IN2)}$.

PWRGD1, PWRGD2 – PWRGD1 and PWRGD2 signal the presence of undervoltage conditions on VSENSE1 and VSENSE2, respectively. These pins are open-drain outputs and are pulled low during an undervoltage condition. To minimize erroneous PWRGDx responses from transients on the voltage rail, the voltage sense circuit incorporates a 20-μs deglitch filter. When VSENSEx is lower than the reference voltage (about 1.23 V), PWRGDx is active low to indicate an undervoltage condition on the power-rail voltage. PWRGDx may not correctly report power conditions when the device is disabled, because there is no gate drive power for the PWRGD output transistor in the disable mode, or, in other words, PWRGD is floating. Therefore, PWRGD is pulled up to its pullup power supply rail in disable mode.

TIMER – A capacitor on TIMER sets the time during which the power switch can be in overcurrent before turning off. When the overcurrent protection circuits sense an excessive current, a current source is enabled which charges the capacitor on TIMER. Once the voltage on TIMER reaches approximately 0.5 V, the circuit-breaker latch is set and the power switch is latched off. Power must be recycled or the ENABLE pin must be toggled to restart the controller. In high-power or high-temperature applications, a minimum 50-pF capacitor is strongly recommended from TIMER to ground, to prevent any false triggering.

VREG – VREG is the output of an internal low-dropout voltage regulator, where IN1 is the input. The regulator is used to generate a regulated voltage source, less than 5.5 V, for the device. A 0.1-μF ceramic capacitor should be connected between VREG and ground to aid in noise rejection. In this configuration, upon disabling the device, the internal low-dropout regulator will also be disabled, which removes power from the internal circuitry and allows the device to be placed in low-quiescent-current mode. In applications where IN1 is less than 5.5 V, VREG and IN1 may be connected together. However, under these conditions, disabling the device does not place the device in low-quiescent-current mode, because the internal low-dropout voltage regulator is being bypassed, thereby keeping internal circuitry operational. If VREG and IN1 are connected together, a 0.1-μF ceramic capacitor between VREG and ground is not needed if IN1 already has a bypass capacitor of 1 μF to 10 μF.

VSENSE1, VSENSE2 – VSENSE1 and VSENSE2 can be used to detect undervoltage conditions on external circuitry. If VSENSE1 senses a voltage below approximately 1.23 V, PWRGD1 is pulled low. Similarly, a voltage less than 1.23 V on VSENSE2 causes PWRGD2 to be pulled low.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
Input voltage range	$V_{I(IN1)}$, $V_{I(ISENSE1)}$, $V_{I(VSENSE1)}$, $V_{I(VSENSE2)}$, $V_{I(ISET1)}$, $V_{I(ENABLE)}$, $V_{I(VREG)}$	–0.3 to 15	V
	$V_{I(IN2)}$, $V_{I(ISENSE2)}$, $V_{I(ISET2)}$	–0.3 to 7	V
Output voltage range	$V_{O(GATE1)}$	–0.3 to 30	V
	$V_{O(GATE2)}$	–0.3 to 22	V
	$V_{O(DISCH1)}$, $V_{O(PWRGD1)}$, $V_{O(PWRGD2)}$, $V_{O(\overline{FAULT})}$, $V_{O(DISCH2)}$, $V_{O(TIMER)}$	–0.3 to 15	V
Sink current range	$I_{(GATE1)}$, $I_{(GATE2)}$, $I_{(DISCH1)}$, $I_{(DISCH2)}$	0 to 100	mA
	$I_{(PWRGD1)}$, $I_{(PWRGD2)}$, $I_{(TIMER)}$, $I_{(\overline{FAULT})}$	0 to 10	mA
Operating virtual junction temperature range, T_J		–40 to 100	°C
Storage temperature range, T_{stg}		–55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are respect to DGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW-20	1015 mW	13.55 mW/°C	406 mW	203 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_I	Input voltage	$V_{I(IN1)}$, $V_{I(ISENSE1)}$, $V_{I(VSENSE1)}$, $V_{I(VSENSE2)}$, $V_{I(ISET1)}$	3		13	V
		$V_{I(IN2)}$, $V_{I(ISENSE2)}$, $V_{I(ISET2)}$, $V_{I(VREG)}$	3		5.5	
		$V_{I(ISENSE1)}$, $V_{I(ISET1)}$, $V_{I(VSENSE1)}$			$V_{I(IN1)}$	
		$V_{I(ISENSE2)}$, $V_{I(ISET2)}$, $V_{I(VSENSE2)}$			$V_{I(IN2)}$	
T_J	Operating virtual junction temperature		–40		100	°C

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range (–40°C < T_A < 85°C), 3 V ≤ $V_{I(IN1)}$ ≤13 V, 3 V ≤ $V_{I(IN2)}$ ≤ 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
$I_{I(IN1)}$	Input current, IN1	$V_{I(\overline{ENABLE})}$ = 5 V (TPS2301), $V_{I(\overline{ENABLE})}$ = 0 V (TPS2300)			0.5	1	mA
$I_{I(IN2)}$	Input current, IN2				75	200	µA
$I_{I(stby)}$	Standby current (sum of currents into IN1, IN2, ISENSE1, ISENSE2, ISET1, and ISET2)	$V_{I(ENABLE)}$ = 0 V (TPS2301), $V_{I(\overline{ENABLE})}$ = 5 V (TPS2300)				5	µA
GATE1							
$V_{G(GATE1\_3V)}$	Gate voltage	$I_{I(GATE1)}$ = 500 nA, DISCH1 open	$V_{I(IN1)}$ = 3 V	9	11.5		V
$V_{G(GATE1\_4.5V)}$			$V_{I(IN1)}$ = 4.5 V	10.5	14.5		
$V_{G(GATE1\_10.8V)}$			$V_{I(IN1)}$ = 10.8 V	16.8	21		
$V_{C(GATE1)}$	Clamping voltage, GATE1 to DISCH1			9	10	12	V
$I_{S(GATE1)}$	Source current, GATE1	3 V ≤ $V_{I(IN1)}$ ≤ 13.2 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE1)}$ = $V_{I(IN1)}$ + 6 V		10	14	20	µA
	Sink current, GATE1	3 V ≤ $V_{I(IN1)}$ ≤ 13.2 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE1)}$ = $V_{I(IN1)}$		50	75	100	µA
$t_{r(GATE1)}$	Rise time, GATE1	C_g to GND = 1 nF(1)	$V_{I(IN1)}$ = 3 V		0.5		ms
			$V_{I(IN1)}$ = 4.5 V		0.6		
			$V_{I(IN1)}$ = 10.8 V		1		
$t_{f(GATE1)}$	Fall time, GATE1	C_g to GND = 1 nF(1)	$V_{I(IN1)}$ = 3 V		0.1		ms
			$V_{I(IN1)}$ = 4.5 V		0.12		
			$V_{I(IN1)}$ = 10.8 V		0.2		
GATE2							
$V_{G(GATE2\_3V)}$	Gate voltage	$I_{I(GATE2)}$ = 500 nA, DISCH2 open	$V_{I(IN2)}$ = 3 V	9	11.7		V
$V_{G(GATE2\_4.5V)}$			$V_{I(IN2)}$ = 4.5 V	10.5	14.7		
$V_{C(GATE2)}$	Clamping voltage, GATE2 to DISCH2			9	10	12	V
$I_{S(GATE2)}$	Source current, GATE2	3 V ≤ $V_{I(IN2)}$ ≤ 5.5 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE2)}$ = $V_{I(IN2)}$ + 6 V		10	14	20	µA
	Sink current, GATE2	3 V ≤ $V_{I(IN2)}$ ≤ 5.5 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE2)}$ = $V_{I(IN2)}$		50	75	100	µA
$t_{r(GATE2)}$	Rise time, GATE2	C_g to GND = 1 nF(1), $V_{I(IN2)}$ = 3 V	$V_{O(VREG)}$ = 3 V		0.5		ms
		$V_{I(IN2)}$ = 4.5 V			0.6		
$t_{f(GATE2)}$	Fall time, GATE2	C_g to GND = 1 nF(1), $V_{I(IN2)}$ = 3 V			0.1		ms
		$V_{I(IN2)}$ = 4.5 V			0.12		

(1) Specified, but not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating temperature range (–40°C < T_A < 85°C), 3V ≤$V_{I(IN1)}$ ≤13V, 3V ≤ $V_{I(IN2)}$ ≤ 5.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TIMER							
$V_{(TO\_TIMER)}$	Threshold voltage, TIMER			0.4	0.5	0.6	V
	Charge current, TIMER	$V_{I(TIMER)}$ = 0 V		35	50	65	µA
	Discharge current, TIMER	$V_{I(TIMER)}$ = 1 V		1	2.5		mA
CIRCUIT BREAKER							
$V_{IT(CB)}$	Threshold voltage, circuit breaker	R_{ISETx} = 1 kΩ		40	50	60	mV
		R_{ISETx} = 400 Ω, T_A = 25°C		14	19	24	
		R_{ISETx} = 1 kΩ, T_A = 25°C		44	50	53	
		R_{ISETx} = 1.5 kΩ, T_A = 25°C		68	73	78	
$I_{(IB\_ISENSEx)}$	Input bias current, I_{SENSEx}				0.1	5	µA
	Discharge current, GATEx	$V_{O(GATEx)}$ = 4 V		400	800		mA
		$V_{O(GATEx)}$ = 1 V		25	150		
$t_{pd(CB)}$	Propagation (delay) time, comparator inputs to gate output	C_g = 50 pF, (50% to 10%),	10 mV overdrive, C_{TIMER} = 50 pF		1.3		µs
$\overline{\text{ENABLE}}$, ACTIVE LOW (TPS2300)							
$V_{IH(\overline{ENABLE})}$	High-level input voltage, $\overline{\text{ENABLE}}$			2			V
$V_{IL(\overline{ENABLE})}$	Low-level input voltage, $\overline{\text{ENABLE}}$					0.8	V
$R_{I(\overline{ENABLE})}$	Input pullup resistance, $\overline{\text{ENABLE}}$	See (1)		100	200	300	kΩ
$t_{d(off\_\overline{ENABLE})}$	Turnoff delay time, $\overline{\text{ENABLE}}$	$V_{I(\overline{ENABLE})}$ increasing above stop threshold; 100 ns rise time, 20 mV overdrive (2)			60		µs
$t_{d(on\_\overline{ENABLE})}$	Turnon delay time, $\overline{\text{ENABLE}}$	$V_{I(\overline{ENABLE})}$ decreasing below start threshold; 100 ns fall time, 20 mV overdrive (2)			125		µs
ENABLE, ACTIVE HIGH (TPS2301)							
$V_{IH(\overline{ENABLE})}$	High-level input voltage, ENABLE			2			V
$V_{IL(\overline{ENABLE})}$	Low-level input voltage, ENABLE					0.7	V
$R_{I(\overline{ENABLE})}$	Input pulldown resistance, ENABLE			100	150	300	kΩ
$t_{d(on\_\overline{ENABLE})}$	Turnon delay time, ENABLE	$V_{I(ENABLE)}$ increasing above start threshold; 100 ns rise time, 20 mV overdrive (2)			85		µs
$t_{d(off\_\overline{ENABLE})}$	Turnoff delay time, ENABLE	$V_{I(ENABLE)}$ decreasing below stop threshold; 100 ns fall time, 20 mV overdrive (2)			100		µs
PREREG							
$V_{(VREG)}$	PREREG output voltage	4.5 ≤ $V_{I(IN1)}$ ≤ 13 V		3.5	4.1	5.5	V
$V_{(drop\_PREREG)}$	PREREG dropout voltage	$V_{I(IN1)}$ = 3 V				0.1	V

(1) Test I_O of $\overline{\text{ENABLE}}$ at $V_{I(\overline{ENABLE})}$ = 1 V and 0 V, then $R_{I(\overline{ENABLE})} = \frac{1\ V}{I_{O\_0V} - I_{O\_1V}}$
(2) Specified, but not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating temperature range (–40°C < T_A < 85°C), 3V ≤$V_{I(IN1)}$ ≤13V, 3V ≤ $V_{I(IN2)}$ ≤ 5.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREG UVLO						
$V_{(TO\_UVLOstart)}$	Output threshold voltage, start		2.75	2.85	2.95	V
$V_{(TO\_UVLOstop)}$	Output threshold voltage, stop		2.65	2.78		V
$V_{hys(UVLO)}$	Hysteresis		50	75		mV
	UVLO sink current, GATEx	$V_{I(GATEx)}$ = 2 V	10			mA
PWRGD1 and PWRGD2						
$V_{IT(ISENSEx)}$	Trip threshold, VSENSEx	$V_{I(VSENSEx)}$ decreasing	1.2	1.225	1.25	V
V_{hys}	Hysteresis voltage, power-good comparator		20	30	40	mV
$V_{O(sat\_PWRGDx)}$	Output saturation voltage, PWRGDx	I_O = 2 mA		0.2	0.4	V
$V_{O(VREG\_min)}$	Minimum $V_{O(VREG)}$ for valid power-good	I_O = 100 μA, $V_{O(PWRGDx)}$ = 1 V			1	V
	Input bias current, power-good comparator	$V_{I(VSENSEx)}$ = 5.5 V			1	μA
$I_{lkg(PWRGDx)}$	Leakage current, PWRGDx	$V_{O(PWRGDx)}$ = 13 V			1	μA
t_{dr}	Delay time, rising edge, PWRGDx	$V_{I(VSENSEx)}$ increasing, overdrive = 20 mV, t_r = 100 ns[(1)]		25		μs
t_{df}	Delay time, falling edge, PWRGDx	$V_{I(VSENSEx)}$ decreasing, overdrive = 20 mV, t_r = 100 ns[(1)]		2		μs
$\overline{\text{FAULT}}$ OUTPUT						
$V_{O(sat\_\overline{FAULT})}$	Output saturation voltage, $\overline{\text{FAULT}}$	I_O = 2 mA			0.4	V
$I_{lkg(\overline{FAULT})}$	Leakage current, $\overline{\text{FAULT}}$	$V_{O(\overline{FAULT})}$ = 13 V			1	μA
DISCH1 AND DISCH2						
$I_{(DISCH)}$	Discharge current, DISCHx	$V_{I(DISCHx)}$ = 1.5 V, $V_{I(VIN1)}$ = 5 V	5	10		mA
$V_{IH(DISCH)}$	Discharge on high-level input voltage		2			V
$V_{IL(DISCH)}$	Discharge on low-level input voltage				1	V

(1) Specified, but not production tested.

PARAMETER MEASUREMENT INFORMATION

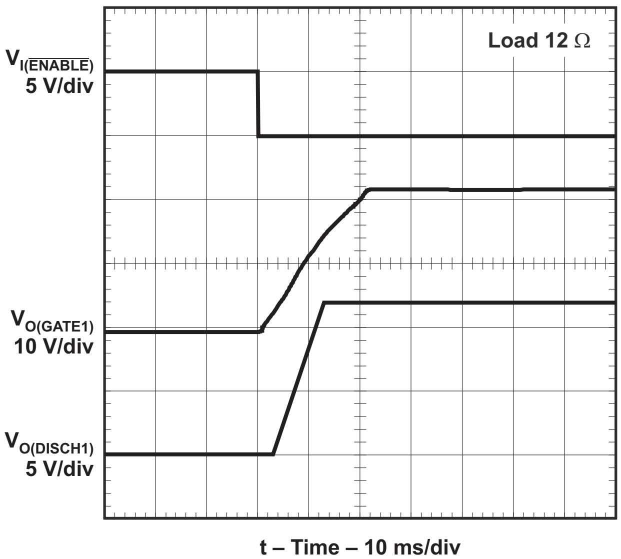


Figure 1. Turnon Voltage Transition of Channel 1

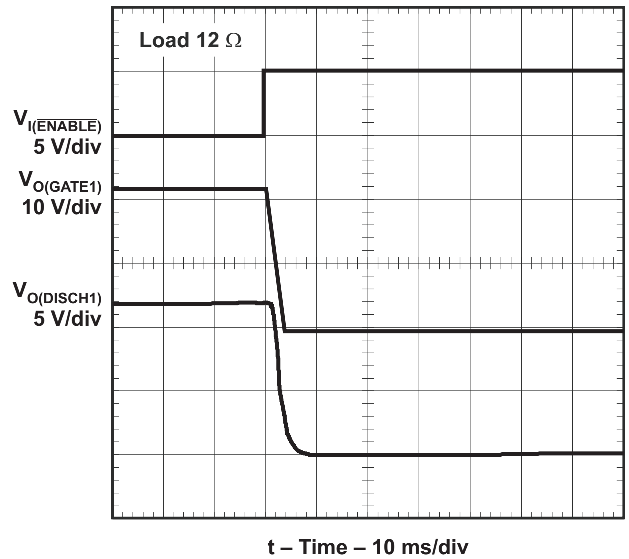


Figure 2. Turnoff Voltage Transition of Channel 1

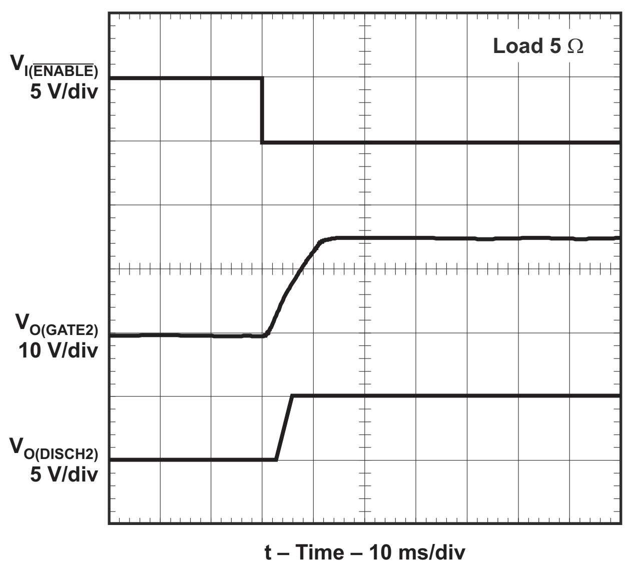


Figure 3. Turnon Voltage Transitioin of Channel 2

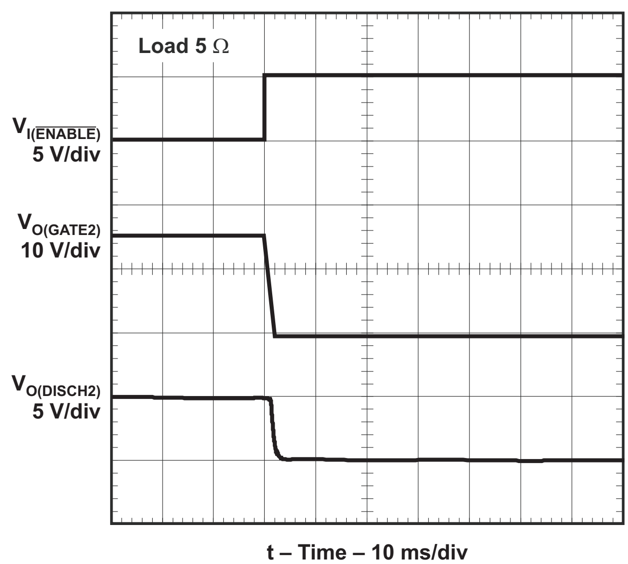


Figure 4. Turnoff Voltage Transition of Channel 2

PARAMETER MEASUREMENT INFORMATION (continued)

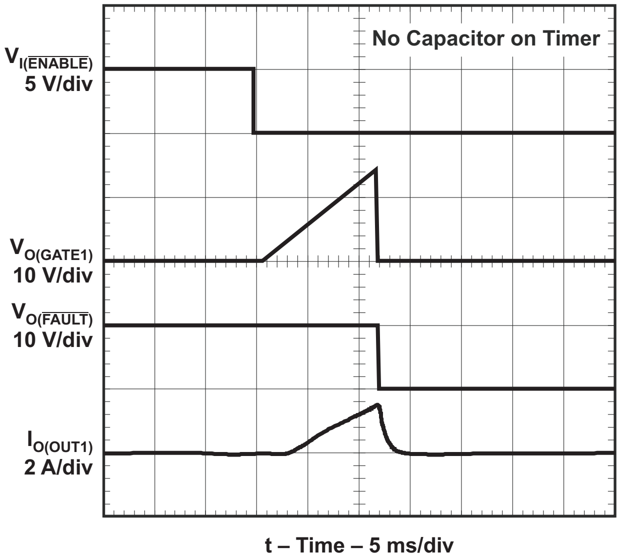


Figure 5. Channel 1 Overcurrent Response: Enabled Into Overcurrent Load

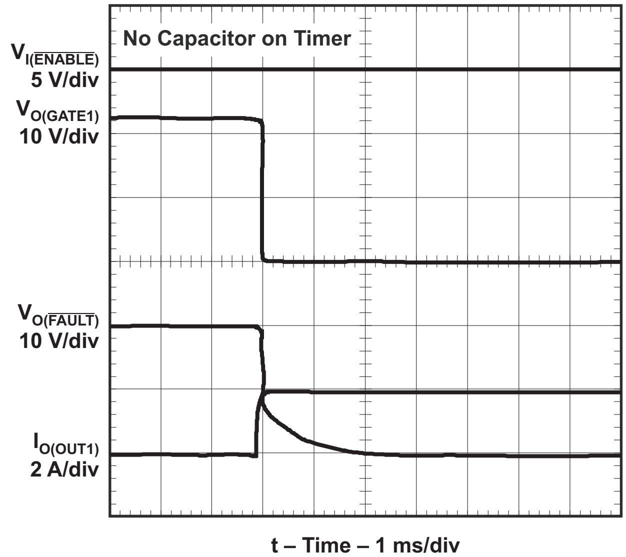


Figure 6. Channel 1 Overcurrent Response: an Overcurrent Load Plugged Into the Enabled Board

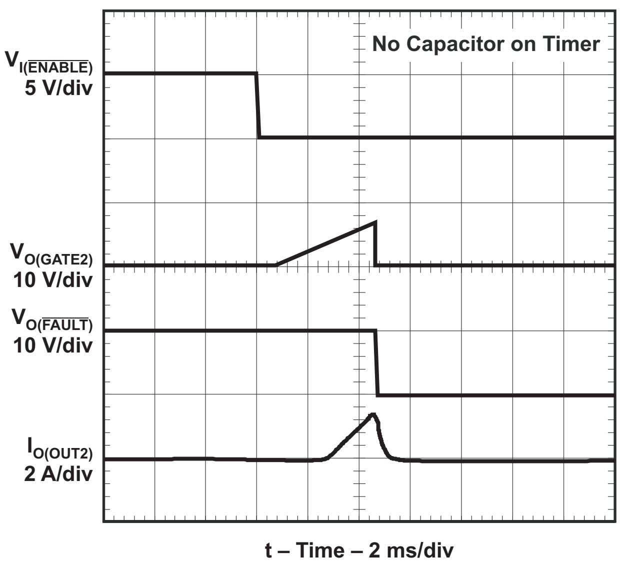


Figure 7. Channel 2 Overcurrent Response: Enabled Into Overcurrent Load

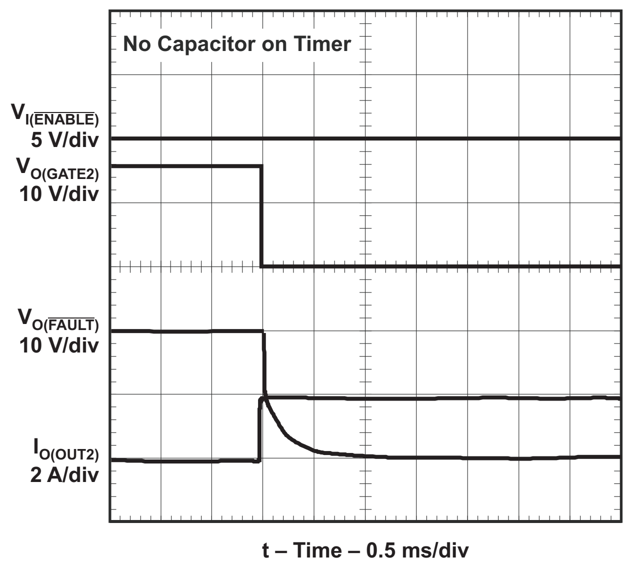


Figure 8. Channel 2 Overcurrent Response: an Overcurrent Load Plugged Into the Enabled Board

PARAMETER MEASUREMENT INFORMATION (continued)

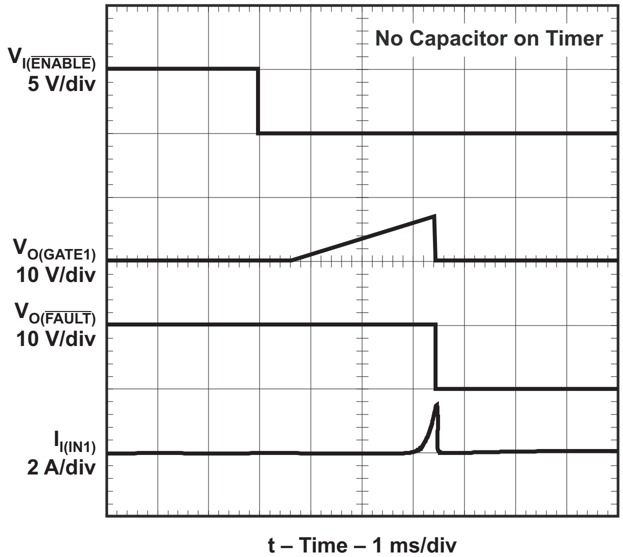


Figure 9. Channel 1 – Enabled Into Short Circuit

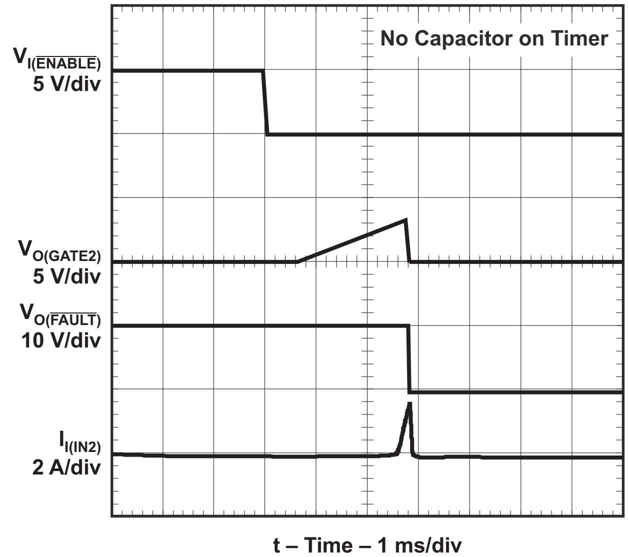


Figure 10. Channel 1 – Enabled Into Short Circuit

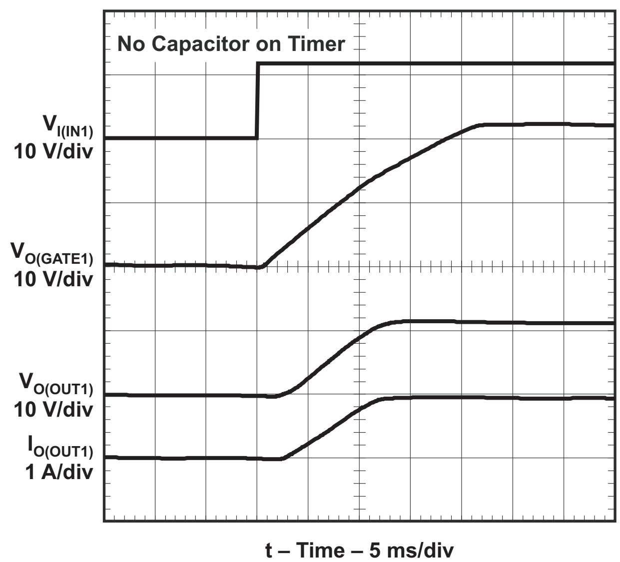


Figure 11. Channel 1 – Hot Plug

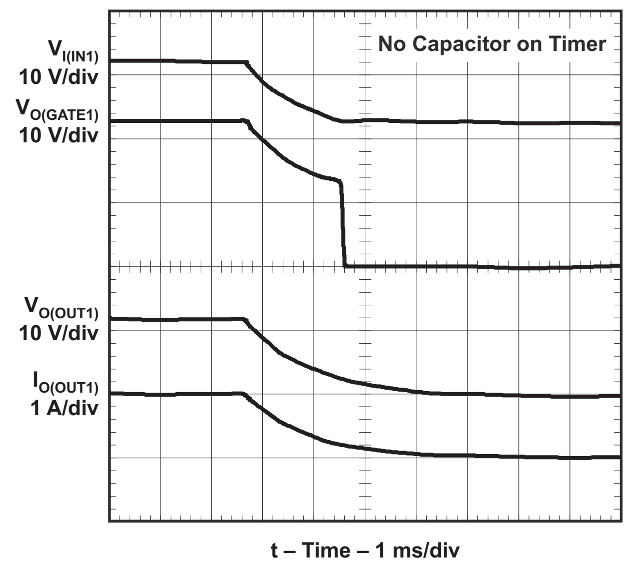


Figure 12. Channel 1 – Hot Removal

PARAMETER MEASUREMENT INFORMATION (continued)

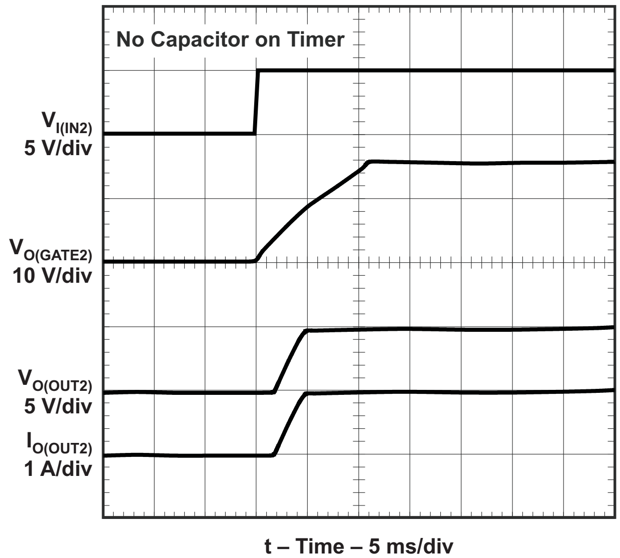


Figure 13. Channel 2 - Hot Plug

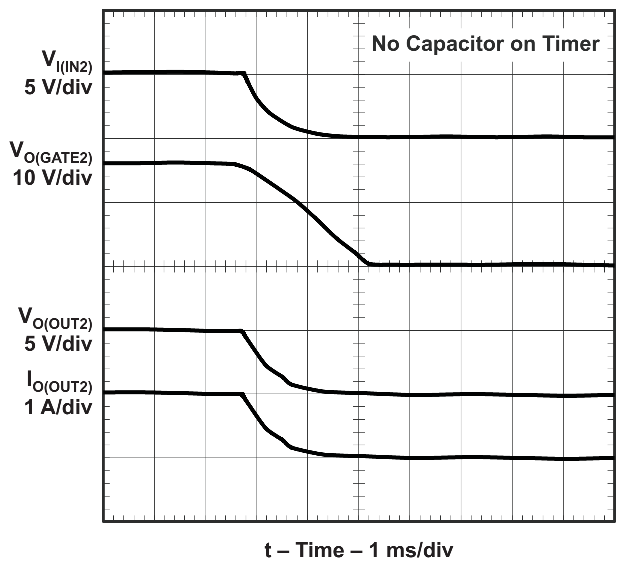


Figure 14. Channel 2 - Hot Removal

TYPICAL CHARACTERISTICS

INPUT CURRENT 1 (ENABLED) vs INPUT VOLTAGE 1

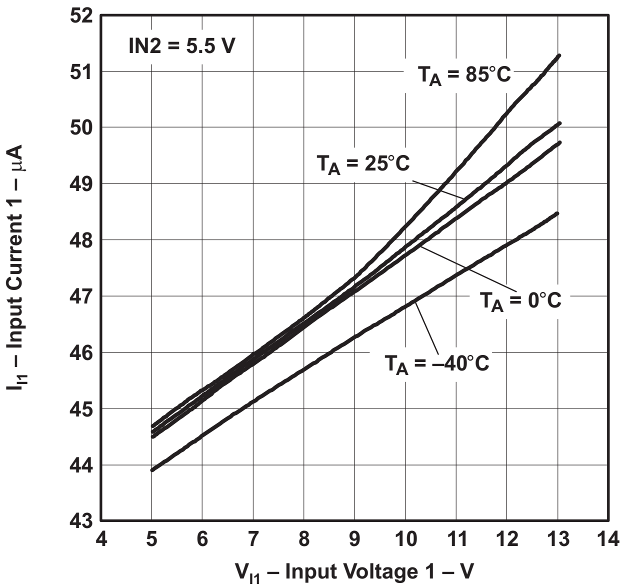


Figure 15.

INPUT CURRENT 2 (ENABLED) vs INPUT VOLTAGE 2

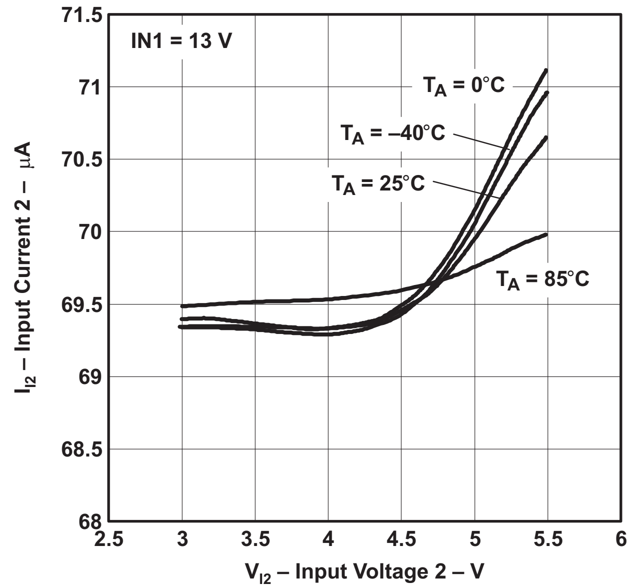


Figure 16.

INPUT CURRENT 1 (DISABLED) vs INPUT VOLTAGE 1

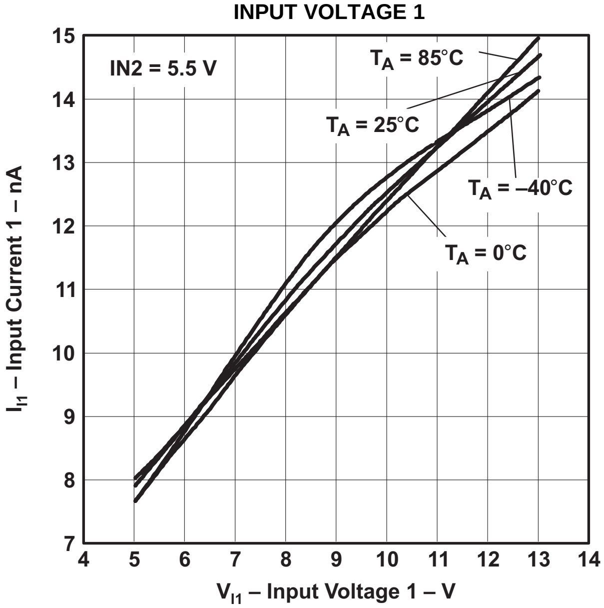


Figure 17.

INPUT CURRENT 2 (DISABLED) vs INPUT VOLTAGE 2

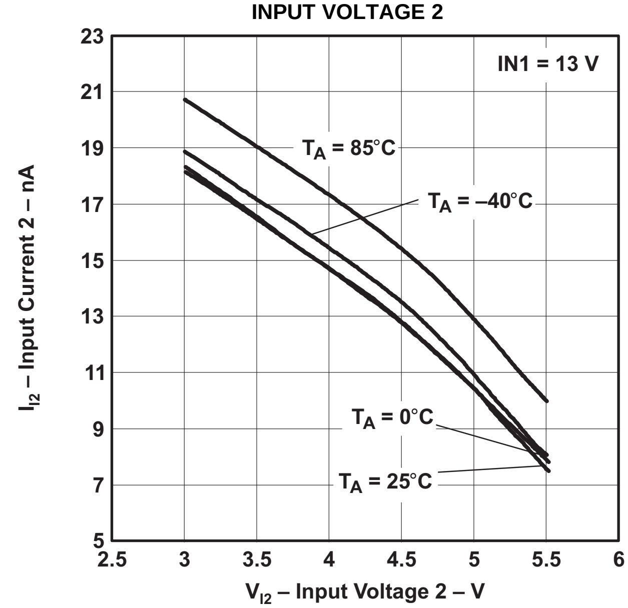


Figure 18.

TYPICAL CHARACTERISTICS (continued)

GATE1 OUTPUT VOLTAGE vs INPUT VOLTAGE 1

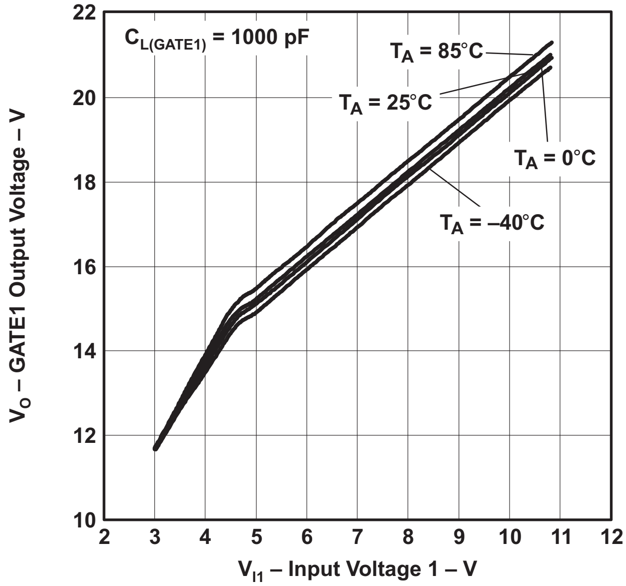


Figure 19.

GATE1 VOLTAGE RISE TIME vs GATE1 LOAD CAPACITANCE

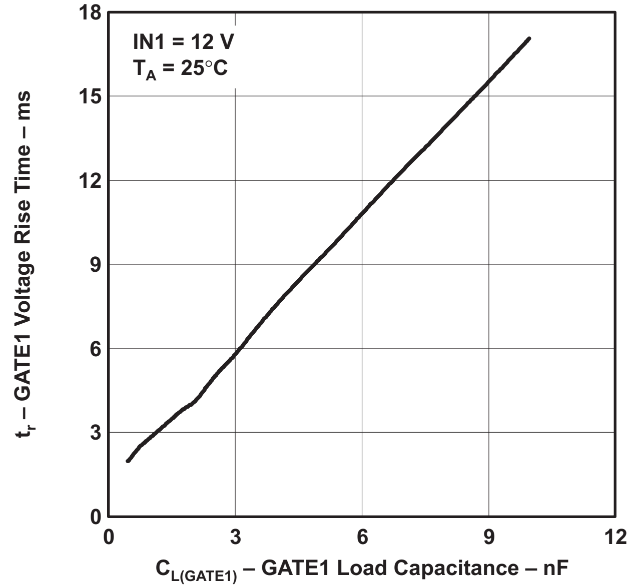


Figure 20.

GATE1 VOLTAGE FALL TIME vs GATE1 LOAD CAPACITANCE

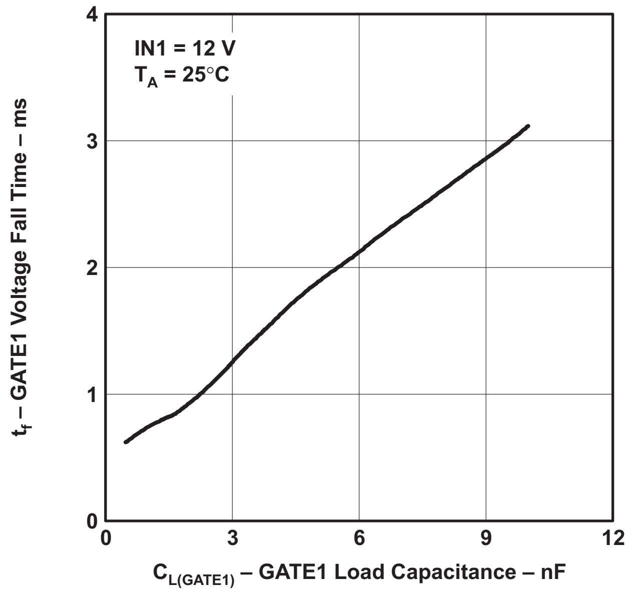


Figure 21.

GATE1 OUTPUT CURRENT vs GATE1 VOLTAGE

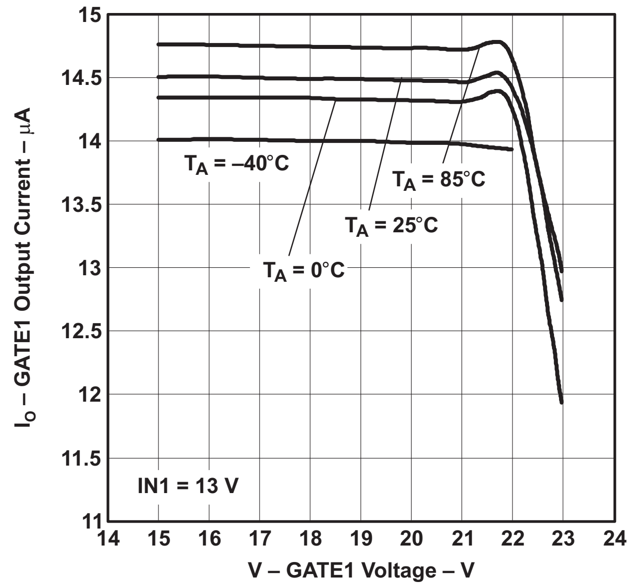


Figure 22.

TYPICAL CHARACTERISTICS (continued)

CIRCUIT-BREAKER RESPONSE TIME
vs
TIMER CAPACITANCE

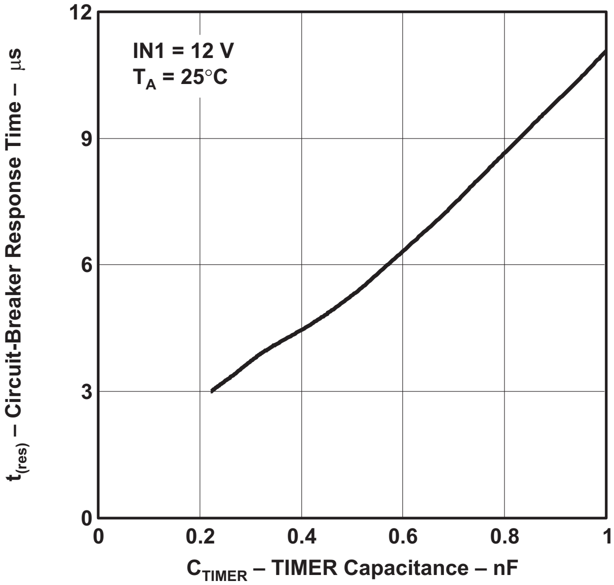


Figure 23.

LOAD VOLTAGE 1 DISCHARGE TIME
vs
LOAD CAPACITANCE

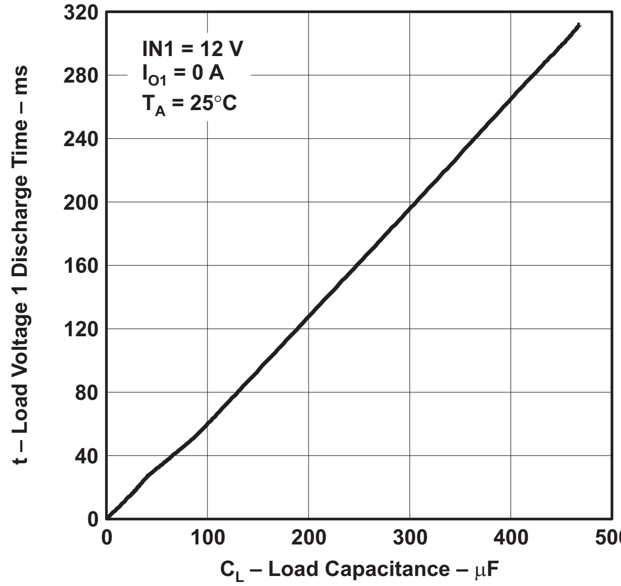


Figure 24.

UVLO START AND STOP THRESHOLDS
vs
TEMPERATURE

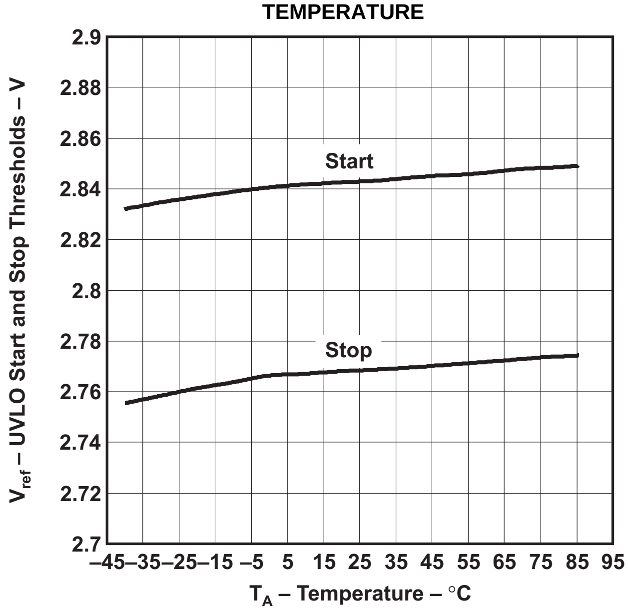


Figure 25.

PWRGDx INPUT THRESHOLD
vs
TEMPERATURE

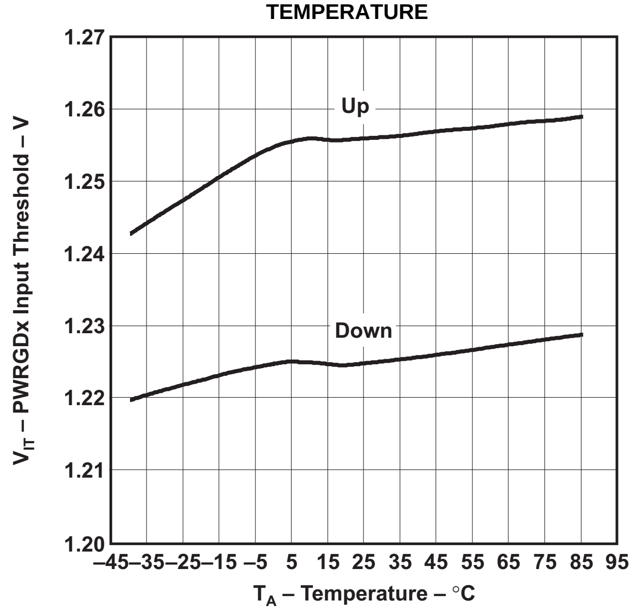


Figure 26.

APPLICATION INFORMATION

TYPICAL APPLICATION DIAGRAM

This diagram shows a typical dual hot-swap application. The pullup resistors at PWRGD1, PWRGD2 and $\overline{\text{FAULT}}$ should be relatively large (e.g., 100 kΩ) to reduce power loss unless they are required to drive a large load.

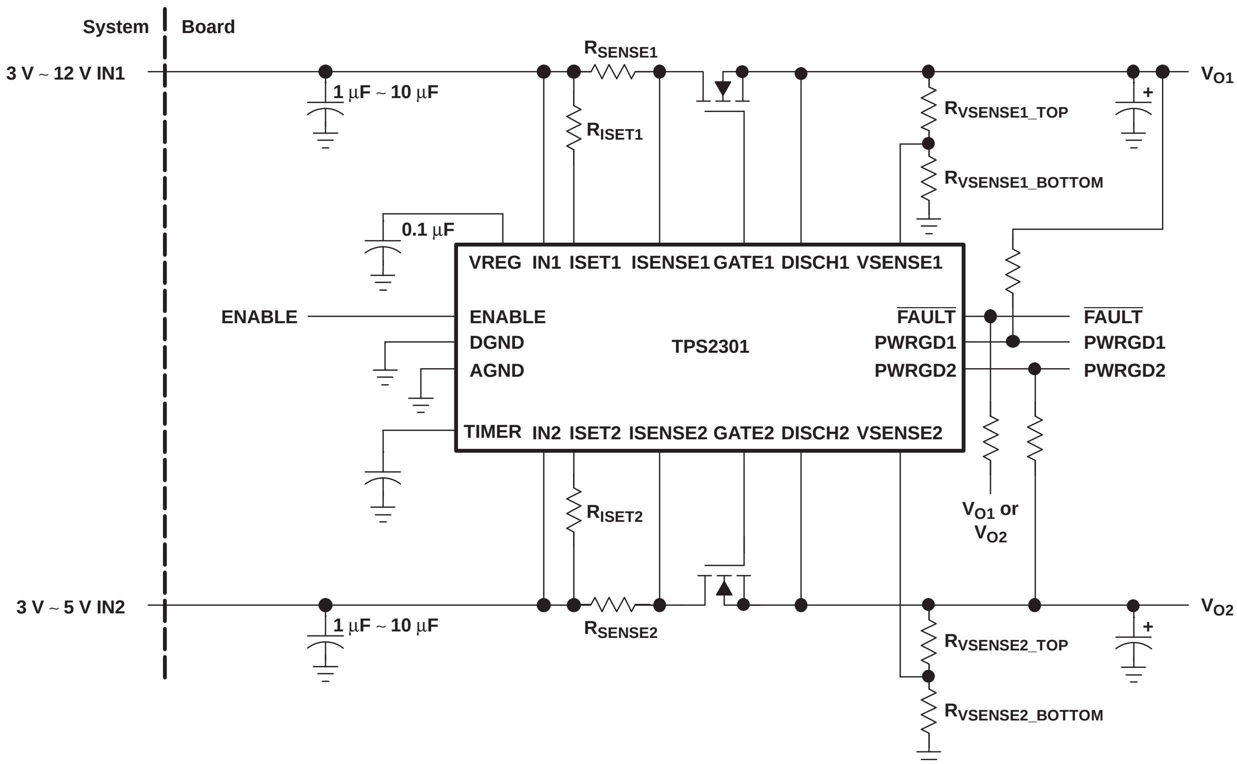


Figure 27. Typical Dual Hot-Swap Application

INPUT CAPACITOR

A 0.1-µF ceramic capacitor in parallel with a 1-µF ceramic capacitor should be placed on the input power terminals near the connector on the hot-plug board to help stabilize the voltage rails on the cards. The TPS2300/01 does not need to be mounted near the connector or these input capacitors. For applications with more severe power environments, a 2.2-µF or higher ceramic capacitor is recommended near the input terminals of the hot-plug board. A bypass capacitor for IN1 and for IN2 should be placed close to the device.

OUTPUT CAPACITOR

A 0.1-µF ceramic capacitor is recommended per load on the TPS2300/01; these capacitors should be placed close to the external FETs and to TPS2300/01. A larger bulk capacitor is also recommended on the load. The value of the bulk capacitor should be selected based on the power requirements and the transients generated by the application.

EXTERNAL FET

To deliver power from the input sources to the loads, each channel needs an external N-channel MOSFET. A few widely used MOSFETs are shown in Table 3. But many other MOSFETs in the market can also be used with TPS23xx in hot-swap systems.

Table 3. Some Available N-Channel MOSFETs

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	IRF7601	N-channel, $r_{DS(on)}$ = 0.035 Ω, 4.6 A, Micro-8	International Rectifier
	MTSF3N03HDR2	N-channel, $r_{DS(on)}$ = 0.040 Ω, 4.6 A, Micro-8	ON Semiconductor
	IRF7101	Dual N-channel, $r_{DS(on)}$ = 0.1 Ω, 2.3 A, SO-8	International Rectifier
	MMSF5N02HDR2	Dual N-channel, $r_{DS(on)}$ = 0.04 Ω, 5 A, SO-8	ON Semiconductor
2 to 5	IRF7401	N-channel, $r_{DS(on)}$ = 0.022 Ω, 7 A, SO-8	International Rectifier
	MMSF5N02HDR2	N-channel, $r_{DS(on)}$ = 0.025 Ω, 5 A, SO-8	ON Semiconductor
	IRF7313	Dual N-channel, $r_{DS(on)}$ = 0.029 Ω, 5.2 A, SO-8	International Rectifier
	SI4410	N-channel, $r_{DS(on)}$ = 0.020 Ω, 8 A, SO-8	Vishay Dale
5 to 10	IRLR3103	N-channel, $r_{DS(on)}$ = 0.019 Ω, 29 A, d-Pak	International Rectifier
	IRLR2703	N-channel, $r_{DS(on)}$ = 0.045 Ω, 14 A, d-Pak	International Rectifier

TIMER

For most applications, a minimum capacitance of 50 pF is recommended to prevent false triggering. This capacitor should be connected between TIMER and ground. The presence of an overcurrent condition on either channel of the TPS2300/01 causes a 50-μA current source to begin charging this capacitor. If the overcurrent condition persists until the capacitor has been charged to approximately 0.5 V, the TPS2300/01 latches off the offending channels and pulls the $\overline{\text{FAULT}}$ pin low. The timer capacitor can be made as large as desired to provide additional time delay before registering a fault condition. The time delay is approximately:

dt(sec) = C_{TIMER}(F) × 10,000(Ω).

OUTPUT-VOLTAGE SLEW-RATE CONTROL

When enabled, the TPS2300/01 controllers supply the gates of each external MOSFET transistor with a current of approximately 15 μA. The slew rate of the MOSFET source voltage is thus limited by the gate-to-drain capacitance C_{gd} of the external MOSFET capacitor to a value approximating:

$$\frac{dV_S}{dt} = \frac{15\ \mu A}{C_{gd}} \quad (1)$$

If a slower slew rate is desired, an additional capacitance can be connected between the gate of the external MOSFET and ground.

VREG CAPACITOR

The internal voltage regulator connected to VREG requires an external capacitor to ensure stability. A 0.1-μF or 0.22-μF ceramic capacitor is recommended.

GATE DRIVE CIRCUITRY

The TPS2300/01 includes four separate features associated with each gate-drive terminal:

- A charging current of approximately 15 μA is applied to enable the external MOSFET transistor. This current is generated by an internal charge pump that can develop a gate-to-source potential (referenced to DISCH1 or DISCH2) of 9 V–12 V. DISCH1 and DISCH2 must be connected to the respective external MOSFET source terminals to ensure proper operation of this circuitry.
- A discharge current of approximately 75 μA is applied to disable the external MOSFET transistor. Once the transistor gate voltage has dropped below approximately 1.5 V, this current is disabled and the UVLO discharge driver is enabled instead. This feature allows the part to enter a low-current shutdown mode while ensuring that the gates of the external MOSFET transistors remain at a low voltage.
- During a UVLO condition, the gates of both MOSFET transistors are pulled down by internal PMOS transistors. These transistors continue to operate even if IN1 and IN2 are both at 0 V. This circuitry also helps hold the external MOSFET transistors off when power is suddenly applied to the system.
- During an overcurrent fault condition, the external MOSFET transistor that exhibited an overcurrent condition is rapidly turned off by an internal pulldown circuit capable of pulling in excess of 400 mA (at 4 V) from the

pin. Once the gate has been pulled below approximately 1.5 V, this driver is disengaged and the UVLO driver is enabled instead. If one channel experiences an overcurrent condition and the other does not, then only the channel that is conducting excessive current is turned off rapidly. The other channel continues to operate normally.

SETTING THE CURRENT-LIMIT CIRCUIT-BREAKER THRESHOLD

Using channel 1 as an example, the current sensing resistor $R_{ISENSE1}$ and the current limit setting resistor R_{ISET1} determine the current limit of the channel, and can be calculated by the following equation:

$$I_{LMT1} = \frac{R_{ISET1} \times 50 \times 10^{-6}}{R_{ISENSE1}} \tag{2}$$

Typically $R_{ISENSE1}$ is usually very small (0.001Ω to 0.1Ω). If the trace and solder-junction resistances between the junction of $R_{ISENSE1}$ and ISENSE1 and the junction of $R_{ISENSE1}$ and R_{ISET1} are greater than 10% of the $R_{ISENSE1}$ value, then these resistance values should be added to the $R_{ISENSE1}$ value used in the calculation above.

The above information and calculation also apply to channel 2. Table 4 shows some of the current sense resistors available in the market.

Table 4. Some Current Sense Resistors

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 1	WSL-1206, 0.05 1%	0.05 Ω, 0.25 W, 1% resistor	Vishay Dale
1 to 2	WSL-1206, 0.025 1%	0.025 Ω, 0.25 W, 1% resistor	
2 to 4	WSL-1206, 0.015 1%	0.015 Ω, 0.25 W, 1% resistor	
4 to 6	WSL-2010, 0.010 1%	0.010 Ω, 0.5 W, 1% resistor	
6 to 8	WSL-2010, 0.007 1%	0.007 Ω, 0.5 W, 1% resistor	
8 to 10	WSR-2, 0.005 1%	0.005 Ω, 0.5 W, 1% resistor	

SETTING THE POWER-GOOD THRESHOLD VOLTAGE

The two feedback resistors $R_{VSENSEx\_TOP}$ and $R_{VSENSEx\_BOT}$ connected between V_{Ox} and ground form a resistor divider setting the voltage at the VSENSEx pins. VSENSE1 voltage equals:

$V_{I(SENSE1)} = V_O \times R_{VSENSE1\_BOT} / (R_{VSENSE1\_TOP} + R_{VSENSE1\_BOT})$

This voltage is compared to an internal voltage reference (1.225 V ±2%) to determine whether the output voltage level is within a specified tolerance. For example, given a nominal output voltage at V_{O1}, and defining V_{O1_min} as the minimum required output voltage, then the feedback resistors are defined by:

$$R_{VSENSE1\_TOP} = \frac{V_{O1\_min} - 1.225}{1.225} \times R_{VSENSE1\_BOT} \tag{3}$$

Start the process by selecting a large standard resistor value for $R_{VSENSE1\_BOT}$ to reduce power loss. Then $R_{VSENSE1\_TOP}$ can be calculated by inserting all of the known values into the equation above. When V_{O1} is lower than V_{O1_min}, PWRGD1 is low as long as the controller is enabled.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS2300/01 includes an undervoltage lockout (UVLO) feature that monitors the voltage present on the VREG pin. This feature disables both external MOSFETs if the voltage on VREG drops below 2.78 V (nominal) and re-enables normal operation when it rises above 2.85 V (nominal). Since VREG is fed from IN1 through a low-dropout voltage regulator, the voltage on VREG tracks the voltage on IN1 within 50 mV. While the undervoltage lockout is engaged, both GATE1 and GATE2 are held low by internal PMOS pulldown transistors, ensuring that the external MOSFET transistors remain off at all times, even if all power supplies have fallen to 0V.

SINGLE-CHANNEL OPERATION

Some applications may require only a single external MOS transistor. Such applications should use GATE1 and the associated circuitry (IN1, ISENSE1, ISET1, DISCH1). The IN2 pin should be grounded to disable the circuitry associated with the GATE2 pin. The VSENSE2 and PWRGD2 circuitry is unaffected by disabling GATE2, and may still be used if so desired.

POWER-UP CONTROL

The TPS2300/01 includes a 500 µs (nominal) start-up delay that ensures that internal circuitry has sufficient time to start before the device begins turning on the external MOSFETs. This delay is triggered only upon the rapid application of power to the circuit. If the power supply ramps up slowly, the undervoltage lockout circuitry provides adequate protection against undervoltage operation.

3-CHANNEL HOT-SWAP APPLICATION

Some applications require hot-swap control of up to three voltage rails, but may not explicitly require the sensing of the status of the output power on all three of the voltage rails. One such application is device bay, where dv/dt control of 3.3 V, 5 V, and 12 V is required. By using channel 2 to drive both the 3.3-V and 5-V power rails and channel 1 to drive the 12-V power rail, as is shown below, TPS2300/01 can deliver three different voltages to three loads while monitoring the status of two of the loads.

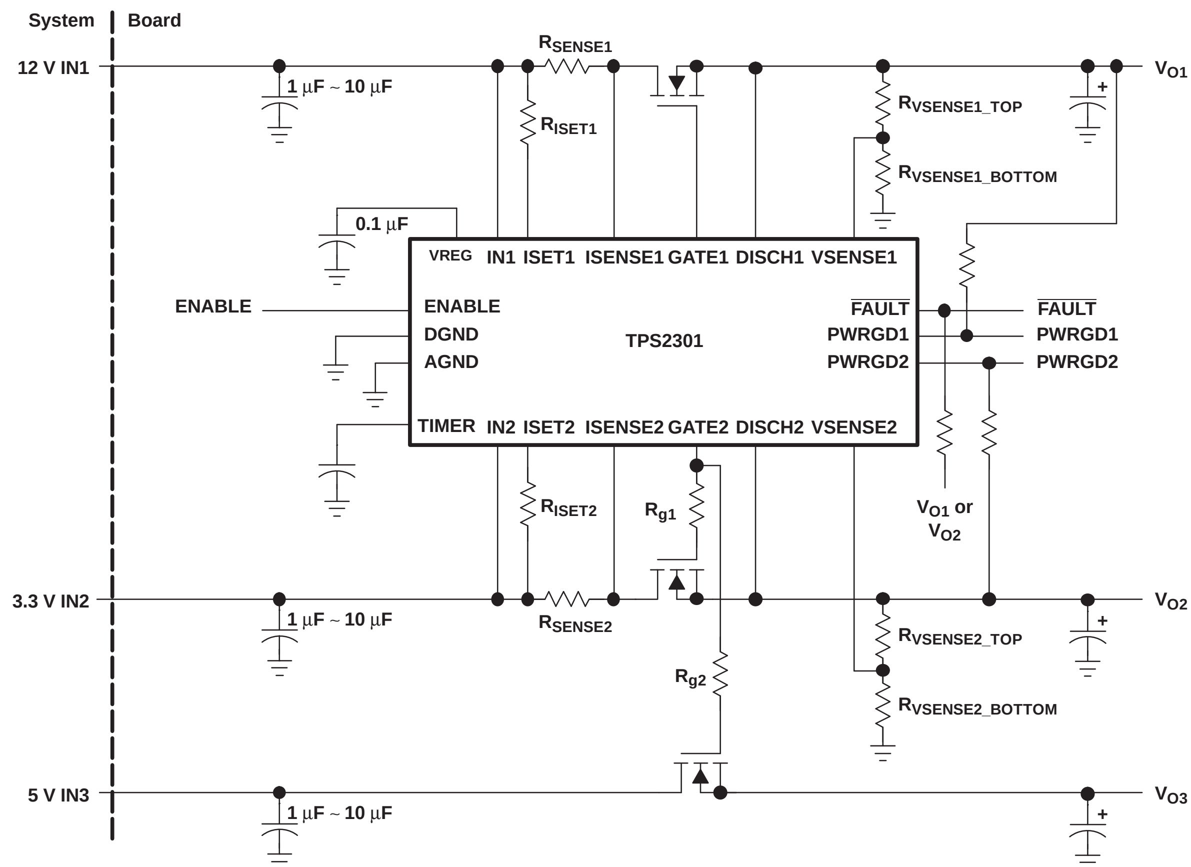


Figure 28. Three-Channel Application

Figure 29 shows ramp-up waveforms of the three output voltages.

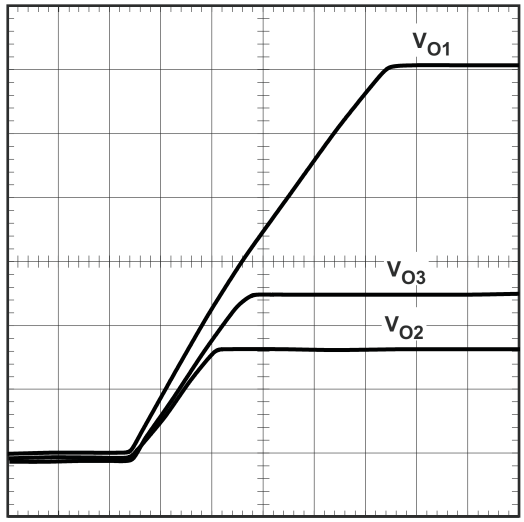


Figure 29.

REVISION HISTORY

Note: Revision history for previous versions is not available. Page numbers of previous versions may differ.

Changes from Revision G (November 2006) to Revision H **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2300IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2300I	Samples
TPS2300IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2300I	Samples
TPS2301IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2301I	Samples
TPS2301IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2301I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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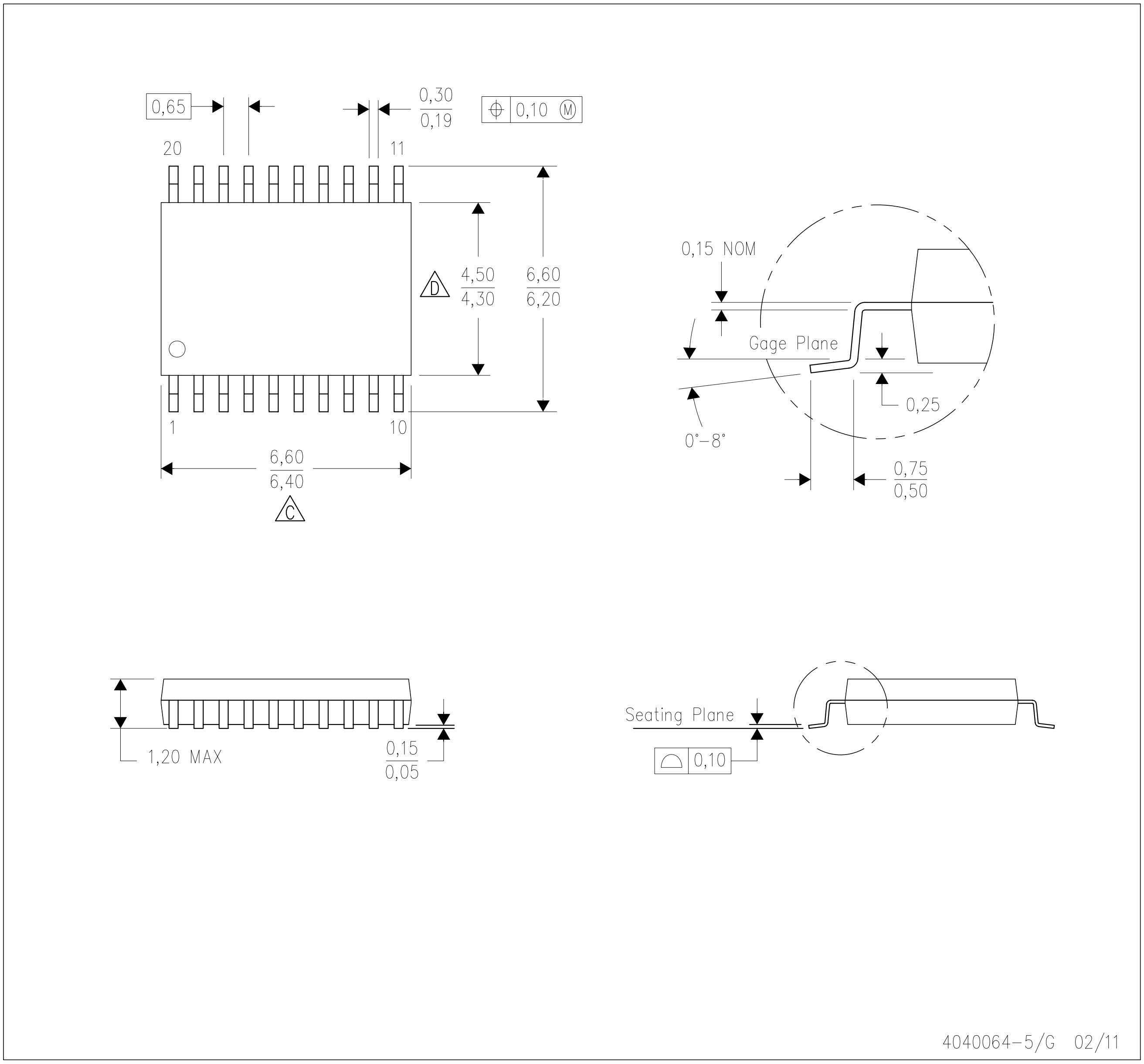
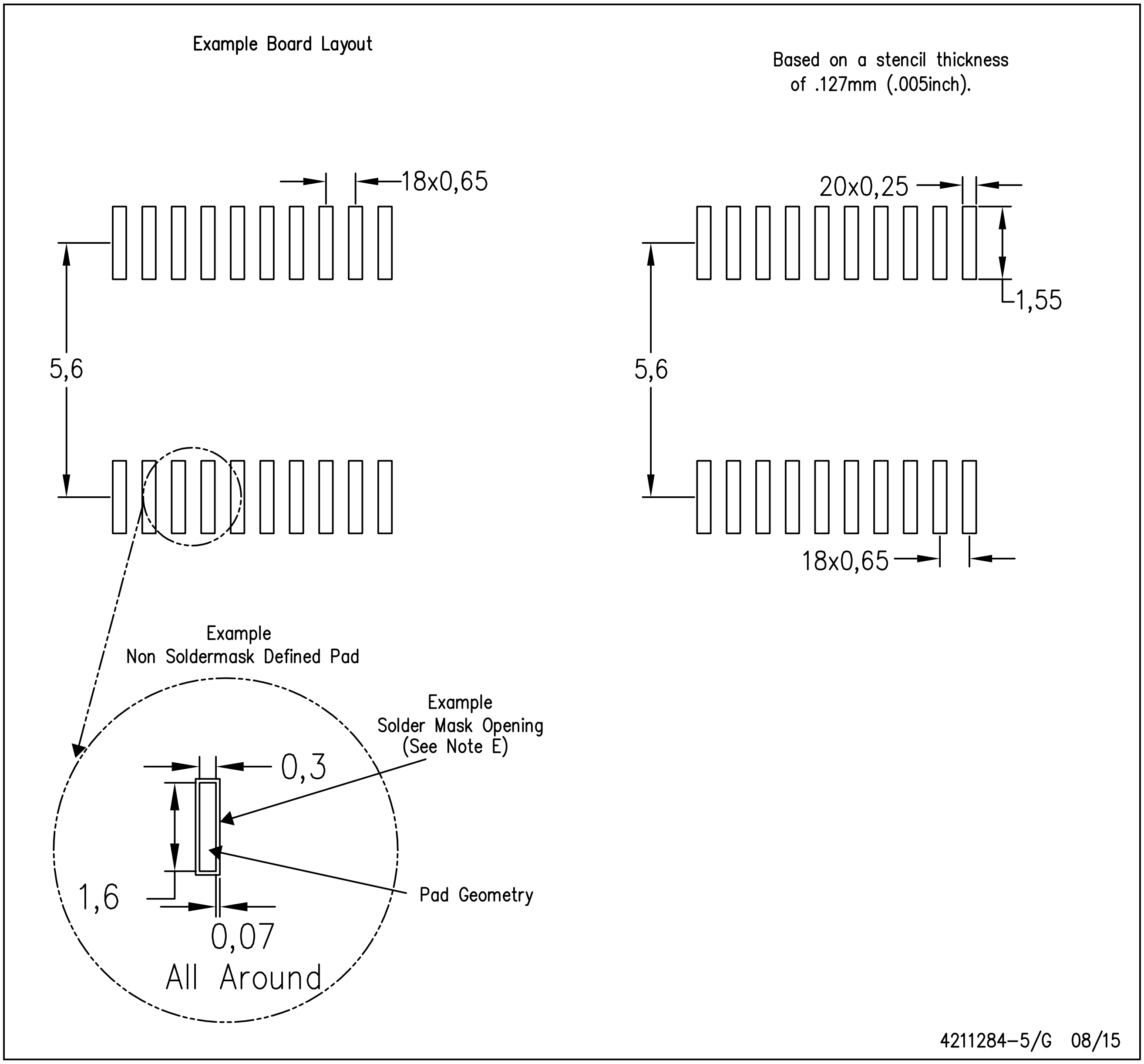
PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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