TPS54122-Q1 Dual-Output, 3-A, QuietSupply™ with Integrated DC-DC Converter and Low-Noise LDO

1 Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range:
  - VIN: 2.95 V to 6.0 V
  - LDOIN: V_{OUT} + V_{DO} to 5.5 V
  - BIAS: 2.375 V to 5.5 V
- Provides Two Configurable Supply Rails
- Independent Enable, Power Good, and Soft-Start
- 3-A, High-Efficiency, Synchronous, Step-Down Switcher:
  - Output Voltage Adjustable Down to 0.8 V
  - Sync to External Clock: 300 kHz to 2 MHz
  - 1% Reference Accuracy
- 3-A, Low-Noise LDO:
  - Output Noise: 17 μV_{RMS} at 10 Hz to 1 MHz with DC-DC Running
  - Output Voltage Range: 0.8 V to 3.6 V
  - Ultralow Dropout: 100 mV (typ) at 3 A
  - 1% Output Accuracy
  - Excellent Load and Line Transient Response
- Small Package: 5.5-mm × 3.5-mm VQFN-24

2 Applications

- Power Optimization in Automotive ECU Power
- Automotive Infotainment Systems
- Automotive ADAS Systems
- Powering Sensitive Clocking-Distribution Circuits
- Powering RF Components: VCOs, Receivers, and ADCs

3 Description

The TPS54122-Q1 combines the efficiency of a step-down switching (dc-dc) converter with a high power-supply rejection (PSR), low-noise, low-dropout regulator (LDO) to provide an ultralow-noise power supply that delivers QuietSupply rails to noise-sensitive applications.

The TPS54122-Q1 is ideally suited for systems with 5-V power busses and can support 3-A continuous output current on both the dc-dc or LDO output. The LDO output voltage can be set from 0.8 V to 3.6 V and the dc-dc can be adjusted from 0.83 V to 5.0 V using external resistors. The TPS54122-Q1 can be used in a wide range of low-noise applications because the dc-dc converter and LDO are completely configurable. In addition, the TPS54122-Q1 includes features such as soft-start, switching frequency synchronization, and a power-good signal.

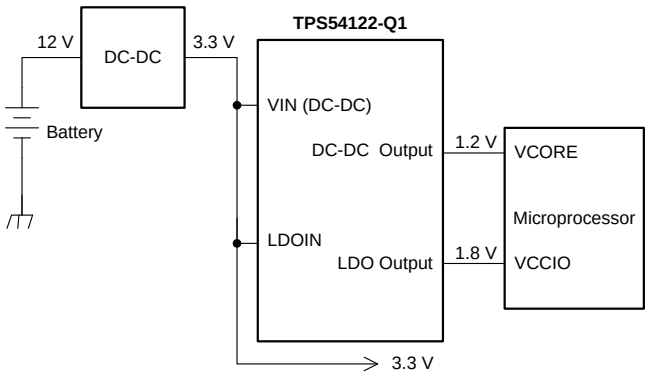
The TPS54122-Q1 can also be configured as a dual-supply rail device, supplying a total of 3 A.

The TPS54122-Q1 is available in a space-saving, 3.5-mm × 5.5-mm VQFN package, and is specified to operate over a –40°C to 125°C ambient temperature range. The TPS54122-Q1 is suited for automotive applications because the device is qualified for AEC-Q100 grade 1.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54122-Q1	VQFN (24)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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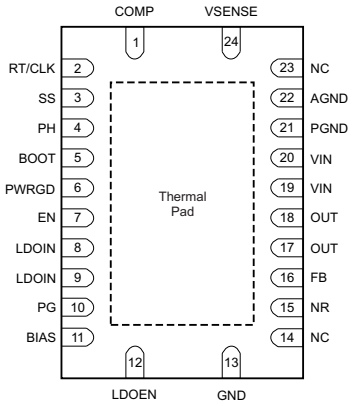
• Released to production	1

5 Pin Configuration and Functions

RHL Package
VQFN-24
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	22	—	Ground return for dc-dc control circuitry of the dc-dc converter
BIAS	11	—	Bias input supply to the LDO error amplifier and reference
BOOT	5	—	A bootstrap capacitor is required between the BOOT and PH pins. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of the dc-dc converter.
COMP	1	O	Input to the output switch current comparator and dc-dc error amplifier output. Connect the external compensation to this pin.
EN	7	I	Enable pin for dc-dc converter. This pin can be left floating to enable the device or can be used with two external resistors to set the undervoltage lockout threshold.
FB	16	I	This pin is the input to the control-loop error amplifier of the LDO and is used to set its output voltage.
GND	13	—	LDO ground
LDOEN	12	I	Enable pin for the LDO. Note that the LDOEN pin must not be left floating; connect this pin to LDOIN if not used.
LDOIN	8, 9	I	LDO input
NC	14, 23	—	No internal connection, can be left floating or connected as needed.
NR	15	—	LDO noise reduction pin. Connect an external capacitor between this pin and LDO ground to reduce output noise and set the V_{OUT} ramp rate of the LDO.
OUT	17, 18	O	LDO output. A 1-µF or larger capacitor is required for stability.
PG	10	O	Open-drain, power-good fault pin of the LDO. Asserts low as a result of thermal shutdown, undervoltage, LDOEN shutdown, or during a slow start of the LDO. If not used, this pin can be left open or grounded.
PGND	21	—	Return for the dc-dc control circuitry and low-side power MOSFET of the dc-dc converter.
PH	4	O	DC-DC converter switch node; connect the inductor and boot capacitor to this pin.
PWRGD	6	O	Open-drain, power-good fault pin of the dc-dc converter. Asserts low as a result of thermal shutdown, undervoltage, overvoltage, EN pin shutdown, or during a soft-start of the dc-dc converter.
RT/CLK	2	I	In RT mode, adding an external timing resistor to this pin adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock signal.
SS	3	I	Soft-start pin. Connect an external capacitor to this pin to set the internal reference voltage rise time for the dc-dc converter. The voltage on this pin overrides the dc-dc converter internal reference.
VIN	19, 20	I	Supplies the power and control circuitry of the dc-dc converter. Use at least a 4.7-µF ceramic capacitor for decoupling.
VSENSE	24	I	Inverting input of the g_M error amplifier of the dc-dc converter.
Thermal pad		—	GND; for best noise and thermal performance, connect the thermal pad to GND and to a large printed circuit board (PCB) ground pad for thermal dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, EN, PWRGD	–0.3	7	V
	PH	–0.6	7	V
	PH (10-ns transient)	–2	10	V
	BOOT	–0.3	PH + 7	V
	BOOT – PH	0	7	V
	LDOIN, LDOEN, BIAS, PG, NR, FB, RT/CLK	–0.3	6	V
	OUT	–0.3	V_{LDOIN} + 0.3	V
	VSENSE, COMP, SS	–0.3	3	V
Current	OUT	Internally limited		A
	RT/CLK, EN, SS	–100	100	µA
	PH	Internally limited		A
	PVIN	Internally limited		A
	COMP	–100	100	µA
	PWRGD (sinking)	–0.1	10	mA
Temperature	Storage, T_{stg}	–55	150	°C
	Operating junction, T_J	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±1000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 2, 11, 12, 13, 14, 23, and 24)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage range	VIN	2.95		6	V
		BIAS	2.375		5.5	V
		LDOIN	$V_O + V_{DO(LDOIN)}$		5.5	V
		EN	0		6	V
		LDOEN	0		5.5	V
$I_{(OUTDC-DC)}$	DC-DC output current		0		3	A
$V_{(OUTLDO)}$	LDO output voltage		V_{FB}		3.6	V
$I_{(OUTLDO)}$	LDO output current		0		3	A
T_A, T_J	Operating free-air temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS54122-Q1 RHL (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	39.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	13.6	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J , T_A= –40°C to 125°C, V_{BIAS} = V_{VIN} = 5 V, V_{LDOIN} = DC-DC_OUT(1) = 2.1 V, V_{LDOEN} = 1.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, and C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{VIN}	VIN pin input voltage range		2.95		6	V
	UVLO threshold			2.6	2.8	V
$I_{SD(VIN)}$	VIN pin shutdown current	V_{EN} < 0.3 V		2		µA
$I_{(OP)}$	VIN pin operating current (no switching)	V_{VSENSE} = 900 mV		360	575	µA
DC-DC BOOT (BOOT PIN)						
	(V_{BOOT} – V_{PH}) UVLO			2.2		V
	Boot charge resistance	V_{EN} = 3 V		16		Ω
DC-DC CONVERTER ENABLE (EN PIN)						
$V_{IL(EN)}$	EN pin low-level input voltage	Falling		1.18		V
$V_{IH(EN)}$	EN pin high-level input voltage	Rising		1.25		V
I_{EN}	EN pin input current	V_{EN} = 1.13 V		1.2		µA
		V_{EN} = 1.3 V		4.6		µA
DC-DC CONVERTER VOLTAGE REFERENCE						
V_{ref}	Reference voltage	2.95 V ≤ V_{VIN} ≤ 6 V	0.802	0.827	0.852	V
DC-DC MOSFET						
R_{HS}	High-side switch resistance	V_{BOOT} – V_{PH} = 5 V		45	81	mΩ
		V_{BOOT} – V_{PH} = 2.95 V		64	110	mΩ
R_{LS}	Low-side switch resistance	V_{VIN} = 5 V		42	81	mΩ
		V_{VIN} = 2.95 V		59	110	mΩ
DC-DC ERROR AMPLIFIER						
I_{IN}	Input current	V_{EN} = 3 V		7		nA
g_M	Error amplifier transconductance	–2 µA ≤ I_{COMP} ≤ 2 µA, V_{COMP} = 1 V		245		µMho
	Error amplifier transconductance during slow-start operation	–2 µA ≤ I_{COMP} ≤ 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		79		µMho
I_{COMP}	Error amplifier output current	V_{COMP} = 1 V, 100-mV input overdrive		±20		µA
	COMP pin to I_{SWITCH} g_M			18		A/V
DC-DC CURRENT LIMIT						
	High-side current limit	V_{VIN} = 3 V	4.2	6.6		A
DC-DC SOFT-START (SS PIN)						
	SS pin charge current	V_{SS} = 0.4 V		2.2		µA
	SS pin to VSENSE pin matching	V_{SS} = 0.4 V		35		mV

(1) DC-DC_OUT refers to the regulated output voltage of the switching regulator (see Figure 27).

Electrical Characteristics (continued)

At T_J , T_A= –40°C to 125°C, V_{BIAS} = V_{VIN} = 5 V, V_{LDOIN} = DC-DC_OUT(1) = 2.1 V, V_{LDOEN} = 1.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, and C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC POWER GOOD (PWRGD PIN)						
	VSENSE pin threshold	VSENSE falling (fault)		0.91 V_{ref}		V
		VSENSE rising (good)		0.93 V_{ref}		V
		VSENSE rising (fault)		1.07 V_{ref}		V
		VSENSE falling (good)		1.05 V_{ref}		V
	High-level output leakage current	V_{VSENSE} = V_{ref}, V_{PWRGD} = 5.5 V, V_{EN} = 3 V		2		nA
	Low-level output voltage	I_{PWRGD} = 3 mA		0.3	0.6	V
	Minimum VIN voltage for valid output	V_{PWRGD} < 0.5 V at 100 µA		1.2	1.6	V
LDO						
V_{LDOIN}	LDO input voltage range		V_O + V_{DO}		5.5	V
V_{BIAS}	LDO bias input voltage range		2.375		5.5	V
V_{FB}	FB pin voltage	T_A = 25°C	0.796	0.8	0.804	V
V_O	OUT pin voltage range		V_{FB}		3.6	V
	OUT pin voltage accuracy	V_O = V_{FB}, 50 mA ≤ I_O < 3 A, 2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{LDOIN} ≥ $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} ≥ $V_{OUT(nom)}$ + 1.62 V	–1.0%	±0.2%	1.0%	
$\Delta V_{O(\Delta IL)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 3 A		0.03		%/A
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 V ≤ V_{LDOIN} ≤ 5.5 V		0.0005	0.06	%/V
$V_{DO(LDOIN)}$	V_{LDOIN} dropout voltage	I_O ≤ 3.0 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62 V		100	200	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage	I_O ≤ 3.0 A, V_{LDOIN} = V_{BIAS}			1.62	V
I_{LIM}	Output current limit	V_O = 0.8 × $V_{OUT(nom)}$	3.8		6.0	A
I_{BIAS}	BIAS pin current			2	4	mA
$I_{SD(LDO)}$	Shutdown current (I_{BIAS})	V_{EN} < 0.4 V		1	100	µA
I_{FB}	FB pin current		–250	95	250	nA
I_{LDOEN}	LDOEN pin input current	V_{EN} = 5 V		0.1	1	µA
$V_{IL(LDOEN)}$	LDOEN pin low-level input voltage (disable)				0.4	V
$V_{IH(LDOEN)}$	LDOEN pin high-level input voltage (enable)		1.1			V
	PG pin trip threshold	V_{FB} decreasing	0.86 V_{FB}	0.90 V_{FB}	0.94 V_{FB}	V
	PG pin trip hysteresis			0.03 V_{FB}		V
	High-level output leakage current	V_{PG} = 5.25 V		0.03	1	µA
	Low-level output voltage	I_{PG} = 1 mA			0.3	V
I_{NR}	NR pin charging current	V_{NR} = 0.4 V	0.5	0.73	1	µA
THERMAL SHUTDOWN						
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C
NOISE						
V_n	Output noise voltage	BW = 10 Hz to 1 MHz, C_{NR} = 10 µF, C_{FB} = 0.1 µF, I_O = 1 A , C_{OUT} = 100 µF		17		μV_{RMS}

6.6 Timing Requirements

at V_{BIAS} = V_{VIN} = 5 V, and T_J , T_A= –40°C to 125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Minimum on-time	Measured at 50% points on PH, I_O = 3 A		65		ns
		Measured at 50% points on PH, I_O = 0 A		120		ns
	Minimum off-time	Prior to skipping off pulses, V_{BOOT} – V_{PH} = 2.95 V, I_O = 3 A		60		ns
t_R	Rise time	V_{VIN} = 5 V, I_O = 3 A		2.5		V/ns
t_F	Fall time	V_{VIN} = 5 V, I_O = 3 A		2		V/ns

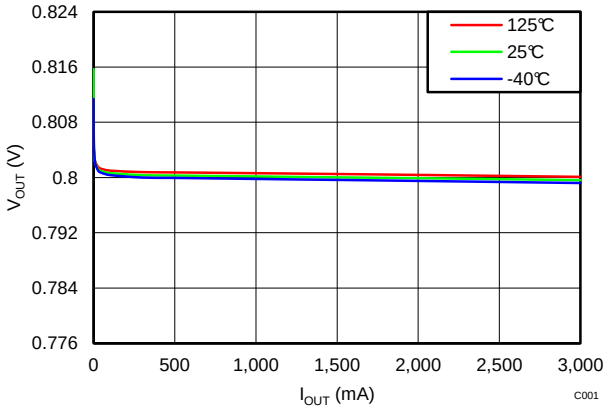
6.7 Switching Characteristics

at V_{BIAS} = V_{VIN} = 5 V, and T_J , T_A= –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching frequency range (RT mode set point and PLL mode)		300		2000	kHz
Switching frequency	R_{RT} = 400 kΩ (1%)	400	500	600	kHz
Switching frequency range in CLK mode		300		2000	kHz
RT/CLK pin high threshold				2.2	V
RT/CLK pin low threshold		0.4			V
PLL lock-in time			14		µs
RT/CLK pin falling edge to PH pin rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns

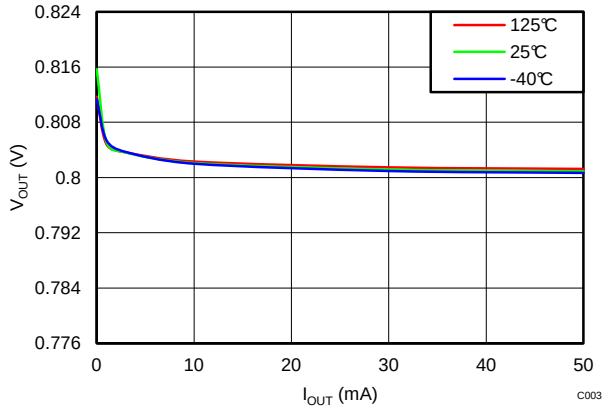
6.8 Typical Characteristics

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.



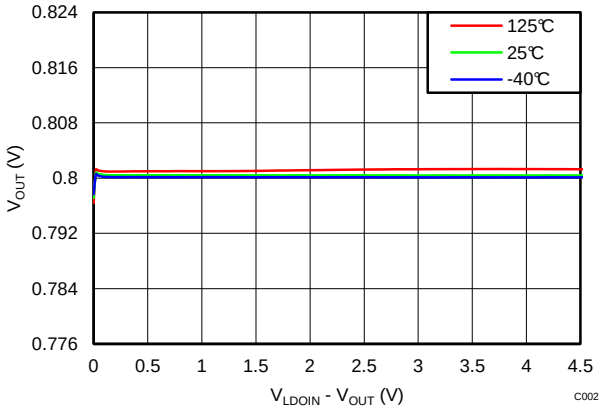
NOTE: Y-axis shows a 1% V_{OUT} per division.

Figure 1. Load Regulation



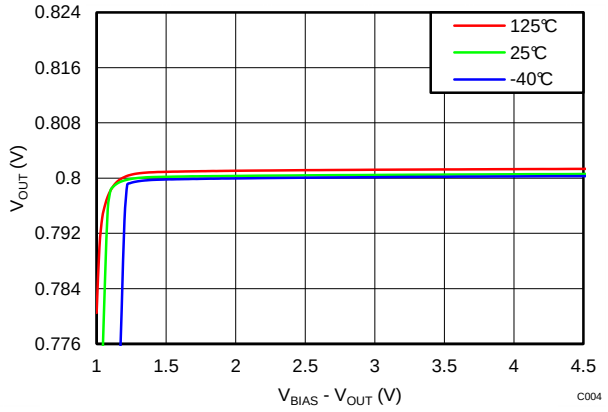
NOTE: Y-axis shows a 1% V_{OUT} per division.

Figure 2. Load Regulation Under Light Loads



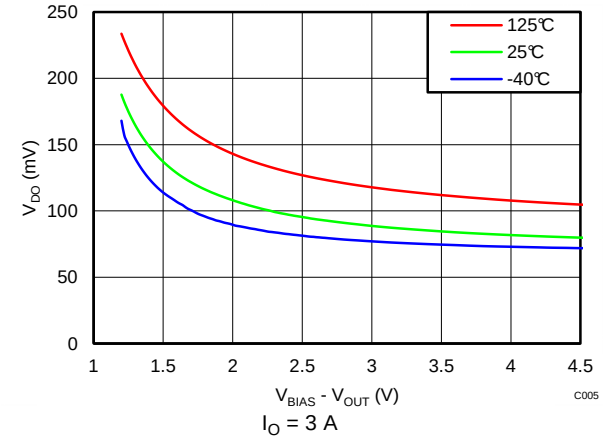
NOTE: Y-axis shows a 1% V_{OUT} per division.

Figure 3. LDOIN Line Regulation



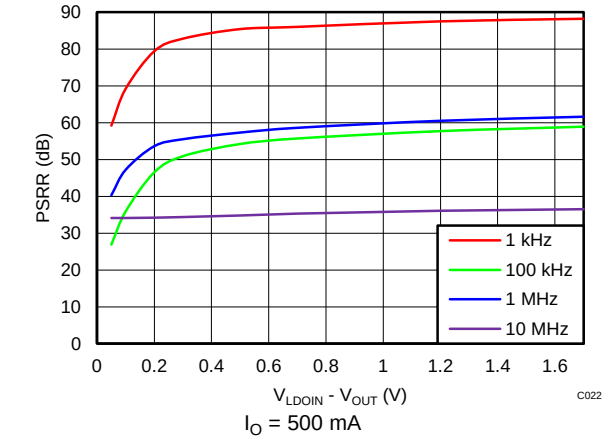
NOTE: Y-axis shows a 1% V_{OUT} per division.

Figure 4. LDO Bias Line Regulation



I_O = 3 A

Figure 5. LDO Dropout Voltage vs LDO Bias Voltage

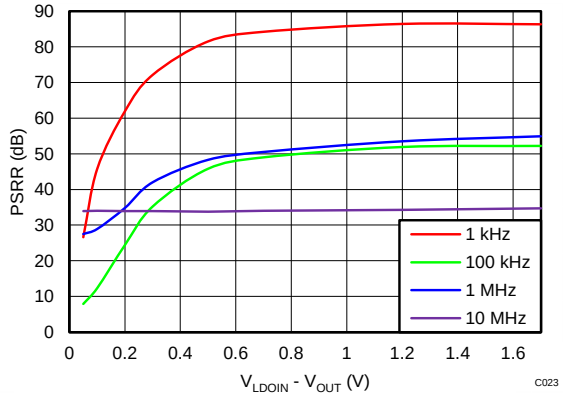


I_O = 500 mA

Figure 6. LDO Power-Supply Ripple Rejection vs LDO Dropout Voltage

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.



I_O = 3 A

Figure 7. LDO Power-Supply Ripple Rejection vs LDO Dropout Voltage

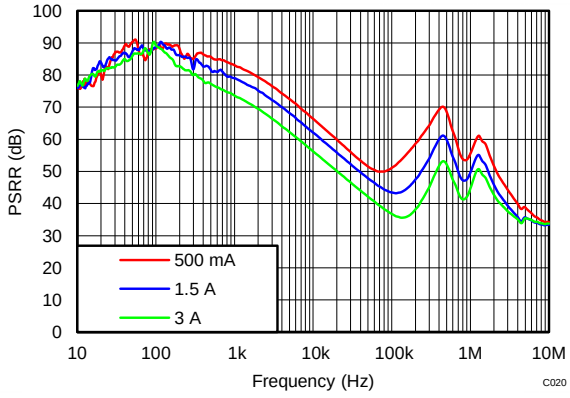
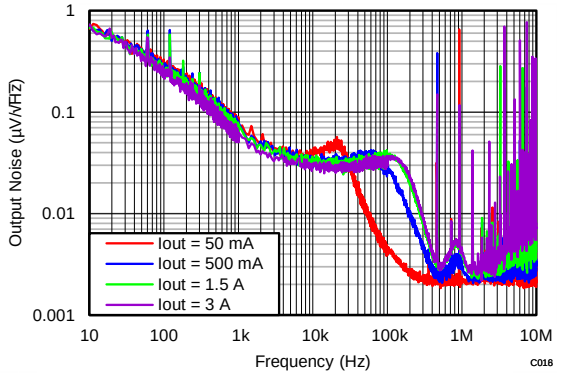
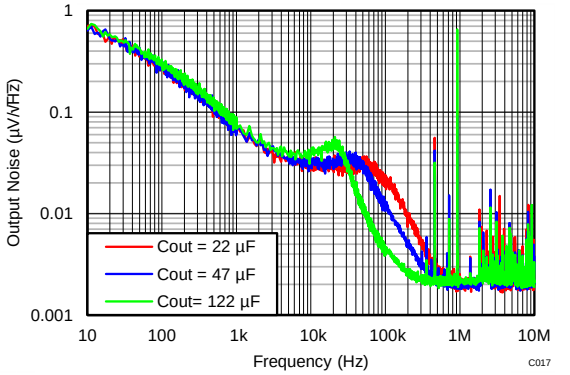


Figure 8. LDO Power-Supply Ripple Rejection vs Frequency



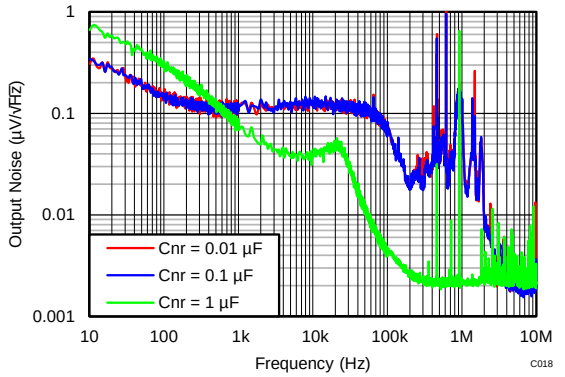
C_{OUT} = 122 µF, C_{NR} = 1 µF, RMS noise = 100 Hz to 100 kHz, 50-mA I_O = 9 μV_{RMS}, 500-mA I_O = 11 μV_{RMS}, 1.5-A I_O = 11 μV_{RMS}, 3-A I_O = 10 μV_{RMS}

Figure 9. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)



C_{NR} = 1 µF, RMS noise = 100 Hz to 100 kHz, 22-µF C_{OUT} = 10 μV_{RMS}, 47-µF C_{OUT} = 9 μV_{RMS}, 122-µF C_{OUT} = 9 μV_{RMS}

Figure 10. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)



C_{OUT} = 122 µF, RMS noise = 100 Hz to 100 kHz, 0.01-µF C_{NR} = 33 μV_{RMS}, 0.1-µF C_{NR} = 33 μV_{RMS}, 1-µF C_{NR} = 9 μV_{RMS}

Figure 11. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)

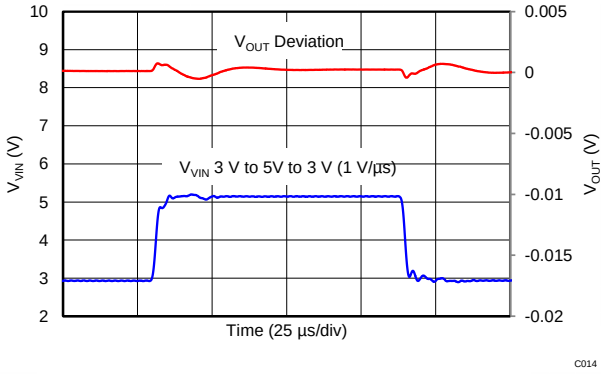


Figure 12. LDO Line Transient Response

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.

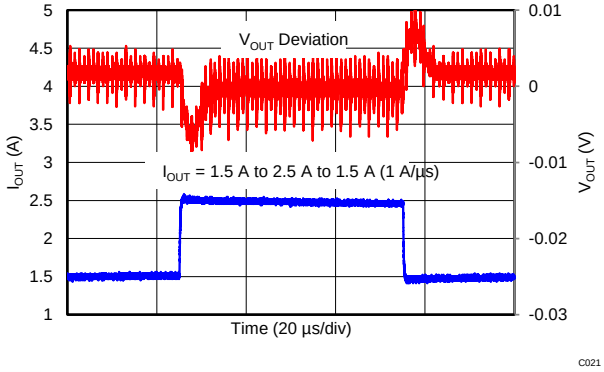
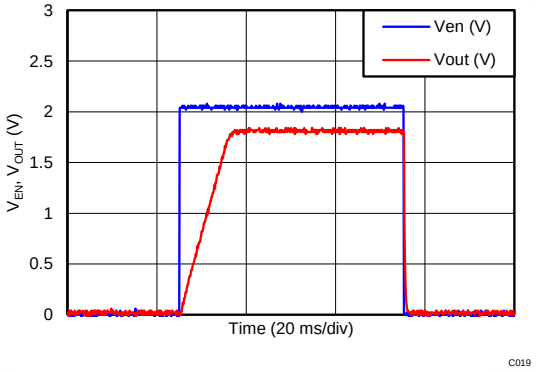
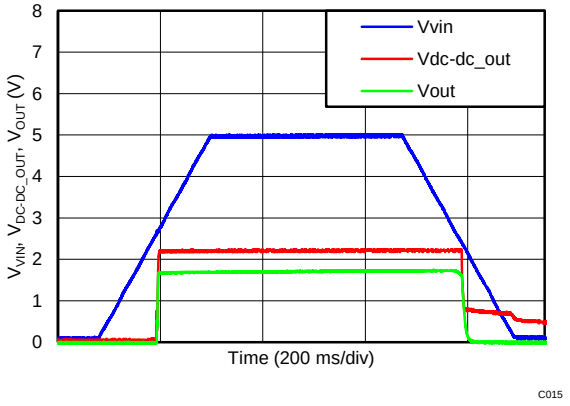


Figure 13. DC-DC Load Transient Response



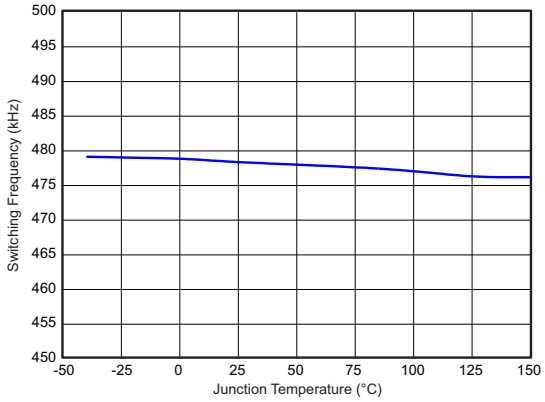
R_{LOAD} = 1.8 Ω

Figure 14. LDO Enable Pulse Response



V_{EN} = V_{VIN}, V_{LDOEN} = V_{DC-DC_OUT}

Figure 15. Power-Up and Power-Down Response (LDO Powered by DC-DC)



RT = 400 kΩ, V_I = 5 V

Figure 16. DC-DC Switching Frequency vs Temperature

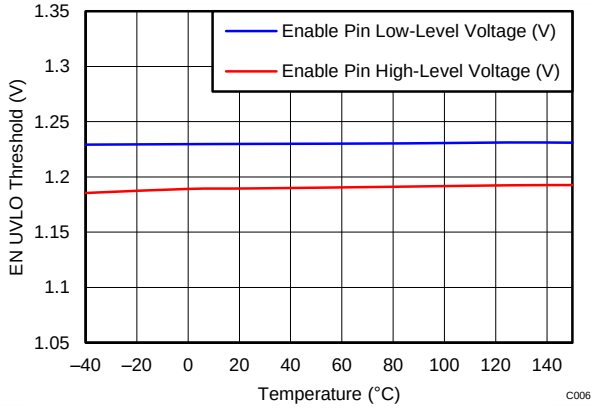


Figure 17. DC-DC EN UVLO Threshold vs Temperature

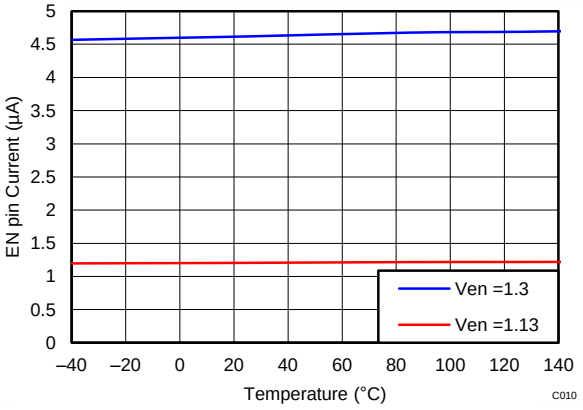


Figure 18. Enable Pin Current vs Temperature

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.

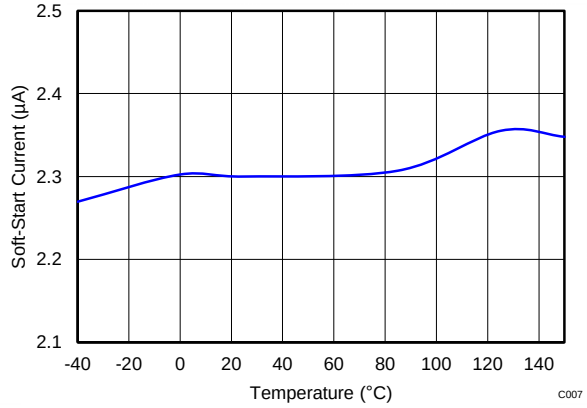


Figure 19. DC-DC Soft-Start Current vs Temperature

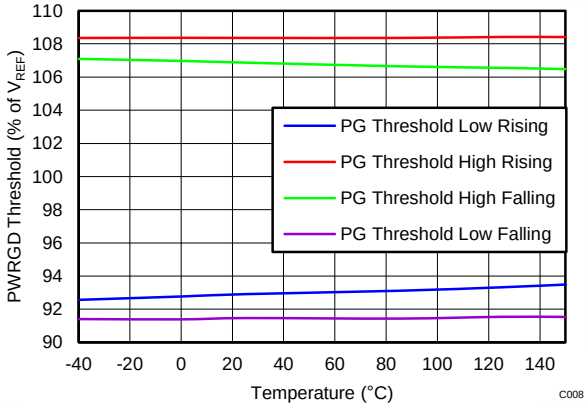


Figure 20. LDO PG Threshold vs Temperature

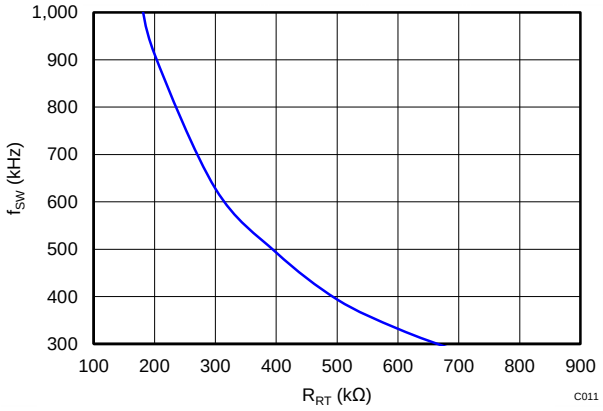


Figure 21. DC-DC Switching Frequency vs R_{RT}

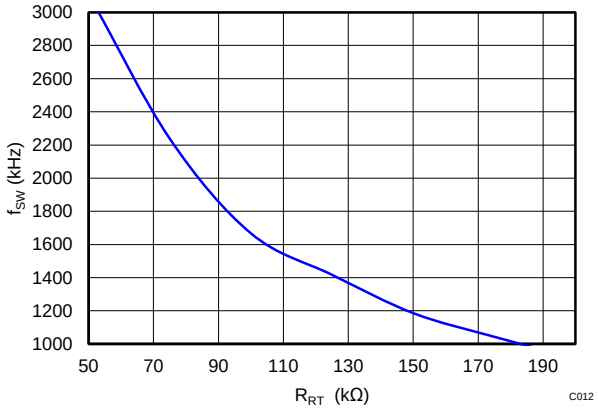


Figure 22. DC-DC Switching Frequency vs R_{RT}

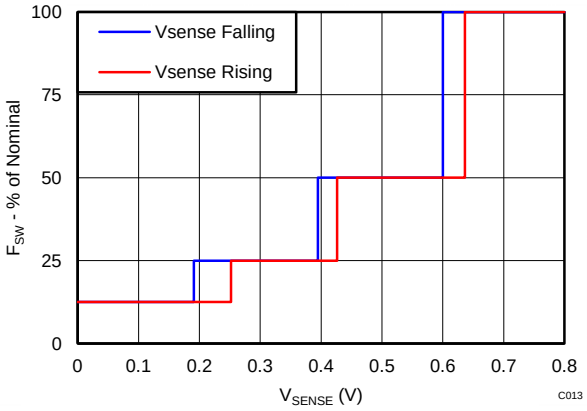


Figure 23. Switching Frequency vs V_{SENSE}

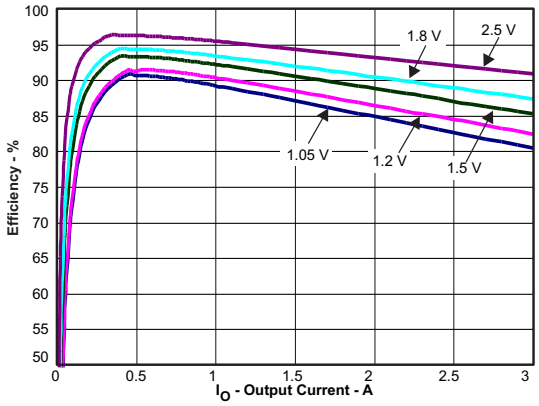


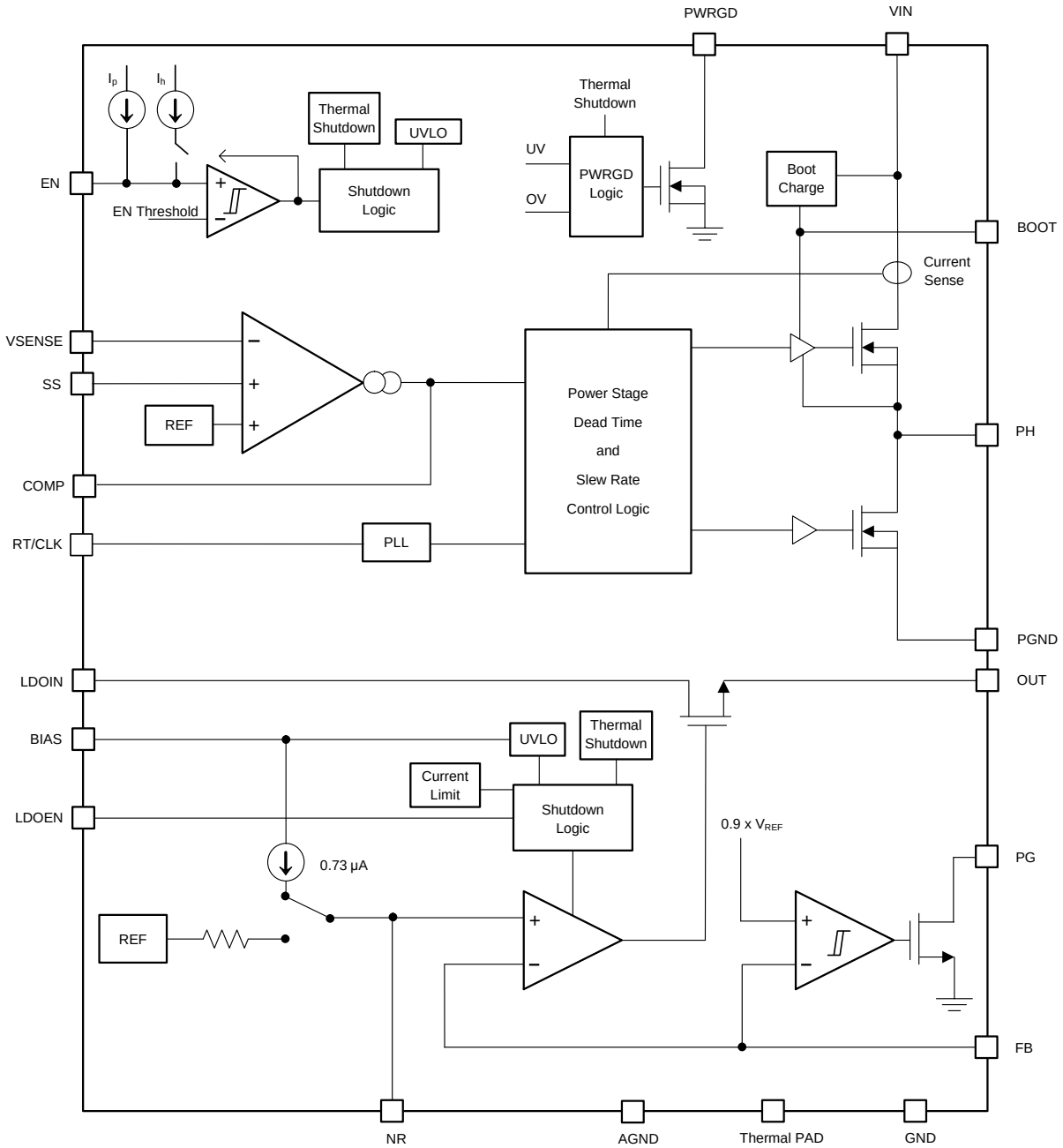
Figure 24. DC-DC Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPS54122-Q1 is a low-noise power supply that delivers a quiet power rail to noise-sensitive components. This device combines a current-mode-controlled, dc-dc, step-down regulator, and a low-noise, wide-bandwidth, low-dropout regulator (LDO) to create an efficient, stable, low-noise power supply. The TPS54122-Q1 is fully characterized for noise performance, thus allowing for easy creation of a quiet power supply. The device includes features such as soft-start, clock synchronization, and a power-good signal, making the TPS54122-Q1 well suited as a power supply for communication, test and measurement, and audio-equipment applications. Both the integrated switching regulator and LDO are fully configurable, allowing for complete design flexibility.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range

7.3.1.1 DC-DC Input Voltage (VIN)

The TPS54122-Q1 VIN pin provides power to both the dc-dc control circuitry as well as the dc-dc power stage. Use a voltage divider connected from the VIN pin to the EN pin to set an undervoltage lockout (UVLO) for the dc-dc regulator to provide consistent power-up behavior; see the *Device Enable and Undervoltage Lockout Adjustment* section for more information. Decouple this pin to PGND with a 4.7-µF ceramic capacitor.

7.3.1.2 LDO Input Voltage (LDOIN)

The LDOIN pin provides power to the pass device of the LDO. The minimum input operating voltage that can be applied to the LDOIN pin of the TPS54122-Q1 is $V_{LDOIN} = [V_{OUT} + V_{DO}]$. The voltage into this pin must not exceed 6.0 V. This pin is designed to be connected to the output inductor of the integrated switcher; decouple this pin to the GND pin with a 1.0-µF ceramic capacitor.

7.3.1.3 LDO Bias Input Voltage (BIAS)

The BIAS pin provides power to the control circuitry of the LDO. The BIAS voltage requires additional voltage headroom over the LDOIN voltage to allow the control circuitry to operate the N-channel pass device. The minimum input operating voltage that can be applied to the BIAS pin is 2.375 V, or V_{OUT} + 1.62 V, whichever is greater. Therefore, when V_{OUT} = 1.5 V, LDOIN can be set as low as 1.8 V and BIAS can be set to 3.3 V, ±5%. In the majority of applications, the BIAS pin can be connected to the VIN pin of the TPS54122-Q1.

7.3.2 Dual Adjustable Output Voltages

The output voltage of both the switcher and the LDO are adjustable. The output voltages are set with a resistor divider from the output voltage to the feedback sensing pins (VSENSE or FB). Use 1% tolerance or better divider resistors for best accuracy.

The values of the LDO feedback resistors can be calculated using Equation 1:

$$R_1 = (V_{OUT} / V_{ref} – 1) \times R_2 \quad (1)$$

where:

- V_{ref} = 0.8 V,
- R_1 = the resistor from the output to the FB pin of the LDO, and
- R_2 = the resistor from the FB pin to ground of the LDO.

The values of the switching regulator feedback resistors can be calculated using Equation 2:

$$R_5 = (DC\text{-}DC\_OUT / V_{ref}) \times R_6 \quad (2)$$

where:

- V_{ref} = 0.827 V,
- R_5 = the resistor from the switcher output at the inductor to the VSENSE pin, and
- R_6 = the resistor from the VSENSE pin to the ground-switching regulator.

To improve efficiency at light loads, consider using larger-value resistors. Larger-value resistors increase the noise sensitivity at the VSENSE and FB pins and error from the VSENSE and FB pin input currents. Using a value of 10 kΩ for R_1 and R_5 provides a good trade-off between noise and light load efficiency.

7.3.3 Power Conversion Efficiency versus Output Noise

The configuration of the TPS54122-Q1 consists of a switching regulator followed by an LDO. The ability of the LDO to reject noise created by the switching regulator and instead of passing the noise to the LDO output is determined by the power-supply rejection (PSR) of the LDO. The PSR of an LDO depends on the LDO input to LDO output voltage difference. The higher the voltage difference, the better the LDO ability to reject noise at its input. The LDO in the TPS54122-Q1 is designed to provide high, wide-bandwidth PSR with a minimum of input-to-output voltage differential. At 3 A for the highest PSR performance, set the input-to-output voltage differential to 0.5 V or greater.

Feature Description (continued)

The LDO input-to-output voltage differential is also a primary contributor to the overall power loss in the TPS54122-Q1. The contribution of the LDO input and output voltage differentials to the power loss is defined as the output current multiplied by the input-to-output voltage differential, as shown in Equation 3:

$$\text{Power Loss from the LDO} = I_{OUT} \times [V_{LDOIN} - V_{OUT}] \quad (3)$$

Therefore, for a 0.5-V drop at 1.5 A, this loss is 0.75 W. Reduce the impact of the power loss by lowering $V_{LDOIN} - V_{OUT}$. In the *Typical Characteristics* section, Figure 6 and Figure 7 illustrate the trade-off between PSR and $V_{LDOIN} - V_O$ for various output current levels and frequencies. For currents less than 1 A, a $V_{LDOIN} - V_O$ of 0.3 V does not have significant impact on PSR performance and provides a substantial improvement to the power loss from the $V_{LDOIN} - V_O$.

7.3.4 DC-DC Output Overvoltage Transient Protection (OVTP)

The TPS54122-Q1 has an overvoltage transient protection (OVTP) circuit on the dc-dc switcher output to minimize overshoots on the dc-dc switcher output. This circuit also protects the input of the LDO from experiencing overshoot above its rated values.

CAUTION

Any voltage above the absolute maximum rated input voltage into the LDOIN pin can damage the device.

The OVTP feature minimizes overshoot by comparing the VSENSE pin voltage to the OVTP threshold (107% of the dc-dc V_{ref}). If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops below the OVTP threshold, the high-side MOSFET is enabled at the next clock cycle.

7.3.5 Overcurrent Protection

The TPS54122-Q1 provides multiple forms of overcurrent protection, as discussed in this section.

7.3.5.1 Switcher Overcurrent Protection

The integrated switcher of the TPS54122-Q1 is protected from overcurrent conditions by using a cycle-by-cycle current limit. During each switching cycle, the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current crosses the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current until the error amplifier output reaches the internally clamped voltage, which then functions as the switch current limit.

7.3.5.1.1 Frequency Division

In addition to a current limit on the high-side switch, the TPS54122-Q1 implements a switching-frequency division technique to allow the low-side MOSFET to be turned off long enough to reduce the current in the inductor to prevent current runaway. During an overcurrent condition, the frequency division reduces the frequency from 100% to 50%, then to 25%, and finally to 12.5%. The overcurrent condition is detected by the decreasing voltage on the VSENSE pin. Figure 23 in the *Typical Characteristics* section illustrates the reduction in frequency based on the VSENSE voltage reduction. During startup, the switching frequency increases corresponding to the voltage on the VSENSE pin increasing from 0 V to 0.827 V.

7.3.5.1.2 Reverse Overcurrent Protection for the Low-Side FET

The TPS54122-Q1 implements low-side current protection by detecting the voltage drop across the low-side MOSFET. When the dc-dc converter sinks current through the low-side MOSFET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 2 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into prebiased outputs.

Feature Description (continued)

7.3.5.2 LDO Internal Current Limit

In addition to the switcher overcurrent protection, the TPS54122-Q1 has an internal current limit on the integrated LDO. The LDO internal current limit helps protect the LDO during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time. The NMOS pass element in the integrated LDO has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at LDOIN. This current is not limited and can damage the LDO, so if extended reverse-voltage operation is anticipated, external limiting is required. Connect a diode from OUT to LDOIN to provide an alternate path for this current.

7.3.6 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes: RT and CLK.

7.3.6.1 RT Mode

In RT mode, the $R_{(RT)}$ resistor is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 300 kHz to 2 MHz by using a maximum $R_{(RT)}$ value of 700 kΩ and a minimum value of 85 kΩ, respectively. To determine the value of the RT resistor for a given switching frequency (f_{SW}), use Equation 4 or the curves in Figure 21 or Figure 22:

$$R_{(RT)}\ (k\Omega) = 311890\ f_{SW}^{\ -1.0793}\ (kHz) \quad (4)$$

7.3.6.2 CLK Mode

In CLK mode, an external clock is connected directly to the RT/CLK pin. The dc-dc converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The dc-dc converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 300 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 75 ns. The clock signal amplitude must transition to less than 0.6 V and to greater than 1.6 V. The PH rising edge is synchronized to the RT/CLK pin falling edge.

In applications where both RT mode and CLK mode are required, the device can be configured to have both an RT resistor and an external clock connected at the same time to the RT/CLK pin. If no external clock is present, the device functions in RT mode and the switching frequency is set by the $R_{(RT)}$ resistor. The first time the SYNC pin is pulled above the RT/CLK high threshold (1.6 V), the device switches from RT mode to CLK mode, and the RT/CLK pin becomes high impedance when the PLL starts to lock on to the frequency of the external clock. After the clocking edges stop, the internal clocking circuitry is re-enabled, and the frequency returns to the switching frequency set by the $R_{(RT)}$ resistor.

7.3.7 Start-Up Time

The TPS54122-Q1 has start-up time control for both the LDO and the dc-dc converter.

7.3.7.1 Soft-Start of the DC-DC Converter

The rate at which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin. The C_{SS} capacitor is connected between the SS pin and ground. The size of the capacitor determines the soft-start ramp-up time (t_{ss}, 10% to 90%), as shown in Equation 5:

$$t_{SS}\ (ms) = C_{SS}\ (nF) \times V_{ref}\ (V) / I_{SS}\ (\mu A) \quad (5)$$

The device has an internal pull-up current source (I_{SS}) of 2.2 µA that charges the external soft-start capacitor, C_{SS}. The voltage reference, V_{ref}, for this device is 0.827 V. By sourcing a constant current onto the capacitor, the device linearly ramps up the voltage on the SS pin that corresponds to the voltage on the FB pin, and thus, the output voltage of the switcher. When the voltage on the SS pin exceeds the value of the internal reference, the device starts regulating to the internal reference value.

If the input UVLO is triggered (or the EN pin is pulled below 1.21 V or a thermal shutdown event occurs), then the device stops switching and enters low-current operation. At the subsequent power-up when the shutdown condition is removed, the dc-dc does not start switching until the SS pin is discharged to ground, ensuring proper soft-start behavior.

Feature Description (continued)

7.3.7.2 NR Soft-Start Time and LDO Start-Up

The primary purpose of the NR capacitor is to filter the noise from the LDO band gap and thereby reduce the LDO output noise. However, the NR capacitor also affects the start-up time of the LDO. The TPS54122-Q1 has a soft-start circuit to charge C_{NR} at a controlled rate for a monotonic soft-start. The controlled voltage ramp of the output also reduces peak inrush current during start-up.

The soft-start ramp time depends on the soft-start charging current ($I_{(NR)}$), the external noise-reduction capacitor (C_{NR}), and the internal voltage reference of the LDO, and can be calculated as shown in Equation 6:

$$t_{SS}\ (ms) = 1{,}096 \times C_{NR}\ (F) \quad (6)$$

7.3.8 Power-Good Indicators

7.3.8.1 Switcher Power Good (PWRGD)

The PWRGD pin is an open-drain output. After the VSENSE pin rises above 93% or falls below 105% of the internal voltage reference, the PWRGD pin pull-down transistor is deasserted and the pin floats, indicating a correct output voltage on the dc-dc converter. The PWRGD pin has a 2% hysteresis, so it does not pull down until the VSENSE pin falls below 91% or rises above 107% of the internal voltage reference, indicating an out-of-range output voltage. Use a 1-kΩ to 100-kΩ pull-up resistor to a voltage source that is less than or equal to 6 V. The PWRGD pin is in a defined state after the VIN input voltage exceeds 1.2 V.

The PWRGD pin is also pulled low if the input UVLO or thermal shutdown are asserted, or if the EN pin is pulled low.

7.3.8.2 LDO Power Good (PG)

The power-good (PG) pin of the LDO is an open-drain output and can be connected to any 5.5 V or lower voltage rail through an external pull-up resistor. This pin requires at least 1.1 V on the BIAS pin in order to have a valid output. At power-on, the PG output becomes high-impedance when V_{OUT} is greater than 93% of the set output voltage. If V_{OUT} falls below 90% of the set output voltage or if the BIAS pin voltage falls below 1.9 V, the open-drain turns on and pulls the PG output low. The PG pin also pulls low when the LDO is disabled. The recommended range for the PG pull-up resistor is from 10 kΩ to 1 MΩ.

7.3.9 Device Enable and Undervoltage Lockout Adjustment

The TPS54122-Q1 provides an independent device enable and undervoltage lockout. The dc-dc converter also provides undervoltage lockout adjustment for the dc-dc converter.

Feature Description (continued)

7.3.9.1 Switcher Enable and Undervoltage Lockout

Use the EN pin to turn the switcher on and off. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low I_Q state.

The EN pin has an internal pull-up current source; float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The TPS54122-Q1 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold (typically, 2.6 V). If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 25.

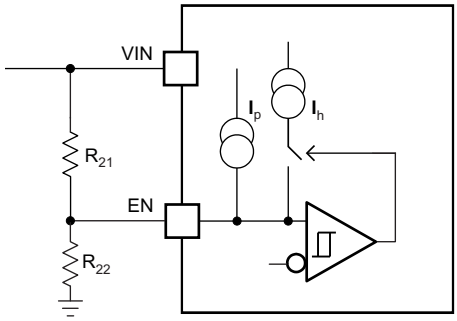


Figure 25. Adjustable VIN Undervoltage Lockout

The EN pin has a small pull-up current (I_p) that sets the state of the pin to enable (default) when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 7 and Equation 8.

$$R_{21} = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1-\frac{V_{ENFALLING}}{V_{ENRISING}}\right)+I_h} \quad (7)$$

$$R_{22} = \frac{R1\times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (8)$$

where:

- V_{START} is the start-up voltage for the dc-dc converter,
- V_{STOP} is the shutdown voltage for the dc-dc converter,
- $V_{ENFALLING}$ = 1.18 V,
- $V_{ENRISING}$ = 1.25 V,
- I_p = 1.2 µA, and
- I_h = 4.6 µA.

7.3.9.2 LDO Enable (LDOEN) and Undervoltage Lockout

The TPS54122-Q1 LDO enable pin (LDOEN) is active high and compatible with standard digital-signaling levels. The LDOEN pin has hysteresis and deglitching (typically, 50 mV) that allow LDOEN to be used with relatively slow-ramping analog signals, such as an upstream power supply. Typical sequencing applications can be implemented using the TPS54122-Q1 dc-dc output or PG, or the output of another power supply. When shutdown capability is not required, EN can be connected to IN.

The LDO also has a fixed UVLO on the BIAS pin to keep the output shut off until the LDO internal circuitry is working properly.

Feature Description (continued)

7.3.10 Sequencing

The TPS54122-Q1 is easy to use and suited for applications that require tracking and sequencing. The TPS54122-Q1 has a built-in power-good function to indicate device status, a soft-start circuit to control the output voltage slope during start-up, noise reduction with start-up time for the LDO, and an enable function for independently controlling start-up of both the LDO and the switcher. Each of these functions is useful for tracking and sequencing applications.

7.3.11 Switcher Fixed-Frequency PWM Control

The integrated switcher of the TPS54122-Q1 uses adjustable, fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier that drives the COMP pin. An internal oscillator turns on the high-side power switch. The error amplifier output is converted into a current reference that is compared to the high-side power-switch current. When the power-switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The device implements a current limit by clamping the COMP pin voltage to a maximum level. A minimum level clamp is also implemented for improved transient-response performance.

7.3.12 Small-Signal Model for Loop Response

Figure 26 shows an equivalent model for the switcher control loop. This model can be run in a circuit simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a g_M of 245 µA/V, and can be modeled using an ideal, voltage-controlled current source. Resistor R_O and capacitor C_O model the open-loop gain and frequency response of the error amplifier. The 1-mV, ac voltage source between nodes *a* and *b* effectively breaks the control loop for the frequency-response measurements. Plotting a / c shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. The transient response can be checked by replacing R_L with a current source using the appropriate load step, amplitude, and slew rate in a time-domain analysis.

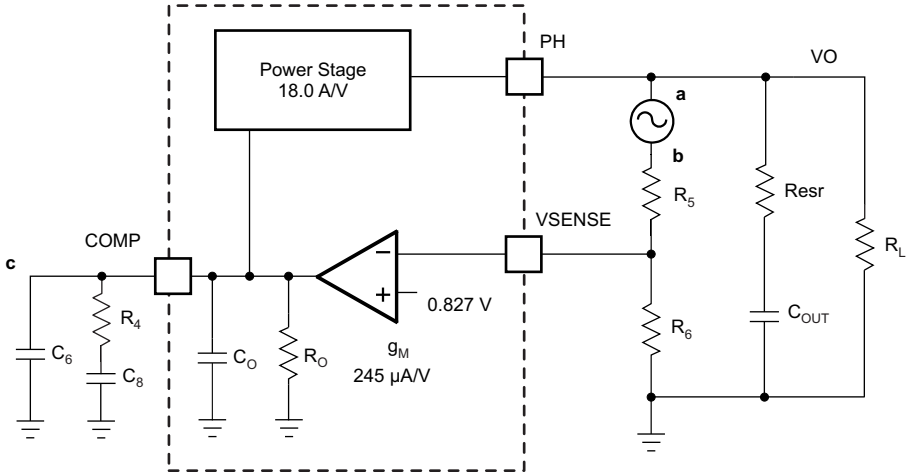


Figure 26. Small-Signal Model for Loop Response

Refer to application report *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a more detailed treatment of the small-signal model and compensation for the TPS54122-Q1.

7.4 Device Functional Modes

7.4.1 Normal Operation

Both the LDO and dc-dc regulate to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage; see the *Dropout Operation* section for additional details.
- The voltage has previously exceeded the enable rising threshold voltage ($V_{LDOEN} > V_{IH(LDOEN)}$) for the LDO and ($V_{EN} > V_{IH(EN)}$) for the dc-dc and has not yet decreased below the enable falling threshold.
- The LDO output current is less than the LDO current limit and the dc-dc peak inductor current is less than the high-side current limit.
- The device junction temperature is less than the thermal shutdown temperature ($T_J < 160°C$).

7.4.2 Dropout Operation

If the input voltage of the LDO (V_{LDOIN}) is lower than the nominal LDO output voltage plus the specified dropout voltage ($V_{DO(LDOIN)}$), but all other conditions are met for normal operation, the LDO operates in input voltage dropout mode. In this mode, the output voltage tracks the input voltage.

The integrated LDO also has a BIAS supply voltage that can cause the output to enter dropout. If the BIAS voltage is lower than the nominal LDO output voltage plus the specified bias supply dropout voltage ($V_{DO(BIAS)}$), but all other conditions are met for normal operation, the LDO operates in bias voltage dropout mode.

When operating in dropout from either the input or bias supply, the transient performance and PSR of the LDO becomes significantly degraded because the pass device is no longer capable or controlling the current through the LDO. Line or load transients on the LDO input in dropout can result in large output-voltage deviations.

The internal dc-dc regulator has an integrated bootstrap-voltage regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than V_{VIN} and the (BOOT – PH) voltage is below regulation. Use a 0.1-µF ceramic capacitor with an X7R- or X5R-grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage provided by these types of capacitors.

To improve dropout, the dc-dc regulator is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. When the voltage between BOOT and PH drops below the 2.2-V UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. The supply current source from the BOOT pin is very low; therefore, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Thus, the effective duty cycle of the switching regulator is nearly 100%.

7.4.3 Disabled

Both the dc-dc regulator and LDO have independent enable pins that enable or disable the output voltage. The LDO output is controlled by the LDOEN pin and the dc-dc output is controlled by the EN pin. The LDO and dc-dc are disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The input voltage is below the UVLO threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Design Methodology

The TPS54122-Q1 has a low-noise output voltage range from 0.8 V to 3.6 V with an output current up to 3 A. To simplify design efforts using the TPS54122-Q1, see Table 1 for a list of designs for common applications according to the schematic diagram illustrated in Figure 27.

The TPS54122-Q1 can also be configured to provide two separate power rails: one from the switching regulator and one from the LDO.

Figure 27 provides a typical application diagram for the TPS54122-Q1. The first step in the design process is to select the switching frequency for the regulator. Higher switching frequencies produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, higher switching frequencies cause additional switching losses that negatively impact converter efficiency and thermal performance.

After a switching frequency is determined, the inductor and output capacitor values of the switcher are selected. These two component values are related to each other and depend on the input and output voltages of the switcher, as well as the current rating. Choosing a high inductor-ripple current also affects the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current.

The TPS54122-Q1 requires a high-quality, ceramic (X5R or X7R type), input decoupling capacitor with a value of at least 4.7 µF on the input voltage rail. The voltage rating of the input capacitor must be greater than the maximum input voltage.

The internal LDO of the TPS54122-Q1 does not require an output capacitor to be stable. However, for best transient and noise performance, use standard ceramic output capacitors with values of 4.7 µF or larger. Higher values are recommended for better noise performance.

For proper operation, connect a 0.1-µF ceramic capacitor between the BOOT and PH pins. Use a ceramic capacitor with an X5R or better grade dielectric, and a 10-V or higher voltage rating.

The output voltage of both the switcher and the LDO are adjustable using an external-resistor feedback network. Also, both the LDO and the switcher have a soft-start function that can be adjusted externally using the C_{SS} and C_{NR} capacitors; see Figure 27.

There are several industry techniques used to compensate dc-dc regulators; refer to application report *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for more details about different compensation networks for the TPS54122-Q1.

Application Information (continued)

8.1.2 Simplified Design Methodology

The TPS54122-Q1 has a low-noise output voltage range from 0.8 V to 3.6 V with an output current up to 3 A. To simplify design efforts using the TPS54122-Q1, the typical designs for common applications are listed in Table 1 based on Figure 27. For the designs shown in Table 1, the values are the closest standard capacitor, inductor, and 1% resistor values. Also, $C_{DC\text{-}DC\_OUT} = C_9 + C_{10}$ and $C_{OUT} = C_2 + C_3 + C_4$. If the LDO input is connected to the output of the dc-dc, the LDO input capacitance must be added to the dc-dc output capacitance. To execute a complete application design, refer to application report *Design Procedures for the TPS54122* (SLVA602). Note that all capacitor values are based on ceramic X5- or X7-type capacitors.

Table 1. Simplified Design Table

V_{VIN} (V)	DC-DC_OUT (V)	LDO V_{OUT} (V)	I_O (max) (A)	f_{SW} (kHz)	L_1 (µH)	$C_{DC\text{-}DC\_OUT}$ (µF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_4 (kΩ)	R_5 (kΩ)	R_6 (kΩ)	C_8 (nF)	C_{OUT} (µF)	C_1 (nF)	C_{11} (pF)
5.0	3.7	3.3	3.0	500	3.3	4 x 22	3.57	1.15	392	28.7	10	2.87	4.7	122	100	1000
5.0	3.6	3.3	1.0	500	3.3	4 x 22	3.57	1.15	392	16.5	10	2.94	22	122	100	1500
5.0	3.6	2.5	2.0	500	3.3	4 x 22	3.57	1.69	392	23.2	10	2.94	6.8	122	100	1500
5.0	3.3	1.8	3.0	500	3.3	4 x 22	3.57	2.87	392	27.4	10	3.32	3.3	122	100	220
5.0	1.8	1.0	2.0	500	3.3	4 x 22	1.13	4.52	392	16.5	10	8.45	4.7	122	100	680
5.0	2.2	1.8	3.0	500	3.3	4 x 22	3.57	2.87	392	22.1	10	5.90	3.3	122	100	330
5.0	2.1	1.8	1.0	500	3.3	4 x 22	3.57	2.87	392	12.7	10	6.49	15	122	100	680
5.0	1.2	0.8	2.0	500	3.3	4 x 22	short	open	392	13.3	10	22.1	4.7	122	N/A	100
3.3	2.8	2.5	2.0	500	1.0	4 x 22	3.57	1.69	392	20.5	10	4.12	6.8	122	100	1000
3.3	2.2	1.8	3.0	500	2.0	4 x 22	3.57	2.87	392	22.1	10	5.90	3.3	122	100	470
3.3	2.1	1.8	1.0	1000	1.0	4 x 22	3.57	2.87	182	12.7	10	6.49	15	122	100	680
3.3	1.3	1.0	2.0	1000	1.0	4 x 22	1.13	4.52	182	14.0	10	17.4	4.7	122	100	220
3.3	1.1	0.8	2.0	1000	1.0	4 x 22	short	open	182	13.0	10	30.1	4.7	122	N/A	68

8.2 Typical Application

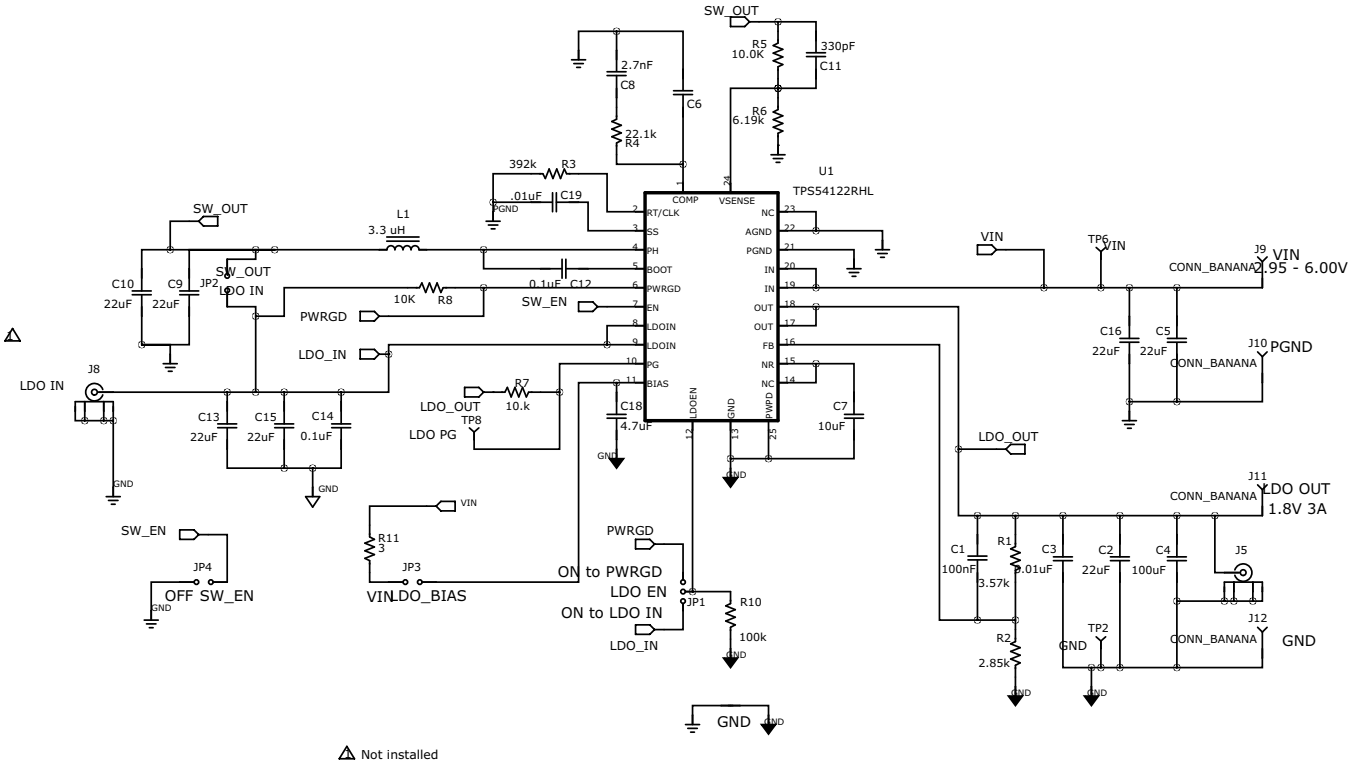


Figure 27. High-Frequency, 1.8-V Output, Low-Noise Power-Supply Design with Adjusted UVLO

Typical Application (continued)

8.2.1 Design Requirements

The application schematic illustrated in Figure 27 meets the parameters of Table 2. This circuit is available as the TPS54122EVM-201 evaluation module. The design procedure is given in this section. For more information about type-II and type-III frequency compensation circuits, see application report *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352).

Table 2. Design Parameters

PARAMETER	VALUE
SW output voltage (V_{OUT})	2.16 V
LDO output voltage (LDO_{Vout})	1.8 V
Transient response at V_{OUT}	ΔV_{OUT} = 5%
Input voltage VIN	5 V nominal, 3 V to 5.5 V
Output voltage ripple at V_{OUT} ($V_{O(ripple)}$)	< 30 mV_{PP}
Switching frequency (f_{SW})	500 kHz
Output current (I_O)	3 A

8.2.2 Detailed Design Procedure

8.2.2.1 Operating Frequency

The first step is to select a switching frequency for the regulator. This step involves a trade-off between higher and lower switching frequencies. Higher switching frequencies can produce a smaller solution size using lower-valued inductors and smaller-output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes additional switching losses that can negatively impact converter efficiency and thermal performance. In this design, the selection of a moderate switching frequency of 500 kHz achieves both a small solution size and high-efficiency operation. Using the resistor at the RT/CLK pin (R_3) sets this frequency.

Using Equation 9, the required resistance for a switching frequency of 500 kHz is 381 kΩ. This design uses a standard 1%, 392-kΩ resistor.

$$R_3\ (k\Omega) = 311890 \times f_{SW}\ (kHz)^{(-1.0793)} \tag{9}$$

8.2.2.2 Inductor Selection

Equation 10 is a calculation of the value of the output inductor, where V_{OUT} is the output voltage of the switcher. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high-inductor-ripple current affects the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Typically, the designer selects the inductor ripple value; however, K_{IND} is typically in the range of 0.1 to 0.3 for most applications.

$$L1 = \frac{V_{IN(max)} - V_{OUT}}{I_O \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{10}$$

For this design example, by using K_{IND} = 0.3, the calculated inductor value is 2.9 µH. The chosen standard value is 3.3 µH for this design. For the output filter inductor, do not exceed the root mean squared (RMS) current and saturation current ratings. Use Equation 11, Equation 12, and Equation 13 to find the inductor ripple current, RMS current, and peak inductor current, respectively.

$$I_{RIPPLE} = \frac{V_{IN(max)} - V_{OUT}}{L1} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \quad (11)$$

$$I_{L(rms)} = \sqrt{I_o^2 + \frac{1}{12} \times \left[\frac{V_O \times (V_{IN(max)} - V_O)}{V_{IN(max)} \times L1 \times f_{SW}} \right]^2} \quad (12)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (13)$$

For this design, the inductor ripple current is 795 mA, the RMS inductor current is 3 A, and the peak inductor current is 3.4 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switching current limit, rather than the peak inductor current.

8.2.2.3 Output Capacitor Selection of the Switcher

Consider the three following primary requirements for selecting the value of the output capacitor of the switcher:

- Minimum capacitance to meet the load transient
- Minimum capacitance to meet the output voltage ripple
- Maximum equivalent series resistance (ESR) to meet the output voltage ripple

Select the output capacitor based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This condition arises if desired hold-up times occur for the regulator, where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs in the load current, such as when transitioning from no load to a full load. The regulator typically requires two or more clock cycles for the change in load current and output voltage to affect the control loop and adjust the duty cycle to react to the change. Choose the output capacitor size to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles, while allowing only a tolerable amount of droop in the output voltage. The minimum output capacitance required is determined by Equation 14.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (14)$$

where:

- ΔI_{OUT} is the change in output current,
- f_{SW} is the regulator switching frequency, and
- ΔV_{OUT} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 1 A. Using these numbers (ΔI_{OUT} = 1 A and ΔV_{OUT} = 0.05 × 2.16 = 108 mV) gives a minimum capacitance of 37 µF. This value does not take into account the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 15 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{O(ripple)}}{I_{RIPPLE}}}$$

where:

- f_{SW} is the switching frequency,
- $V_{O(ripple)}$ is the maximum allowable output voltage ripple of the switcher output, and
- I_{RIPPLE} is the inductor ripple current calculated to be 795 mA. (15)

In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 15 yields 6.6 µF.

Equation 16 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 16 indicates the ESR must be less than 38 mΩ.

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{RIPPLE}} \quad (16)$$

The capacitance of a ceramic capacitor depends on the dc output voltage. Refer to the capacitor data sheet to select output capacitors based on the respective voltage rating. For the minimum capacitance that meets the load step specification of 37 µF, this example uses two effective 22-µF, 6.3-V, X5R ceramic capacitors with 4 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current that can be tolerated without failing or producing excess heat. Use an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the RMS value of the maximum ripple current. Equation 17 can calculate the RMS ripple current the output capacitor must support. For this application, Equation 17 yields 230 mA.

$$I_{Co(rms)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\sqrt{12} \times V_{IN(max)} \times L1 \times f_{SW}} \quad (17)$$

8.2.2.4 Input Capacitor

The TPS54122-Q1 requires a high-quality, ceramic, X5R- or X7R-type, 4.7-µF, input decoupling capacitor on the input voltage rail. In some applications, additional bulk capacitance may also be required for the LDO BIAS input. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54122-Q1. The input ripple current for this design, using Equation 18, is 1.35 A.

$$I_{Ci(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (18)$$

The capacitance of a ceramic capacitor varies significantly over both temperature and the amount of dc bias applied to the capacitor. The capacitance variations resulting from temperature can be minimized by selecting a dielectric material that is stable over temperature. The high capacitance-to-volume ratio and stability over temperature make the X5R and X7R ceramic dielectrics good selections for power-regulator capacitors. The capacitance value of a capacitor decreases as the dc bias across the capacitor increases. For this example design, a ceramic capacitor with at least a 10-V voltage rating is necessary to support the maximum input voltage. Two 22-µF, 10-V capacitors are connected to VIN and a 4.7-µF, 10-V capacitor is connected at BIAS for this example. The input capacitance value determines the input ripple voltage of the regulator. Use Equation 19 to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}} \tag{19}$$

Using the design example values where $I_{OUT(max)}$ = 3 A, C_{IN} = 50 µF, and f_{SW} = 500 kHz, Equation 19 yields an input voltage ripple of 30 mV.

8.2.2.5 Input Capacitor of the LDO

Although an input capacitor is unnecessary for stability, connecting a 0.1-µF to 1-µF low ESR capacitor across the input supply near the LDO input pin is good analog design practice. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device location is several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability. This design example uses two 22-µF input capacitors.

8.2.2.6 Output Capacitor of the LDO

The internal LDO of the TPS54122-Q1 is stable with standard ceramic capacitors with capacitance values 4.7 µF or larger. Higher values are recommended for better noise performance. For best noise performance, the evaluated design uses 100-µF, 22-µF, and 0.1-µF ceramic capacitors with a 6.3-V rating. X5R- and X7R-type capacitors are excellent choices because they have minimal variation in value and ESR over temperature.

8.2.2.7 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach its nominal programmed value during power-up. This feature is useful if a load requires a controlled voltage slew rate. This feature is also useful if the output capacitance is large and requires a large amount of current to charge the capacitor to the output voltage level. The large currents required to charge the capacitor can make the TPS54122-Q1 reach current limit, or the excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use Equation 20 to calculate the soft-start capacitor value.

$$C_{SS} = \frac{T_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)} \tag{20}$$

The example circuit has the soft-start time set to an arbitrary value of 3.5 ms, which requires a 10-nF capacitor. In the TPS54122-Q1, I_{SS} is 2.2 µA and V_{REF} is 0.827 V.

8.2.2.8 Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper device operation. Use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

8.2.2.9 Output Voltage Feedback Resistor Selection

Choose resistors R_5 and R_6 to set the output voltage of the switcher, and choose R_1 and R_2 to set the output voltage of the LDO. This example design uses 6.19 kΩ for R_6 and 2.85 kΩ for R_2. Use Equation 21 and Equation 22 to calculate R_5 and R_1, respectively.

$$R_5 = \frac{V_{OUT} - V_{REF}}{V_{REF}} R_6 \tag{21}$$

$$R_1 = \frac{LDO_{V(out)} - LDO_{V(ref)}}{LDO_{V(ref)}} R_2 \tag{22}$$

where:

- V_{OUT} is the output of the switcher,
- $LDO_{V(out)}$ is for the LDO,
- V_{REF} is 0.827 V, and
- $LDO_{V(ref)}$ is 0.8 V.

The closest 1% resistors from the calculated results of Equation 21 and Equation 22 for R_5 and R_1 are 10 kΩ and 3.57 kΩ, respectively.

8.2.2.10 Switcher Minimum and Maximum Output Voltage

The internal design of the TPS54122-Q1 sets a minimum switcher output voltage limit for any given input voltage. The output voltage can never be less than the internal voltage reference; the minimum controllable on-time can limit output voltage. In this case, Equation 23 gives the minimum output voltage:

$$V_{O(min)} = \text{On-Time(min)} \times f_{S(max)} \times [V_{IN(max)} - I_{O(min)} \times 2 \times RDS] - I_{O(min)} \times (R_L + RDS) \tag{23}$$

where:

- $V_{O(min)}$ = minimum achievable output voltage,
- On-Time(min) = minimum controllable on-time (65 ns typical, 120 ns, no load),
- $f_{S(max)}$ = maximum switching frequency, including tolerance,
- $V_{IN(max)}$ = maximum input voltage,
- $I_{O(min)}$ = minimum load current,
- RDS = minimum high-side MOSFET on-resistance (45 mΩ to 64 mΩ), and
- R_L = series resistance of the output inductor.

There is also a maximum achievable output voltage that is limited by the minimum off-time. The maximum output voltage is given by Equation 24.

$$V_{O(max)} = [1 - \text{Off-Time(max)} \times f_{S(max)}] \times [V_{IN(min)} - I_{O(max)} \times 2 \times RDS] - I_{O(max)} \times (R_L + RDS) \tag{24}$$

where:

- $V_{O(max)}$ = maximum achievable output voltage,
- Off-Time(max) = maximum controllable off-time (60 ns typical),
- $f_{S(max)}$ = maximum switching frequency, including tolerance,
- $V_{IN(min)}$ = minimum input voltage,
- $I_{O(max)}$ = maximum load current,
- RDS = maximum high-side MOSFET on-resistance (81 mΩ to 110 mΩ), and
- R_L = series resistance of the output inductor.

8.2.2.11 Compensation Component Selection

Several industry techniques can compensate dc-dc regulators. The method used here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. This method ignores the effects of the slope compensation that is internal to the TPS54122-Q1. This method ignores the slope compensation; therefore, the actual crossover frequency is usually lower than the crossover frequency in the following calculations.

Type-III compensation is used to achieve a high-bandwidth, high-phase-margin design. This design targets a crossover frequency (bandwidth) of 67 kHz. Equation 25 and Equation 26 calculate the power-stage pole and zero at 2.5 kHz and 1809 kHz, respectively. For the output capacitance of the switcher (C_{OUT}), include the two input capacitors on the LDO; therefore, the total capacitance is 4 × 22 µF = 88 µF, and R_{ESR} = 4 mΩ / 4 = 1 mΩ.

$$f\,p_{MOD} = \frac{I_{OUT(max)}}{2\pi \times V_{OUT} \times C_{OUT}} \tag{25}$$

$$f\,z_{MOD} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{26}$$

The compensation components calculations are now possible. First, calculate the value for R_4 that sets the gain of the compensated network at the crossover frequency. Use Equation 27 to determine the value of R_4.

$$R_4 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{g_{m(ea)} \times V_{REF} \times g_{m(ps)}} \tag{27}$$

By using Equation 27, R_4 = 22.1 kΩ.

Next, calculate the value of C_8. Together with R_4, C_8 places a compensation zero at the dominant power-stage pole frequency f_p. Use Equation 28 to determine the value of C_8:

$$C_8 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_4} \tag{28}$$

Using Equation 28, the standard value for C_8 is 2.7 nF.

In order to provide a zero around the crossover frequency to boost the phase at crossover, add a capacitor (C_{11}) parallel to R_5. Equation 29 gives the value for the C_{11} capacitor. A close standard value for C_{11} is 330 pF.

$$C_{11} = \frac{1}{2\pi \times R_5 \times f_C} \tag{29}$$

Using the feed-forward capacitor (C_{11}) creates a low, ac-impedance path from the output voltage to the VSENSE input of the integrated circuit that can couple noise at the switching frequency into the control loop. Do not use a feed-forward capacitor for high-output voltage ripple designs (greater than 15 mV peak-to-peak at the VSENSE input) operating at duty cycles of less than 30%. When using C_{11}, always limit the closed-loop bandwidth to no more than one-tenth of the switching frequency.

Use an additional high-frequency pole, if necessary, to cancel the zero from the output capacitor ESR by adding a capacitor in parallel with the series combination of R_4 and C_8. Equation 30 calculates the pole that cancels the zero from the output capacitor ESR. Capacitor C_6 is optional and is not used in this design.

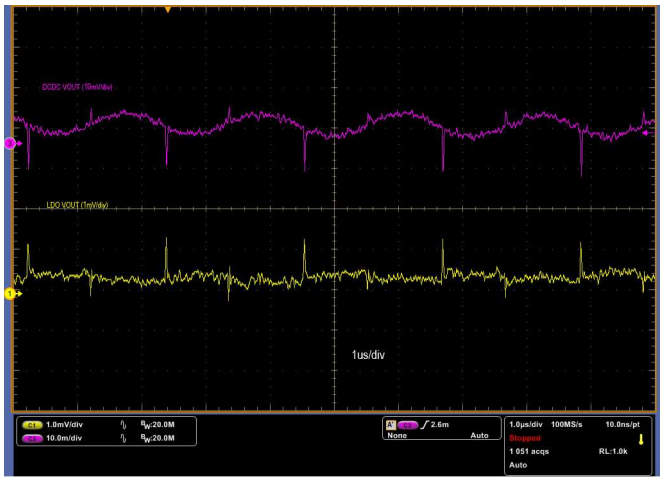
$$C_6 = \frac{R_{ESR} \times C_{OUT}}{R_4} \tag{30}$$

8.2.2.12 Noise-Reduction Capacitor

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS54122-Q1, the band gap does not contribute significantly to noise. Instead, the output resistor divider and the error amplifier input dominate the noise. To minimize the noise in this application, use a 1-µF noise-reduction capacitor.

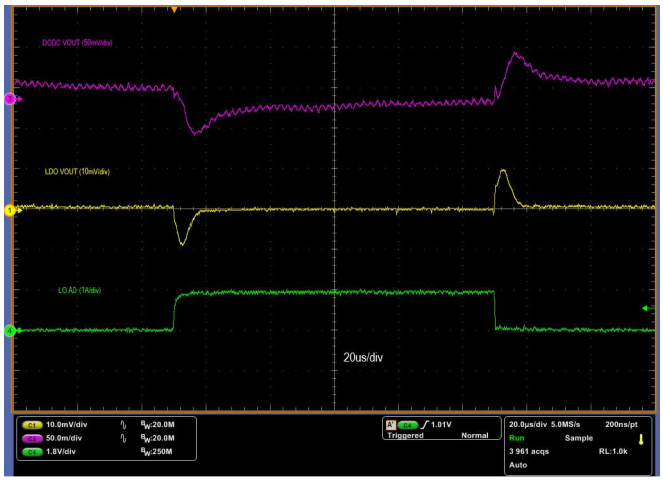
In addition to noise-reduction purposes, the capacitor on the NR pin slows start-up time. Changing the value of C_{NR} can adjust the start-up time of the LDO. In this design, the 1-µF noise-reduction capacitor sets the LDO start-up time to 1 s.

8.2.3 Application Curves



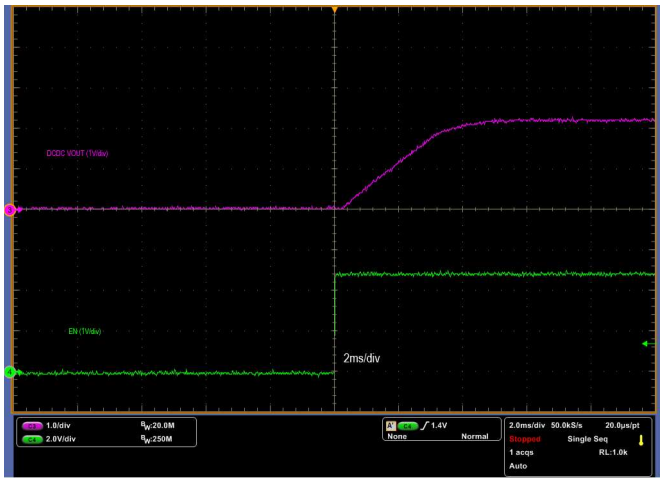
V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 28. DC-DC Output Voltage and LDO V_{OUT} ($LDO_{V(out)}$)



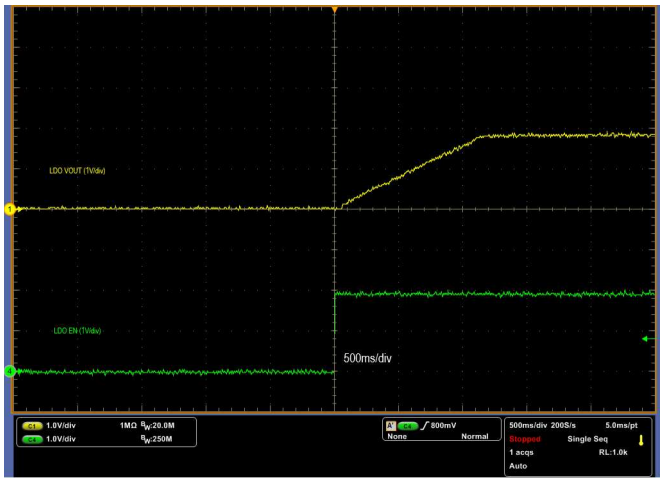
V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A to 2 A

Figure 29. Load Transient Response



V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 30. Start-Up Using DC-DC Enable (EN Pin)



V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 31. Start-Up Using LDO Enable (LDOEN Pin)

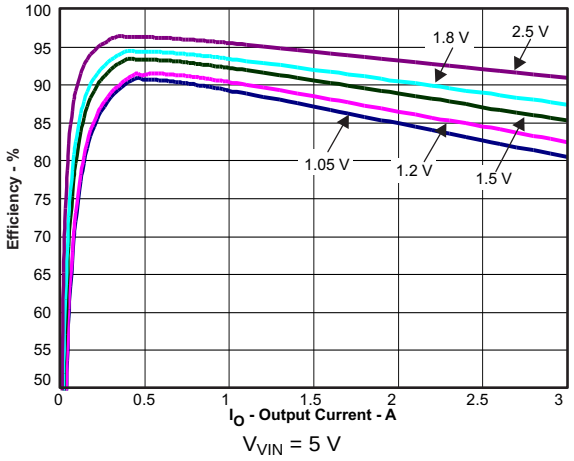


Figure 32. DC-DC Efficiency vs Output Current

9 Power Supply Recommendations

With BIAS connected to VIN, the device is designed to operate from an input voltage supply range of 2.95 V to 5.5 V. This input supply to the dc-dc converter or LDO regulator must be well-regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The added capacitance is not critical; a 47-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

Correct printed circuit board (PCB) layout is a critical portion of good power-supply design and is particularly important for the high PSR and low-noise performance of the TPS54122-Q1. The following general guidelines are provided; for a more detailed description, refer to the TPS54122-EVM-201 user guide, SLVU829.

- Place the inductor, boot capacitor, and output capacitor of the dc-dc converter on the layers of the board (such as the bottom layer) that help minimize the spread of switching noise into the LDO area on the board.
- Connect the boot capacitor and inductor L1 as close as possible to the PH pin to reduce parasitic inductance of long traces.
- To help shield the compensation components (the soft-start capacitors, the CLK/RT resistor, and the dc-dc feedback resistors) from noise, ground these components to a power ground that is shielded from the high-current ground plane. To achieve this shielding, use a separate trace to the PGND pin.
- The RT/CLK pin is sensitive to noise so place the RT resistor as close as possible to the device, routed with a short connection.
- Place the noise-reduction capacitor as close as possible to the device to avoid noise pickup into the LDO reference.
- Isolate the ground planes on the input and output from each other, connected through a separate trace route that parallels the power-loop routing from the dc-dc output to the LDO input.
- Terminate the low-noise analog ground of the LDO circuits (such as the voltage set point divider, the LDO input, and output capacitors) to ground using a wide ground trace separate from the power ground plane.
- Place the LDO input and output capacitors as close to the device as possible.
- Bypass the VIN pin to ground using a low-ESR ceramic capacitor with an X5R or X7R dielectric, placed as close as possible to the VIN and PGND pins.
- For operation at the full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipation.
- Minimize PCB conductor planes to prevent excessive capacitive coupling.

10.2 Layout Example

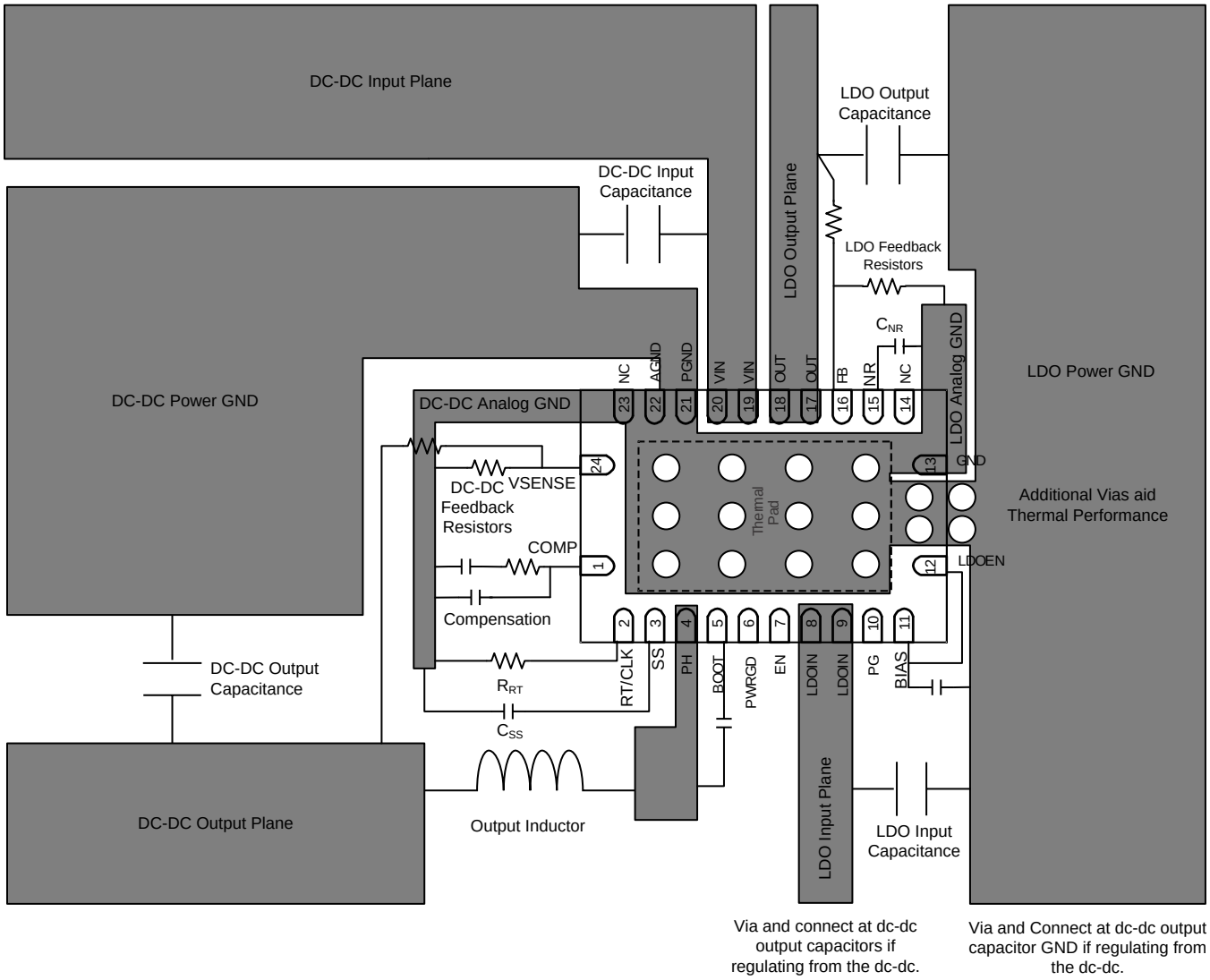


Figure 33. Example Layout

10.3 Thermal Information

The internal thermal protection circuitry of the device is designed to protect against overload conditions. However, this circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability. The TPS54122-Q1 has thermal protection for both the switcher and the LDO, which operate independently of each other.

10.3.1 Thermal Protection of the Switcher

The internal thermal-shutdown circuitry of the switcher forces the device to stop switching if the junction temperature exceeds 165°C (typically). After the device junction temperature drops below 150°C (typically), the dc-dc converter reinitiates the power-up sequence by discharging the SS pin to less than 40 mV.

10.3.2 Thermal Protection of the LDO

Thermal protection of the integrated LDO disables the LDO output of the TPS54122-Q1 when the junction temperature rises to 155°C (typically), allowing the device to cool. When the junction temperature cools to 140°C (typically), the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal-protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS54122-Q1. The TPS54122EVM-201 evaluation module (and related user guide) can be requested at the Texas Instruments web site through the evaluation module tool folder.

11.2 Documentation Support

11.2.1 Related Documentation

- TPS54122-EVM-201 User Guide, SLVU829
- *Design Procedures for the TPS54122*, SLVA602
- *Designing Type III Compensation for Current Mode Step-Down Converters*, SLVA352

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54122QRHLRQ1	ACTIVE	VQFN	RHL	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	54122Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS54122-Q1 :

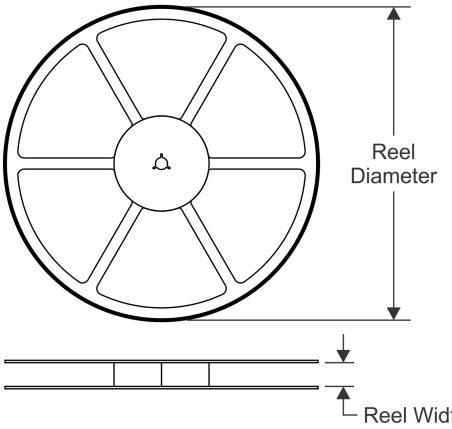
- Catalog: TPS54122

NOTE: Qualified Version Definitions:

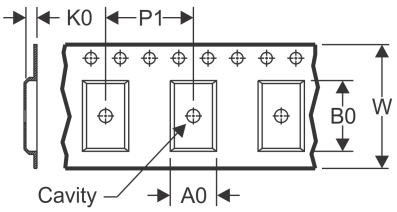
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

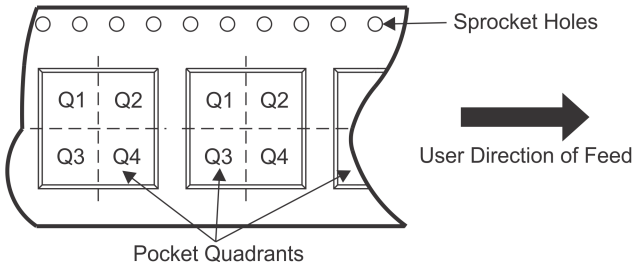


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

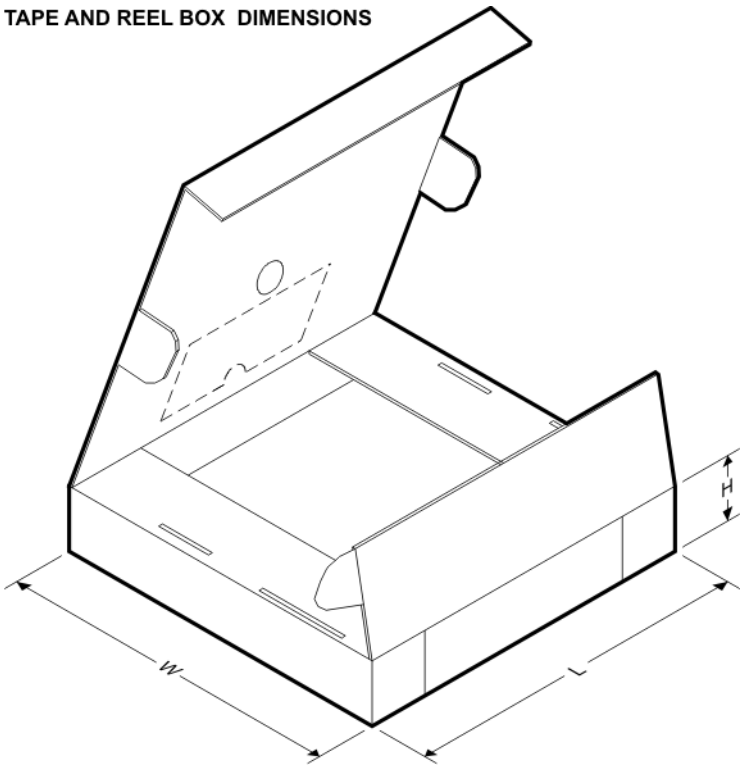
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54122QRHLRQ1	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

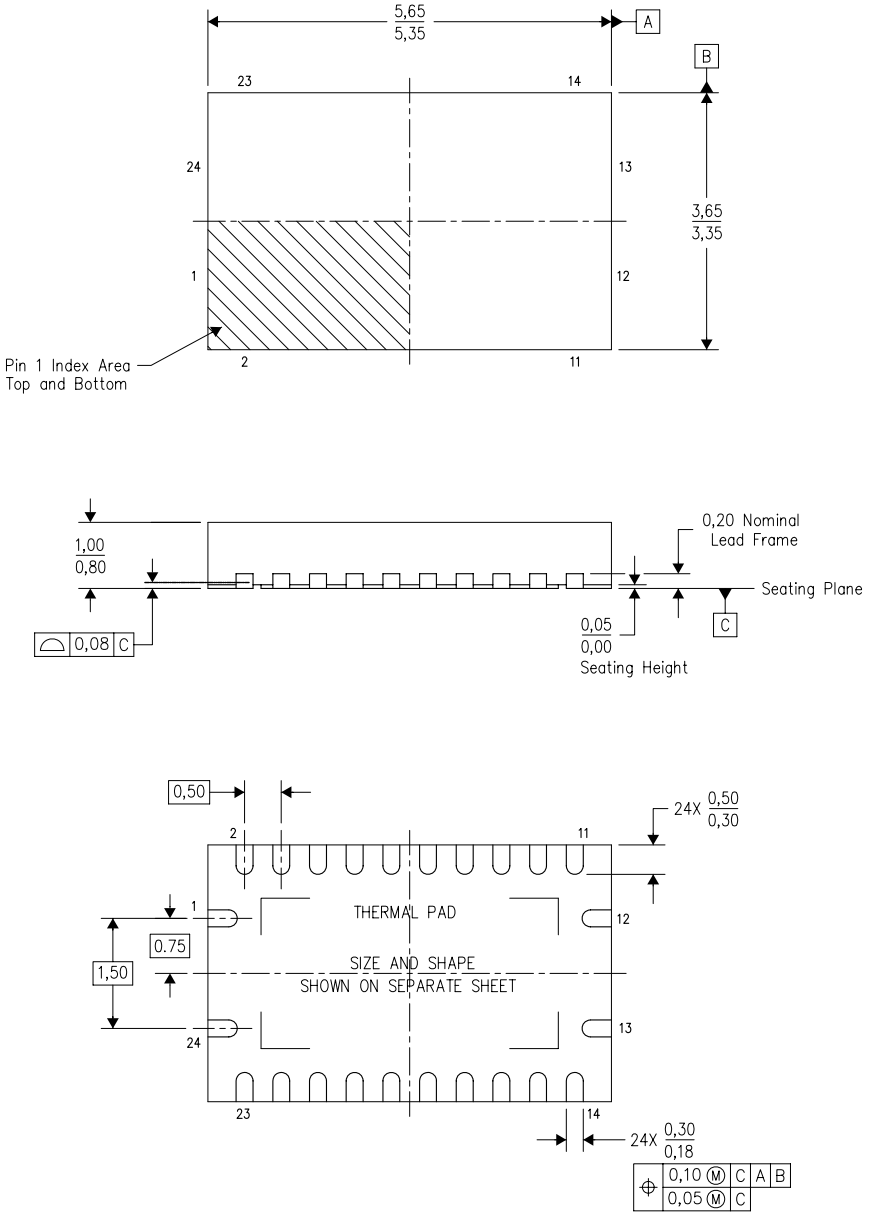
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54122QRHLRQ1	VQFN	RHL	24	3000	367.0	367.0	35.0

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4205346–4/J 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. JEDEC MO–241 package registration pending.

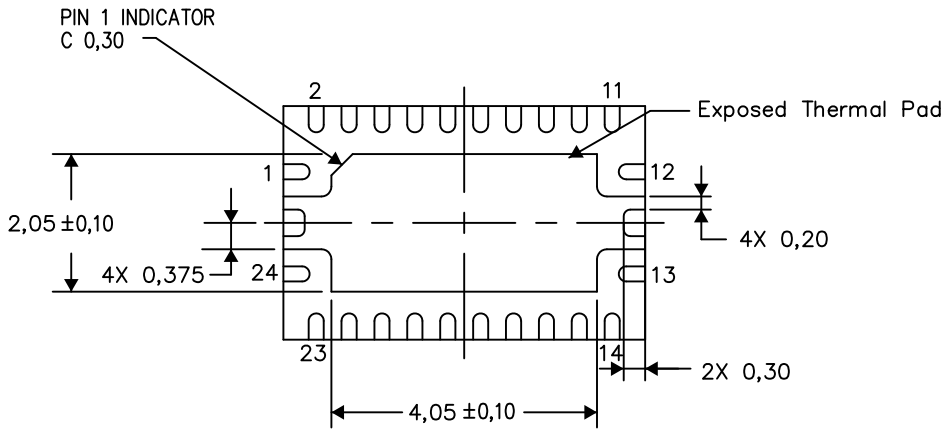
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



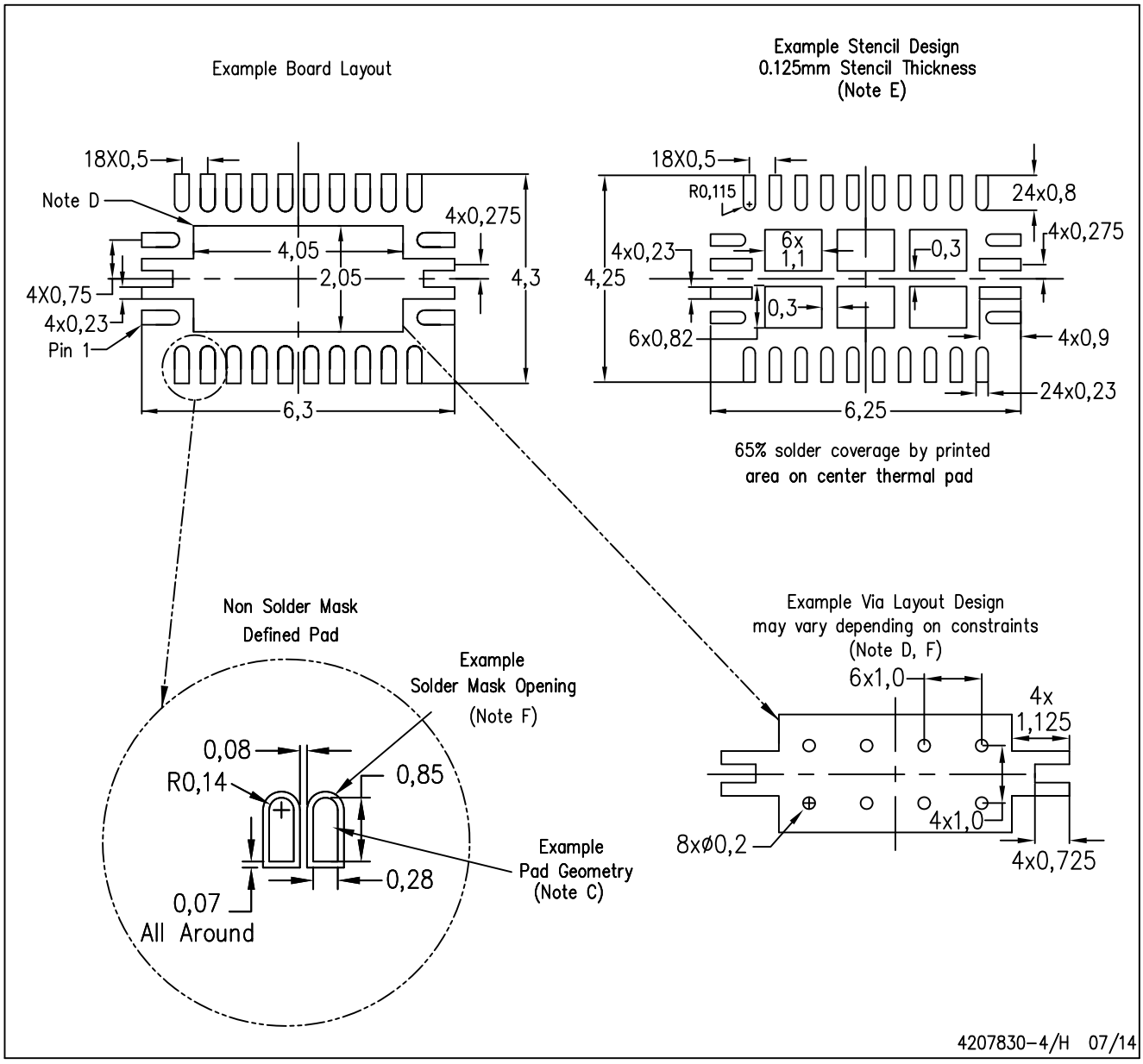
Bottom View

Exposed Thermal Pad Dimensions

4206363–4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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