TPS62745 Dual-cell Ultra Low I_Q Step Down Converter for Low Power Wireless Applications

1 Features

- Input Voltage Range V_{IN} from 3.3 V to 10 V
- Typical 400 nA Quiescent Current
- Up to 90% efficiency with load currents >15 µA
- Up to 300 mA Output Current
- RF Friendly DCS-Control™
- Low Output Ripple Voltage
- 16 Selectable Output Voltages from
  - 1.8 V to 3.3 V (TPS62745)
  - 1.3 V to 2.8 V (TPS627451)
- Integrated input voltage switch
- Integrated Discharge Function at VOUT
- Open Drain Power Good Output
- Operates with a Tiny 3.3 µH or 4.7 µH Inductor
- Small 3 mm x 2 mm WSON Package

2 Applications

- Bluetooth® Low Energy, RF4CE, Zigbee
- Industrial Metering
- Energy Harvesting

3 Description

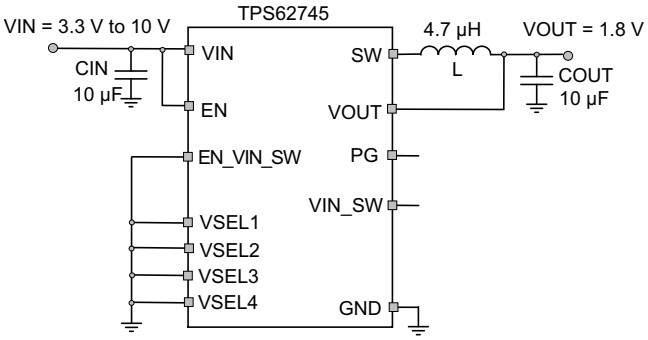
The TPS62745 is a high efficiency ultra low power synchronous step down converter optimized for low power wireless applications. It provides a regulated output voltage consuming only 400-nA quiescent current. The device operates from two rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-SO2, Li-MnO2 or four to six cell alkaline batteries. The input voltage range up to 10 V allows also operation from a USB port and thin-film solar modules. The output voltage is set with four VSEL pins between 1.8 V and 3.3 V for TPS62745 or 1.3 V and 2.8 V for TPS627451. TPS62745 features low output ripple voltage and low noise with a small output capacitor. An internal input voltage switch controlled by pin EN_VIN_SW connects the supply voltage to pin VIN_SW. The switch is intended to be used for an external voltage divider, scaling down the input voltage for an external ADC. The switch is automatically opened when the supply voltage is below the undervoltage lockout threshold. The TPS62745 is available in a small 12 pin 3 mm × 2 mm WSON package.

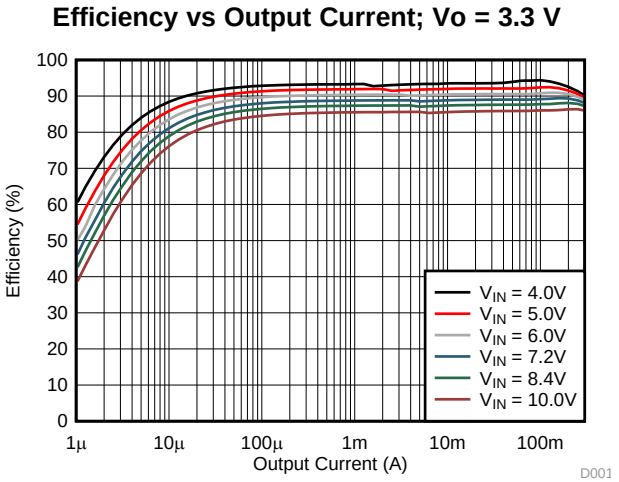
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62745	WSON	3 mm x 2 mm
TPS627451		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Schematic





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Changes from Original (May 2015) to Revision A **Page**

- Changed status to Production Data ... 1

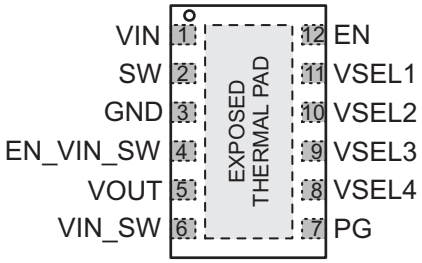
5 Device Comparison Table[(1)]

Device Number	Output voltage range	marking
TPS62745	1.8 V to 3.3 V in 100-mV steps	PD5I
TPS627451	1.3 V to 2.8 V in 100-mV steps	PD6I

(1) For all available packages, see the orderable addendum at the end of the datasheet.

6 Pin Configuration and Functions

DSS Package
12-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	PWR	V_{IN} power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 4.7 µF from this pin to GND is required.
SW	2	OUT	This is the switch pin which is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	3	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
EN_VIN_SW	4	IN	This pin connects / disconnects the internal switch from VIN to pin VIN_SW. With EN_VIN_SW = Low, the switch is open. With EN_VIN_SW = High, the switch is closed connecting VIN with VIN_SW. If not used, the pin should be tied to GND.
VOUT	5	IN	Feedback pin for the internal feedback divider network and regulation loop. Connect this pin directly to the output capacitor with a short trace.
VIN_SW	6	OUT	This is the output of a switch connecting VIN with VIN_SW when EN_VIN_SW = High. If not used, leave this pin open.
PG	7	OUT	This is an open drain power good output.
VSEL4	8	IN	Output voltage selection pins. See Table 1 and Table 2 for V_{OUT} selection. These pins must be terminated.
VSEL3	9	IN	
VSEL2	10	IN	
VSEL1	11	IN	
EN	12	IN	High level enables the devices, low level turns the device into shutdown mode. This pin must be terminated.
EXPOSED THERMAL PAD		NC	Not electrically connected to the IC. Connect this pad to GND and use it as a central GND plane.

Table 1. Output Voltage Setting for TPS62745

Device	VOUT / V	VSEL4	VSEL 3	VSEL 2	VSEL 1
TPS62745	1.8	0	0	0	0
	1.9	0	0	0	1
	2.0	0	0	1	0
	2.1	0	0	1	1
	2.2	0	1	0	0
	2.3	0	1	0	1
	2.4	0	1	1	0
	2.5	0	1	1	1
	2.6	1	0	0	0
	2.7	1	0	0	1
	2.8	1	0	1	0
	2.9	1	0	1	1
	3.0	1	1	0	0
	3.1	1	1	0	1
	3.2	1	1	1	0
	3.3	1	1	1	1

Table 2. Output Voltage Setting for TPS627451

Device	VOUT / V	VSEL4	VSEL 3	VSEL 2	VSEL 1
TPS627451	1.3	0	0	0	0
	1.4	0	0	0	1
	1.5	0	0	1	0
	1.6	0	0	1	1
	1.7	0	1	0	0
	1.8	0	1	0	1
	1.9	0	1	1	0
	2.0	0	1	1	1
	2.1	1	0	0	0
	2.2	1	0	0	1
	2.3	1	0	1	0
	2.4	1	0	1	1
	2.5	1	1	0	0
	2.6	1	1	0	1
	2.7	1	1	1	0
	2.8	1	1	1	1

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

	PIN	MIN	MAX	UNIT
Voltage	VIN	–0.3	12	V
	SW, VIN_SW(2)	–0.3	V_{IN} +0.3	V
	EN	–0.3	V_{IN} +0.3	V
	EN_VIN_SW, VSEL1-4	–0.3	6	V
	PG	–0.3	6	V
	VOUT	–0.3	3.6	V
Power Good Sink Current	PG		10	mA
V_{IN} Switch Output Current	VIN_SW		10	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The DC voltage on the SW pin must not exceed 3.6 V

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage V_{IN}		3.3		10	V
Output current I_{OUT}	V_{OUT} + 0.7 V ≤ V_{IN} ≤ 10 V			300	mA
Effective inductance		2.8	4.7	6.2	µH
Capacitance connected to VIN pin		3	10		µF
Total effective capacitance connected to VOUT pin (1)		5	10	22	µF
Operating junction temperature range, T_J		–40		125	°C
Operating ambient temperature range, T_A		–40		85	°C

(1) Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the smallest capacitor required with the DC bias effect for this type of capacitor in mind. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

7.4 Thermal Information

THERMAL METRIC[1]		TPS62745 DSS 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 6 V, T_J = –40°C to 125°C typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range	V_{OUT} + 0.7 V ≤ V_{IN} ≤ 10 V ; min 3.3 V, whichever value is higher	3.3		10	V
I_Q	Operating quiescent current	EN = V_{IN}, device not switching; I_{OUT} = 0 µA; V_{OUT} = 2 V; T_J = –40°C to 85°C		400	1960	nA
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN}; T_J = -40°C to 85°C		130	1200	nA
		EN = GND, shutdown current into V_{IN}; T_J = 60°C			830	
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}; T_J = –40°C to 85°C		3.1	3.3	V
V_{TH_UVLO-}		Falling V_{IN}; T_J = –40°C to 85°C		2.9	3.1	
INPUTS (EN, EN_VIN_SW, VSEL1-4)						
$V_{IH\ TH}$	High level input voltage	V_{TH_UVLO-} ≤ V_{IN} ≤ 10 V	1.2			V
$V_{IL\ TH}$	Low level input voltage	V_{TH_UVLO-} ≤ V_{IN} ≤ 10 V			0.35	V
I_{IN}	Input bias current; except EN pin	T_J = 25°C			10	nA
		T_J = 60°C			20	
		T_J = –40°C to 85°C			50	
I_{IN}	Input bias current for EN pin	T_J = 25°C			20	nA
		T_J = 60°C			40	
		T_J = –40°C to 85°C			100	
POWER SWITCHES						
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 4 V, I = 140 mA		0.6	0.98	Ω
	Low side MOSFET on-resistance			0.5	0.85	
I_{LIMF}	High side MOSFET DC switch current limit	3.6 V ≤ V_{IN} ≤ 10 V; device not in soft start	480	600	720	mA
	Low side MOSFET DC switch current limit			600		

Electrical Characteristics (continued)

V_{IN} = 6 V, T_J = –40°C to 125°C typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE SWITCH (VOUT)							
R_{DSCH_VOUT}	MOSFET on-resistance	EN = GND, I_{OUT} = –10 mA into VOUT pin			25	60	Ω
I_{IN_VOUT}	Bias current into VOUT pin (1)	EN = V_{IN}, V_{OUT} = 2 V	T_J = 25°C		40	100	nA
			T_J = –40°C to 85°C			500	
INPUT VOLTAGE SWITCH (VIN_SW)							
$R_{DS(ON)}$	MOSFET on-resistance	EN_VIN_SW = High, I_{VIN_SW} = 1 mA			85	160	Ω
$I_{VIN\_SW\_LKG}$	VIN-switch leakage current	EN_VIN_SW = GND; leakage from VIN to VIN_SW when pulled to GND; T_J = –40°C to 85°C		-20		20	nA
I_{VIN_SW}	VIN-switch current					5	mA
POWER GOOD OUTPUT (PG)							
V_{TH_PG+}	Power good threshold voltage	Rising output voltage on VOUT pin		95	97.5		%
V_{TH_HYS}	Power good threshold hysteresis	Falling output voltage on VOUT pin			3		
V_{OL}	Low level output threshold	3.3 V ≤ V_{IN} ≤ 10 V, EN = GND, current into PG pin I_{PG} = 4 mA				0.3	V
V_{OH}	High level output threshold	3.3 V ≤ V_{IN} ≤ 10 V, EN = high, current into PG pin I_{PG} = 0 mA				6	V
I_{IN_PG}	Bias current into power good pin	PG pin is high impedance, VOUT = 2 V, EN = V_{IN}, I_{OUT} = 0 mA; T_J = –40°C to 85°C				20	nA
OUTPUT							
$I_{LIM\_softstart}$	Switch current limit during soft start	Current limit is reduced during soft start, T_J = –40°C to 85°C		40	110	180	mA
V_{VOUT}	Output voltage range	For TPS627450; output voltages are selected with pins VSEL1 - 4		1.8		3.3	V
		For TPS627451; output voltages are selected with pins VSEL1 - 4		1.3		2.8	
	Output voltage accuracy	PFM mode, I_{OUT} = 0 mA, V_{OUT} + 0.6 V ≤ V_{IN} ≤ 10 V; min 3.3 V, whichever value is higher; T_J = –40°C to 85°C		-2.5	0	2.5	%
		PWM Mode, V_{OUT} + 0.7 V ≤ V_{IN} ≤ 10 V; min 3.3 V, whichever value is higher; T_J = –40°C to 85°C		–2	0	2	
	DC output voltage load regulation	V_{OUT} = 2.0 V; I_{OUT} = 2 mA to 80 mA (PFM mode)			0.005		%/mA
	DC output voltage load regulation	V_{OUT} = 2.0 V; I_{OUT} = 150 mA to 300 mA (PWM mode)			0.001		%/mA
	DC output voltage line regulation	V_{OUT} = 2.0 V, I_{OUT} = 300 mA, 4 V ≤ V_{IN} ≤ 10 V			0.015		%/V

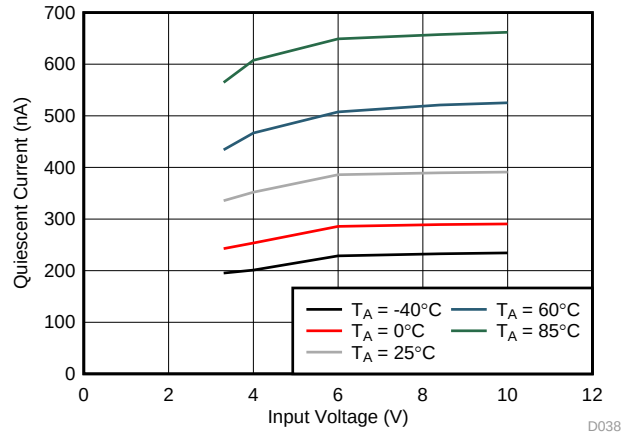
(1) A 50-MΩ (typical) internal resistor divider is internally connected to the VOUT pin

7.6 Timing Characteristics

V_{IN} = 6 V, T_J = –40°C to 125°C typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
t_{delay}	UVLO delay time	response time of UVLO circuit		200		µs
INPUT VOLTAGE SWITCH (VIN_SW)						
t_{VIN_SW}	VIN-switch turn-on settling time	Time from EN_VIN_SW = High until $R_{DS(ON)}$ is within specification		100		µs
POWER GOOD OUTPUT (PG)						
t_{delay}	PGOOD delay time	Response time of PGOOD circuit; falling edge		200		µs
OUTPUT						
t_{ONmin}	Minimum ON time	V_{IN} = 6 V, V_{OUT} = 2.0 V, I_{OUT} = 0 mA		256		ns
t_{OFFmin}	Minimum OFF time	V_{IN} = 3.3 V		50		ns
t_{Start}	Regulator start up time	V_{IN} = 6 V, from transition EN = Low to High until device starts switching, T_J = -40°C to 85°C		15	50	ms
$t_{Softstart}$	Softstart time with reduced switch current limit	3.3 V ≤ V_{IN} ≤ 10 V, EN = V_{IN}		700		µs

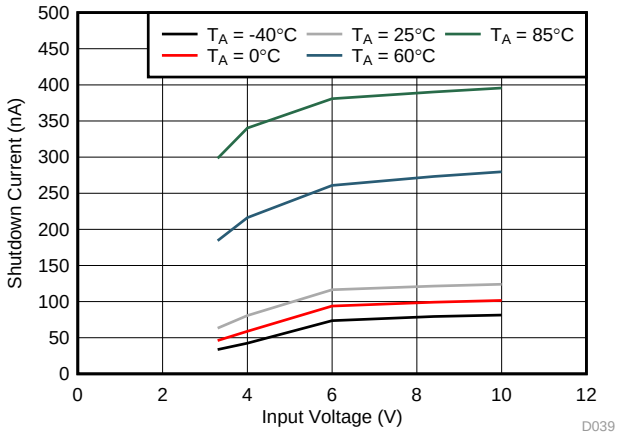
7.7 Typical Characteristics



EN = VIN, VOUT = 1.8 V, EN_VIN_SW = GND

Device Not Switching

Figure 1. Quiescent Current



EN = GND, EN_VIN_SW = GND

Figure 2. Shutdown Current

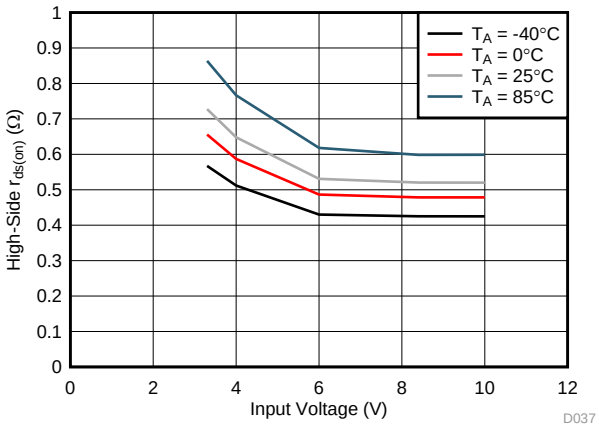


Figure 3. $R_{DS(ON)}$ High-Side MOSFET

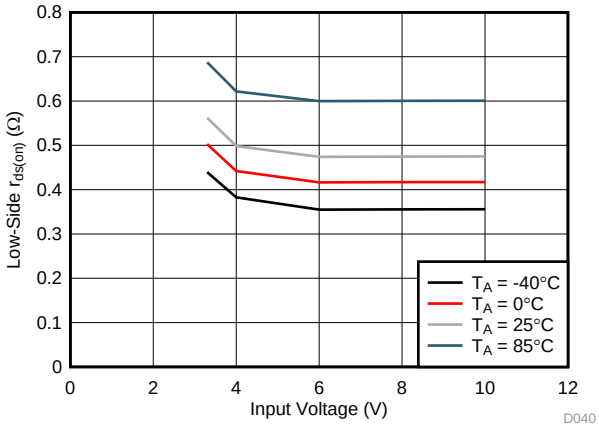


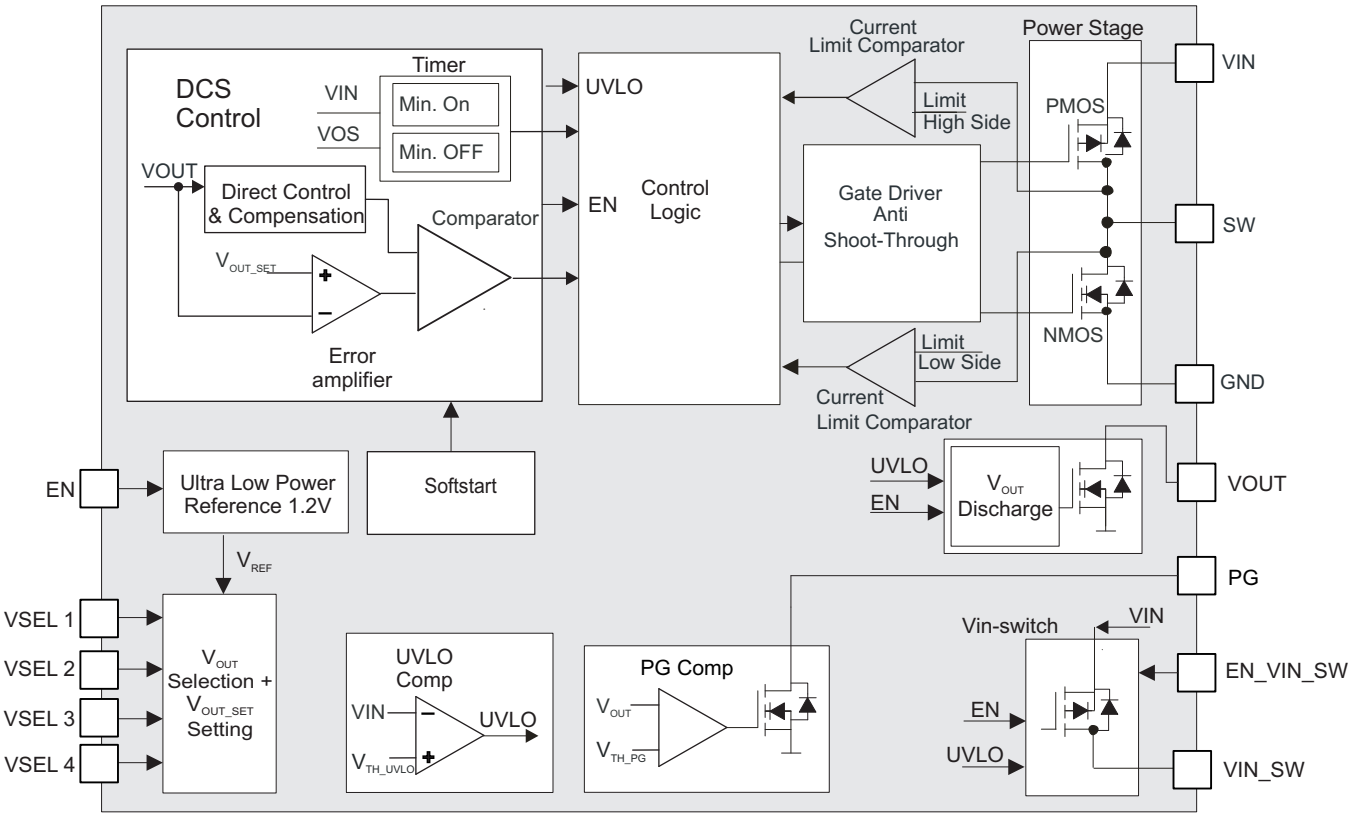
Figure 4. $R_{DS(ON)}$ Low-Side MOSFET

8 Detailed Description

8.1 Overview

The TPS62745 is the first dual-cell, ultra low power step down converter combining TI's DCS-Control™ topology and ultra low quiescent current consumption (400 nA typical) while maintaining a regulated output voltage. The device extends high efficiency operation to output currents down to a few micro amperes.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS - Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between pulse frequency modulation (PFM) and pulse width modulation (PWM) mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOUT pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The DCS-Control™ topology supports PWM mode for medium and high load conditions and a power save mode at light loads. During PWM mode, it operates in continuous conduction. The switching frequency is up to 2.5 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters power save mode to maintain high efficiency down to very light loads. In power save mode the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage. The TPS62745 offers both excellent DC voltage and superior load transient regulation, combined with very low

Feature Description (continued)

output voltage ripple, minimizing interference with RF circuits. At high load currents the converter operates in quasi fixed frequency PWM mode operation and at light loads in PFM mode to maintain highest efficiency over the full load current range. In PFM mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a quiescent current of typically 400-nA. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

8.3.2 Enable / Shutdown

The DC/DC converter is activated when EN pin is set to High. For proper operation, the pin must be terminated and must not be left floating. With EN pin set to Low, the device enters shutdown mode with typical 130 nA current consumption.

8.3.3 Power Good Output (PG)

The power good comparator features an open drain output. The PG comparator is active with EN pin set to high and V_{IN} above the threshold V_{TH_UVLO+}. It is driven to high impedance once V_{OUT} trips the threshold V_{TH_PG+} for rising V_{OUT}. The output is pulled to low level once V_{OUT} falls below the threshold V_{TH_PG-} . The output is as well pulled to low level in case the input voltage V_{IN} falls below the undervoltage lockout threshold V_{TH_UVLO-} or the device is disabled with EN = Low. With EN = High, the output is driven to high impedance state, once the load current falls below ~1 mA. In this case the PG comparator is turned off to achieve lowest quiescent current. PG will be triggered when a output voltage change is ongoing due to a change in VSEL pin levels if the new target is high enough to trigger the PG threshold.

8.3.4 Output Voltage Selection (VSEL1 - 4)

The TPS62745 does not require an external resistor divider network to program the output voltage. The device integrates a high impedance (typical 50 MΩ) feedback resistor divider network which is programmed by the pins VSEL1-4. TPS62745 supports an output voltage range of 1.8 V to 3.3 V in 100-mV steps while the TPS627451 supports an output voltage range of 1.3 V to 2.8 V. The output voltage can be changed during operation and supports simple dynamic output voltage scaling; see the *Application and Implementation* section for further details. The output voltage is programmed according to Table 1 for TPS62745 and Table 2 for TPS627451.

8.3.5 Input Voltage Switch

There is an internal switch that connects the input voltage applied at pin VIN to the VIN_SW output. The switch can be used to connect an external voltage divider for an ADC monitoring to the input voltage. An enable pin EN_VIN_SW turns the switch on and off, making sure there is no current through that external voltage divider when not needed. A logic high level on EN_VIN_SW turns the switch on once the input voltage is above the undervoltage lockout threshold and the device is enabled. The switch can be used for other purposes as long as the current rating of 5 mA and its turn-on resistance is observed. An external voltage divider should be in a range of 10 kΩ to 100 kΩ. Larger values than 100 kΩ can be used as long as the input resistance and capacitance of the external circuit (e.g. ADC input) is observed.

8.4 Device Functional Modes

8.4.1 Soft Start

When the device is enabled, the internal reference is powered up and after the startup delay time $t_{Startup\_delay}$ has expired, the device enters soft start, starts switching and ramps up the output voltage. During soft start the device operates with a reduced current limit, $I_{LIM\_softstart}$, of typical 1/5 of the nominal current limit. This reduced current limit is active during the soft start time $t_{Softstart}$. The current limit is increased to its nominal value, I_{LIMF}, once the soft start time has expired or the power good comparator detects that the output voltage reached its target value.

8.5 VOUT Discharge

The VOUT pin has a discharge circuit to connect the rail to GND, once it is disabled. This feature prevents residual charge voltages on the output capacitor, which may impact proper power up of the systems connected to the converter. With the EN pin pulled to low, the discharge circuit at the VOUT pin becomes active. The discharge circuit on VOUT is also associated with the UVLO comparator. The discharge circuit becomes active once the UVLO comparator triggers and the input voltage V_{IN} has dropped below the UVLO comparator threshold V_{TH_UVLO-} (typical 2.9 V).

8.6 Internal Current Limit

The TPS62745 integrates a current limit on the high side, as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

9 Application and Implementation

9.1 Application Information

The TPS62745 devices are a step down converter family featuring typical 400-nA quiescent current and operating with a tiny 4.7-µH inductor and a 10-µF output capacitor. These DCS-Control™ based devices extend the light load efficiency range below 10-µA load currents. TPS62745 supports output currents up to 300 mA,

9.2 Typical Application

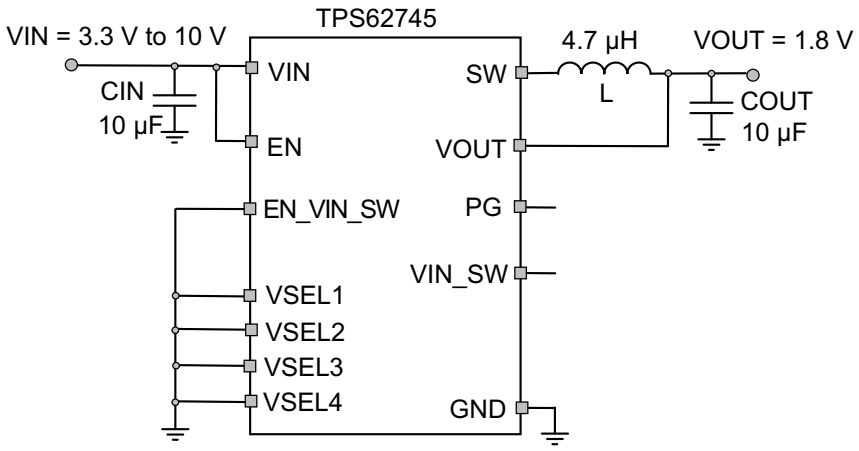


Figure 5. TPS62745 Typical Application

9.2.1 Design Requirements

The TPS62745 is a highly integrated DC/DC converter. The output voltage is set via the VSEL pin interface without any additional external components. For proper operation only an input and output capacitor and an inductor is required. When the input voltage switch is not used, its enable input should be tied to GND. The output VIN_SW can either be left open or tied to GND. Table 3 shows the components used for the application characteristic curves.

Table 3. List of Components

REFERENCE	DESCRIPTION	Value	MANUFACTURER(1)
IC	TPS62745		Texas Instruments
L	DFE252010	4.7 µH	Toko
CIN	TMK212BBJ106MG	10 µF / 25 V / X5R / 0805	Taiyo Yuden
COUT	LMK212ABJ106KG-T	10 µF / 10 V / X5R / 0805	Taiyo Yuden

(1) See *Third-Party Products Disclaimer*

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Selection (VSEL1 - 4)

The VSEL pins select the output voltage of the converters. See the *Output Voltage Selection (VSEL1 - 4)* of the Feature Descriptions. The output voltage can be changed during operation by changing the logic level of these pins. The output voltage of the TPS62745 ramps to the new target with a slew rate as defined in the electrical characteristics. Typically these pins are driven by an applications processor with an I/O voltage of either 1.8 V or 3.3 V or hard wired to a logic high or logic low signal. In case the pins are not driven from an applications processor and the supply voltage is higher than the voltage rating of the VSEL pins, a logic high level can be taken from the output voltage at pin VOUT. During start-up, when the output is rising from 0 V to its target, the VSEL pins connected to VOUT will change their logic level from low to high. TPS62745 is designed such that such a configuration ensures a steadily rising output voltage.

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS62745 is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter. Table 4 can be used to simplify the output filter component selection.

Table 4. Recommended LC Output Filter Combinations

Inductor Value [µH](1)	Output Capacitor Value [µF](2)	
	10 µF	22 µF
4.7	√(3)	√
3.3	√	√

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

9.2.2.3 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where:

- f = Switching frequency
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance R_{DC}) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used:

Table 5. List of Inductors

INDUCTANCE [µH]	DCR [Ω], typical	DIMENSIONS [mm³]	INDUCTOR TYPE	SUPPLIER(1)
4.7	0.250	2.5 x 2.0 x 1.0	DFE252010	TOKO
3.3	0.190	2.5 x 2.0 x 1.0	DFE252010	TOKO
4.7	0.336	2.0 x 1.9 x 1.0	XPL2010	Coilcraft
3.3	0.207	2.0 x 1.9 x 1.0	XPL2010	Coilcraft
4.7	0.217	3.0 x 3.0 x 1.1	XFL3010	Coilcraft
4.7	0.270	4.5 x 3.2 x 3.2	CC453232	Bourns

(1) See *Third-Party Products Disclaimer*

9.2.2.4 DC/DC Output Capacitor Selection

The DCS-Control™ scheme of the TPS62745 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. A larger output capacitor can be used, but it should be considered that larger output capacitors lead to an increased leakage current in the capacitor and may reduce overall conversion efficiency. Furthermore, larger output capacitors impact the start up behavior of the DC/DC converter. Furthermore, the contol loop of the TPS62745 requires a certain voltage ripple across the output capacitor. Super-capacitors can be used in parallel to the ceramic capacitors when it is made sure that the super-capacitors series resistance is large enough to provide a valid feedback signal to the error amplifier which is in phase with the inductor current. Applications using an output capacitance above of what is stated under Recommended Operating Conditions should be checked for stability over the desired operating conditions range.

9.2.2.5 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10 µF or 4.7 µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Table 6 shows a list of tested input/output capacitors.

Table 6. List of Input and Output Capacitors

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER(1)
10	0603	GRM188R61C106MA73	Murata
10	0603	EMK107BBJ106MA	Taiyo Yuden
4.7	0805	EMK212ABJ475KG	Taiyo Yuden
10	0805	TMK212BBJ106MG	Taiyo Yuden
10	0805	LMK212ABJ106KG-T	Taiyo Yuden

(1) See *Third-Party Products Disclaimer*

9.2.3 Application Curves

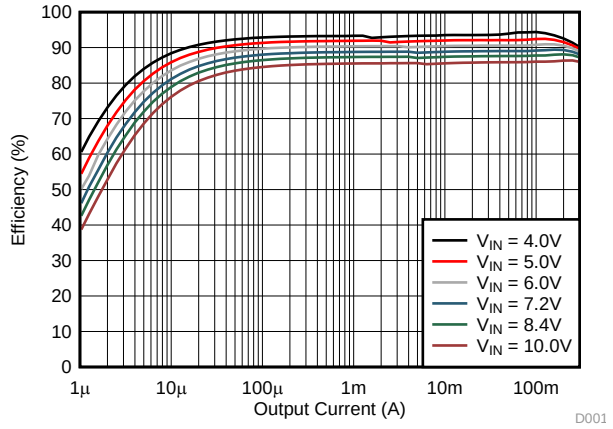


Figure 6. V_{OUT} = 3.3 V

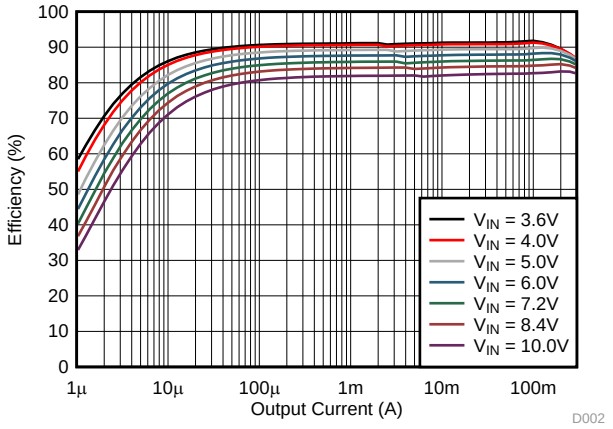


Figure 7. V_{OUT} = 2.5 V

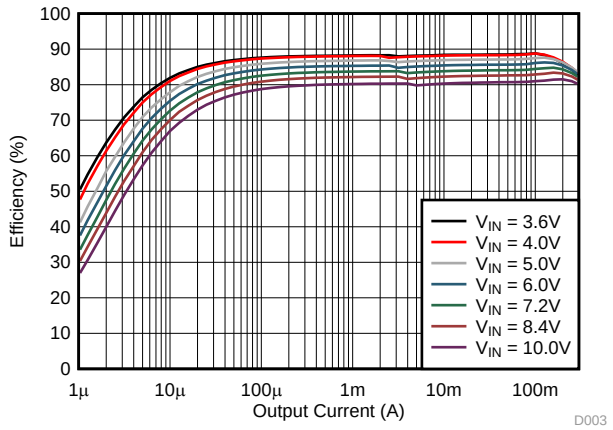


Figure 8. V_{OUT} = 1.8 V

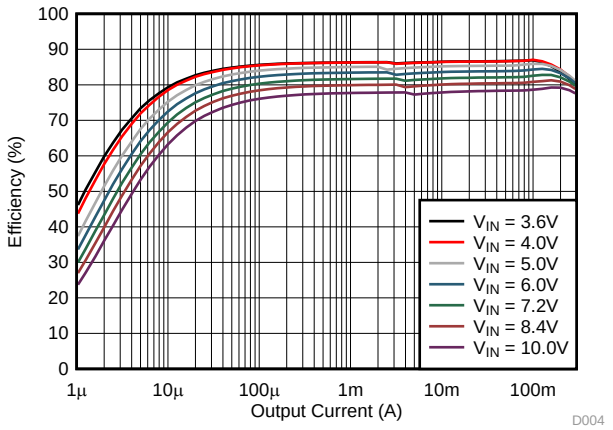


Figure 9. V_{OUT} = 1.5 V

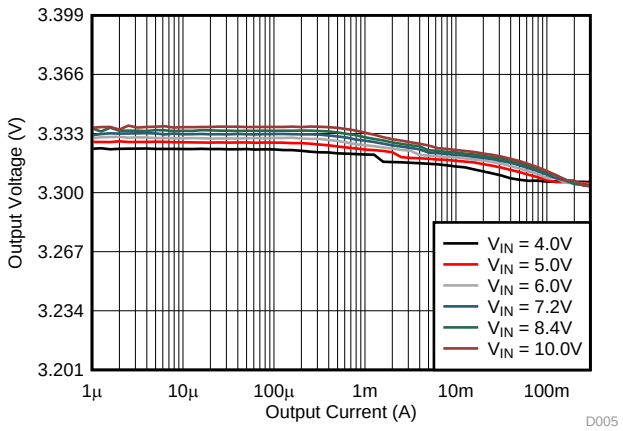


Figure 10. V_{OUT} = 3.3 V

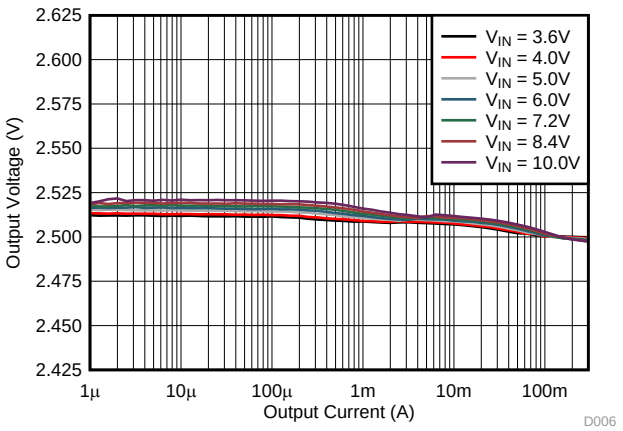


Figure 11. V_{OUT} = 2.5 V

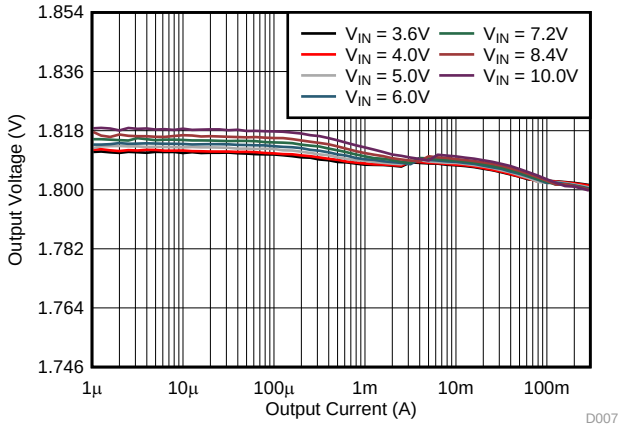


Figure 12. V_{OUT} = 1.8 V

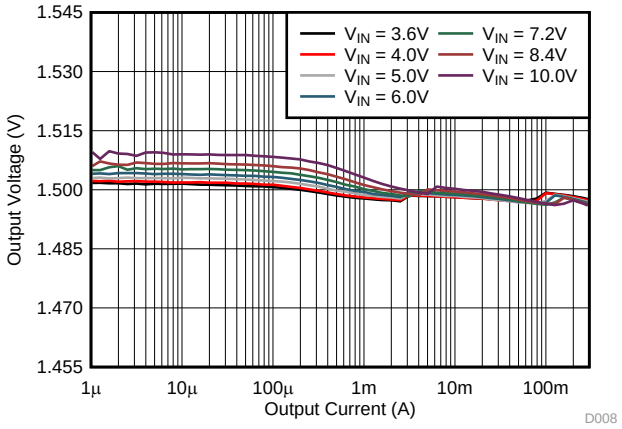


Figure 13. V_{OUT} = 1.5 V

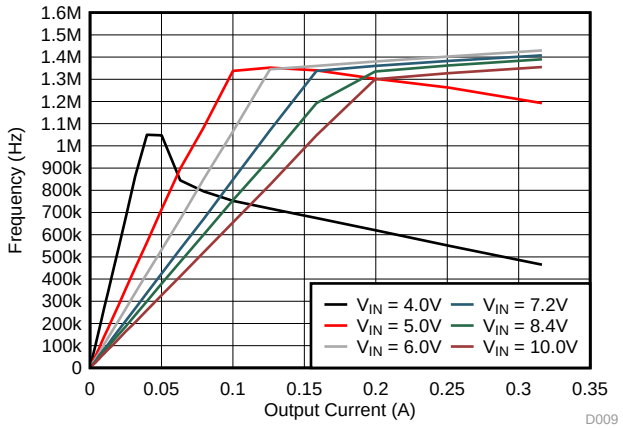


Figure 14. V_{OUT} = 3.3 V

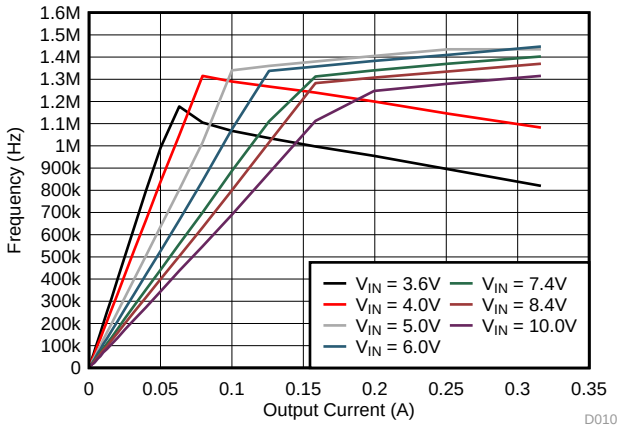


Figure 15. V_{OUT} = 2.5 V

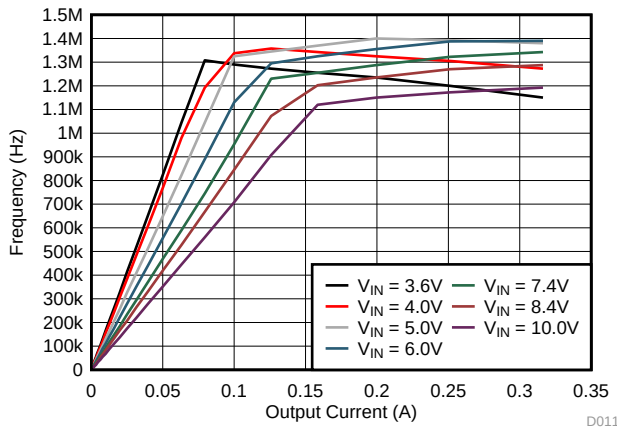


Figure 16. V_{OUT} = 1.8 V

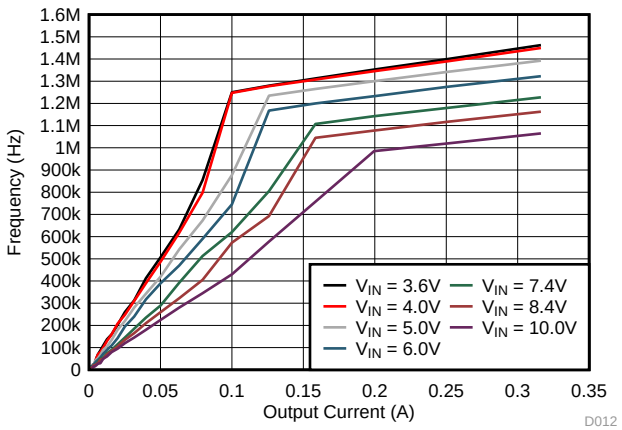


Figure 17. V_{OUT} = 1.5 V

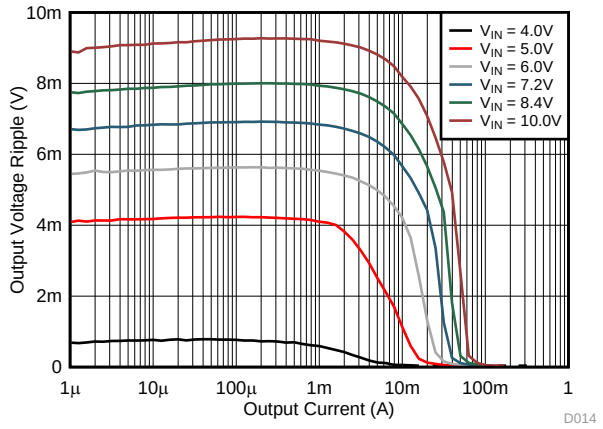


Figure 18. V_{OUT} = 3.3 V

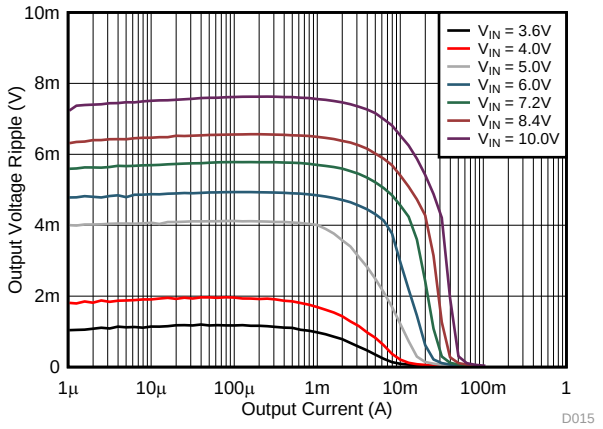


Figure 19. V_{OUT}= 2.5 V

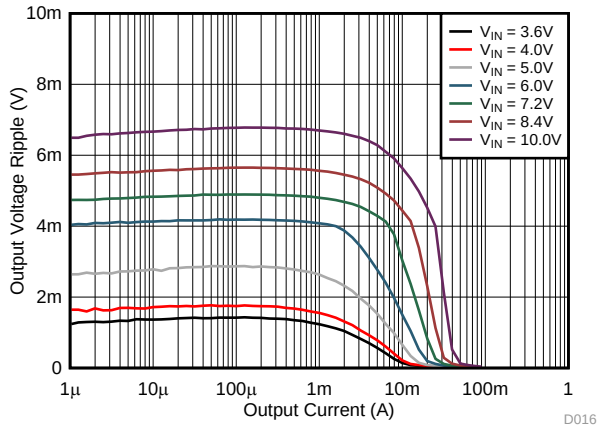


Figure 20. V_{OUT} = 1.8 V

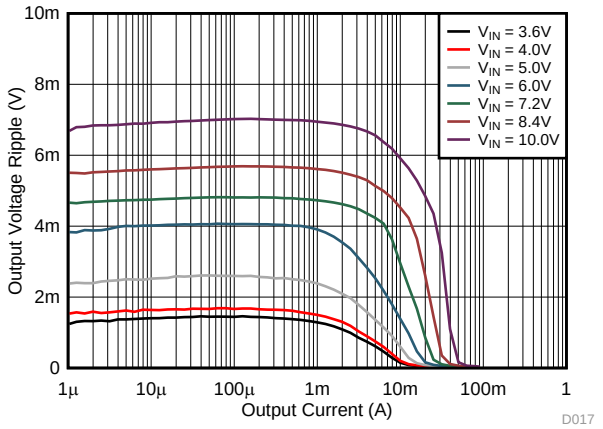


Figure 21. V_{OUT}= 1.5 V

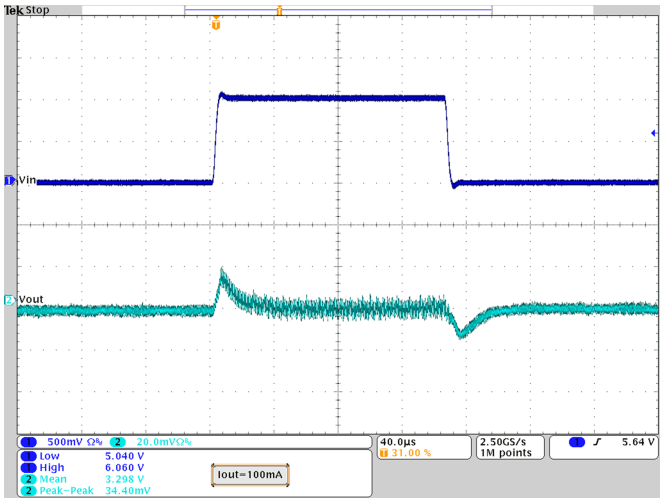


Figure 22. Line Transient Response; V_{OUT} = 3.3 V

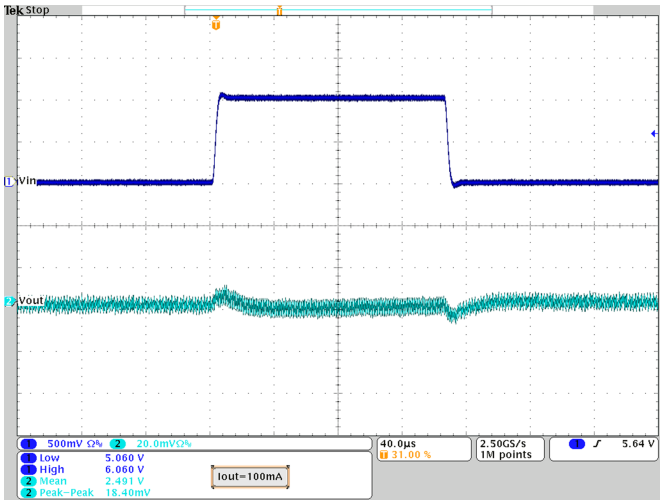


Figure 23. Line Transient Response; V_{OUT} = 2.5 V

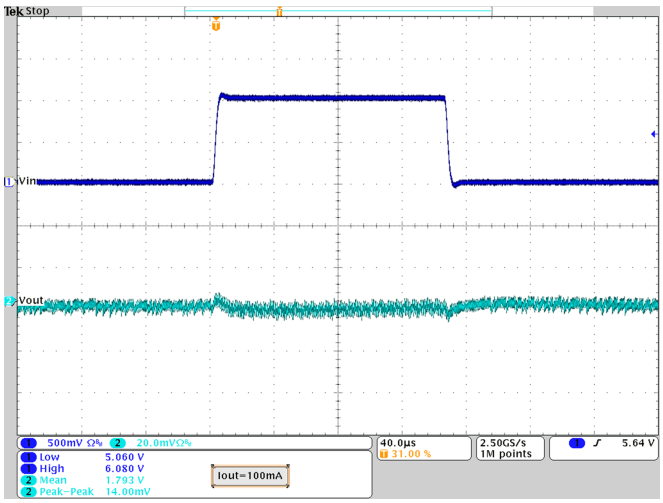


Figure 24. Line Transient Response; V_{OUT} = 1.8 V

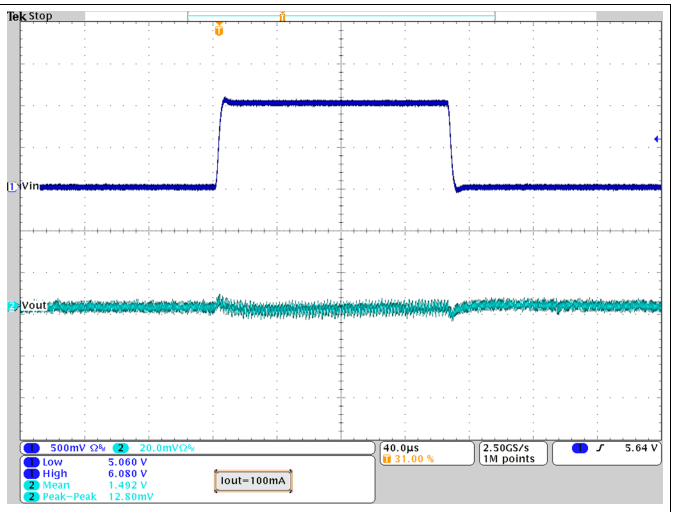


Figure 25. Line Transient Response; V_{OUT} = 1.5 V

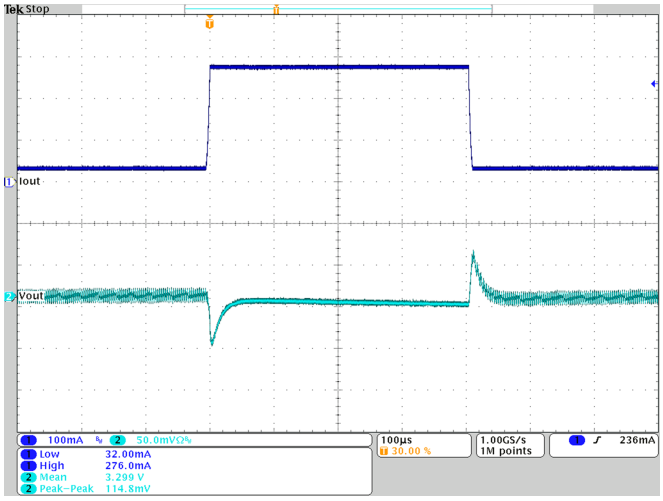


Figure 26. Load Transient Response; V_{OUT} = 3.3 V

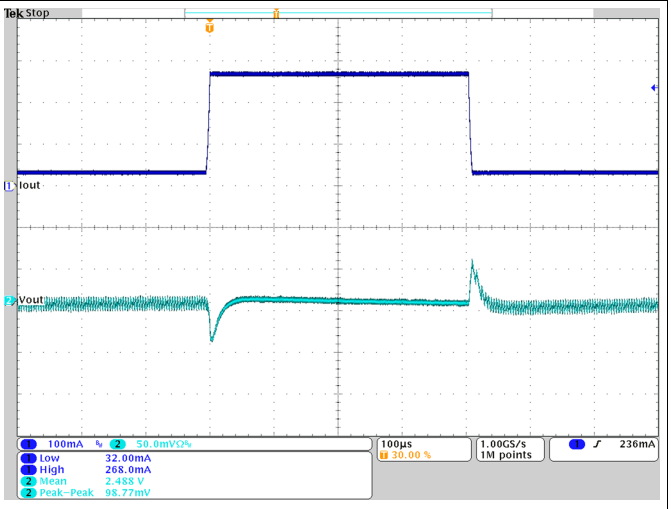


Figure 27. Load Transient Response; V_{OUT} = 2.5 V

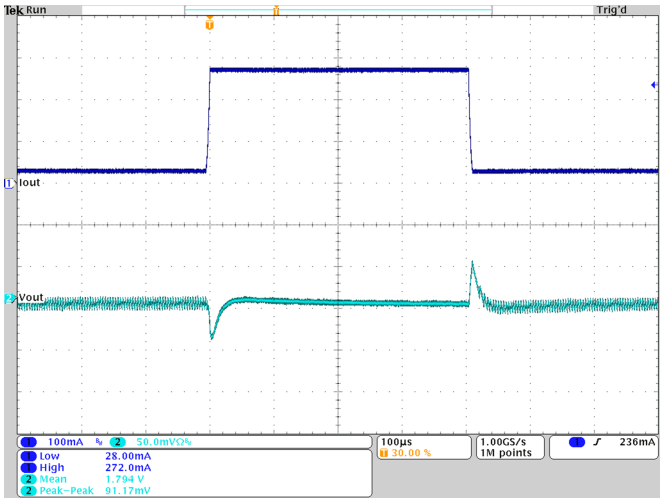


Figure 28. Load Transient Response; V_{OUT} = 1.8 V

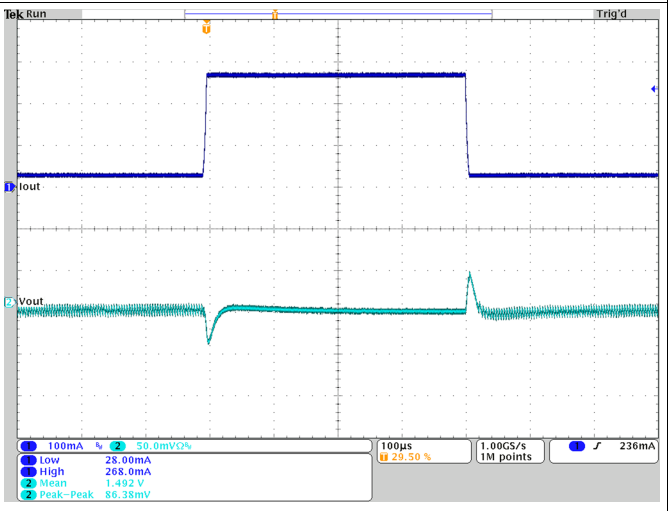


Figure 29. Load Transient Response; V_{OUT} = 1.5 V

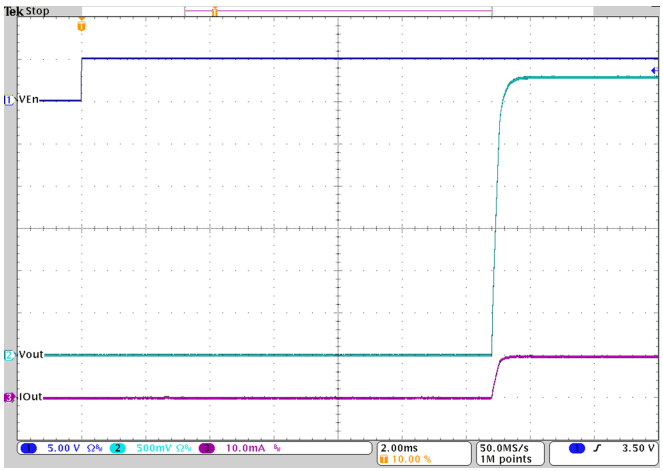


Figure 30. Startup with V_{OUT} = 3.3 V

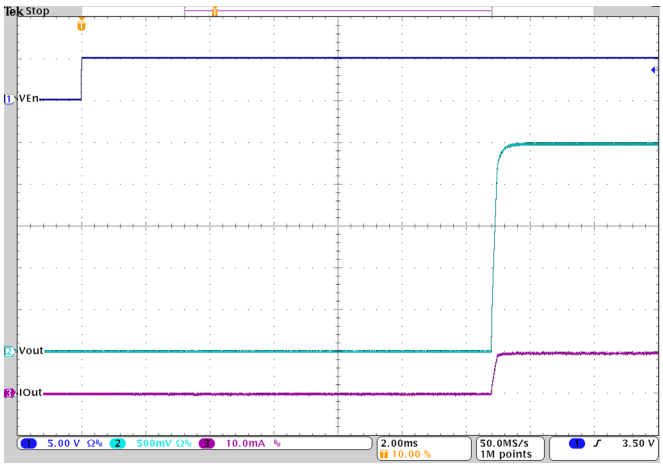


Figure 31. Startup with V_{OUT} = 2.5 V

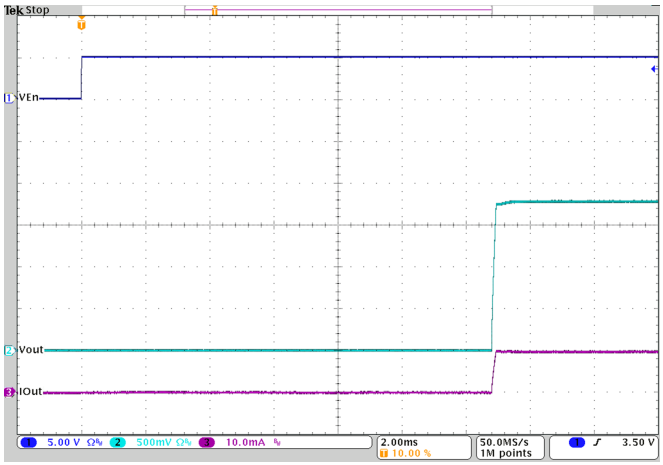


Figure 32. Startup with V_{OUT} = 1.8 V

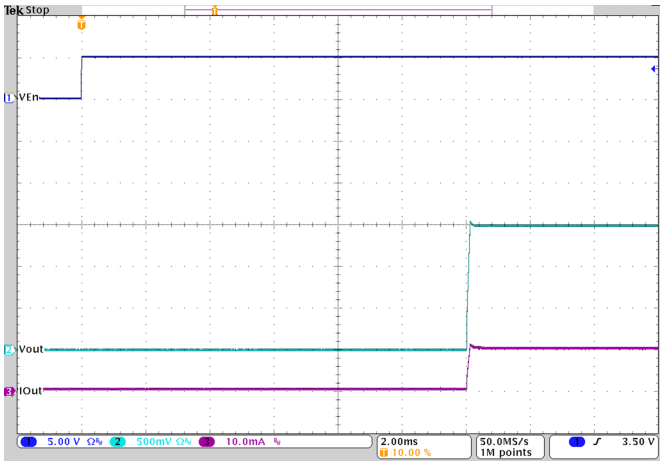


Figure 33. Startup with V_{OUT} = 1.5 V

9.3 System Examples

9.3.1 TPS62745 Set to a Fixed Voltage of 3.3 V

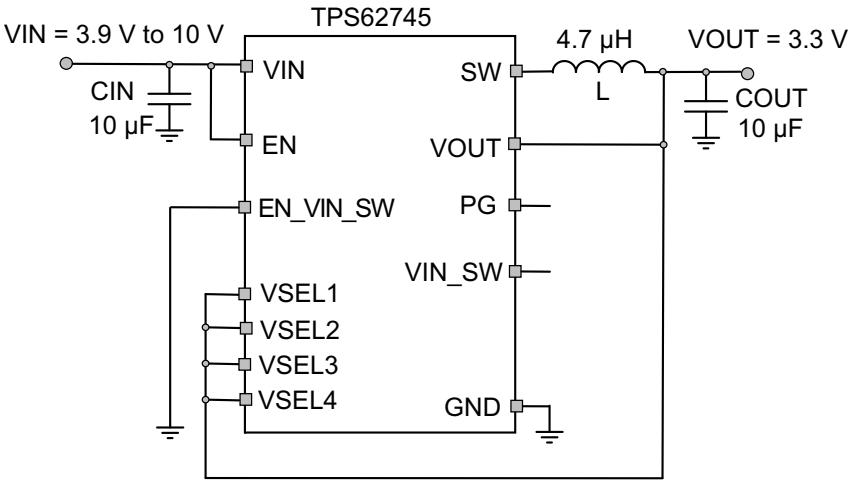


Figure 34. TPS62745 Typical Application for Vout = 3.3 V

9.3.1.1 Design Requirements

The minimum input voltage needs to be at least 700 mV above the desired output voltage for full output current.

Table 7. List of Components

REFERENCE	DESCRIPTION	Value	MANUFACTURER(1)
IC	TPS62745		Texas Instruments
L	DFE252010	4.7 µH	Toko
CIN	TMK212BBJ106MG	10 µF / 25 V / X5R / 0805	Taiyo Yuden
COUT	LMK212ABJ106KG-T	10 µF / 10 V / X5R / 0805	Taiyo Yuden

(1) See *Third-Party Products Disclaimer*

9.3.1.2 Detailed Design Procedure

The logic level of the VSEL pins sets the output voltage. The maximum high level does not allow a direct connection to the supply voltage if it is above 6 V. The output voltage can be used instead to provide a logic high level.

9.3.1.3 Application Curves

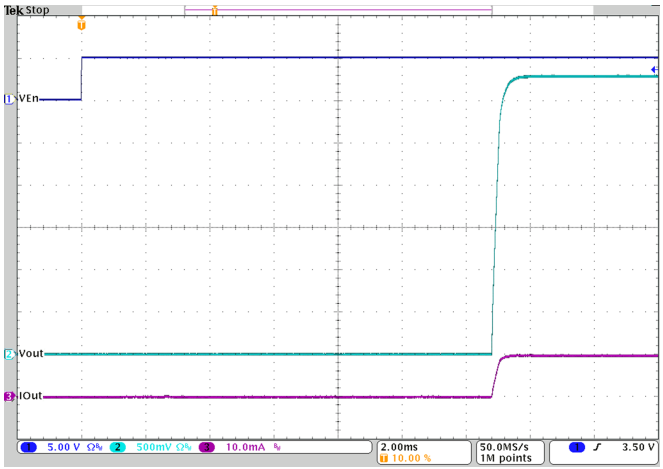


Figure 35. TPS62745 with V_{OUT} = 3.3 V Startup

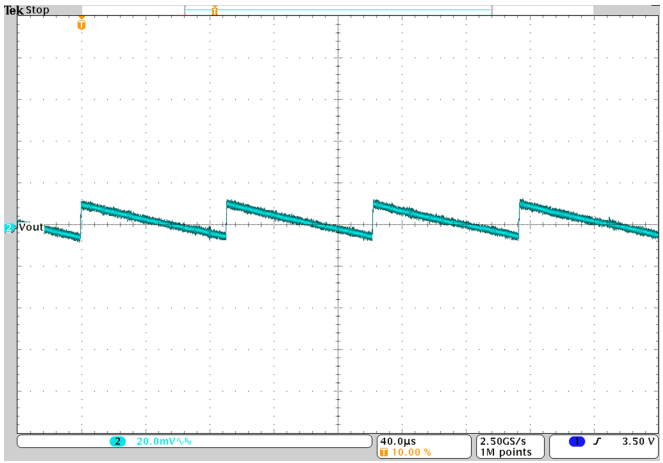


Figure 36. TPS62745 with V_{OUT} = 3.3 V; Output Voltage Ripple for I_{OUT} = 1 mA

9.3.2 Dynamic Voltage Change on TPS62745

TPS62745 allows to change its output voltage during operation by changing the logic level of the VSEL pins.

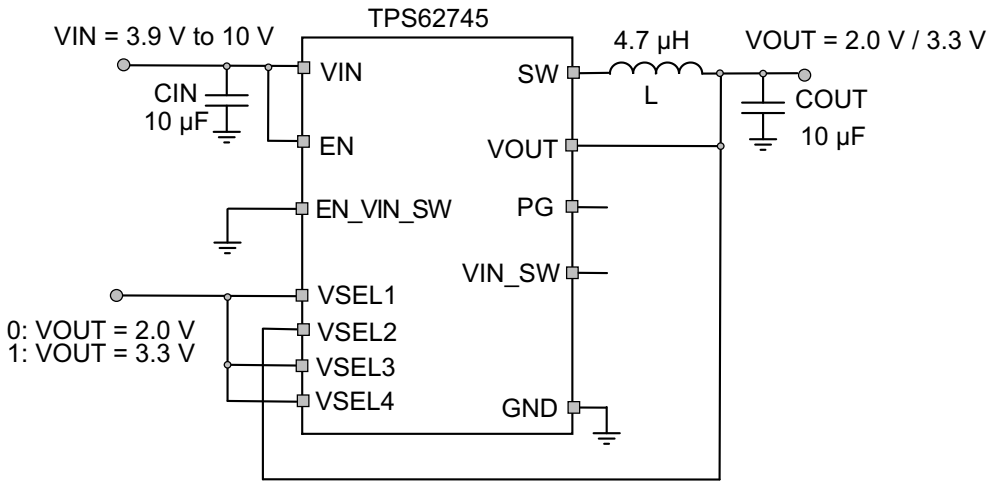


Figure 37. TPS62745 Typical Application for Switching Between Two Output Voltages

9.3.2.1 Design Requirements

The minimum input voltage needs to be at least 700 mV above the maximum output voltage for full output current. For an input voltage above 6V, the VSELx pins have to be tied to the output for a logic high level as their voltage rating is 6V.

Table 8. List of Components

REFERENCE	DESCRIPTION	Value	MANUFACTURER(1)
IC	TPS62745		Texas Instruments
L	DFE252010	4.7 µH	Toko
CIN	TMK212BBJ106MG	10 µF / 25 V / X5R / 0805	Taiyo Yuden
COUT	LMK212ABJ106KG-T	10 µF / 10 V / X5R / 0805	Taiyo Yuden

(1) See *Third-Party Products Disclaimer*

9.3.2.2 Detailed Design Procedure

Toggle the logic level at VSEL1, VSEL3 and VSEL4 to change the output voltage from 2.0 V to 3.3 V and vice versa. The slope from higher output voltage to the lower output voltage is determined by the load current and output capacitance because the discharge of the output capacitor is through the load current only.

9.3.2.3 Application Curves

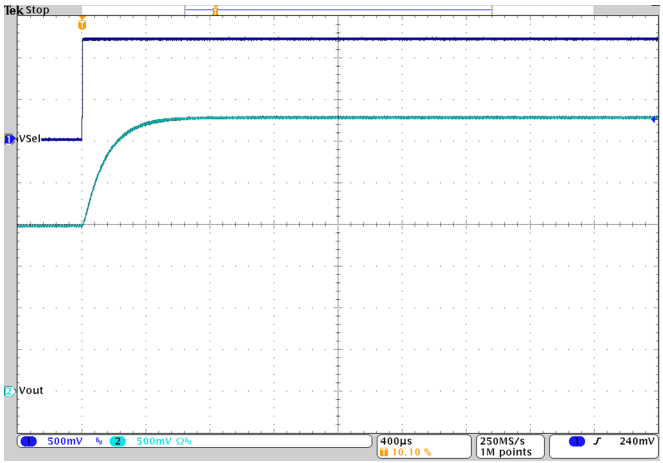


Figure 38. TPS62745 Output Voltage Change from 2.0 V to 3.3 V for I_{OUT} = 10 mA

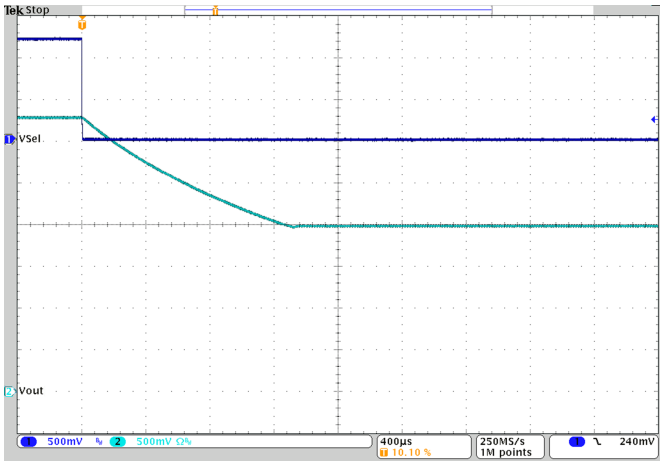


Figure 39. TPS62745 Output Voltage Change from 3.3 V to 2.0 V for I_{OUT} = 10 mA

10 Power Supply Recommendations

The power supply to the TPS62745 needs to have a current rating according to the supply voltage, output voltage and output current of the TPS62745 shown in the *Specifications* section.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Especially RF designs demand careful attention to the PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line).

11.2 Layout Example

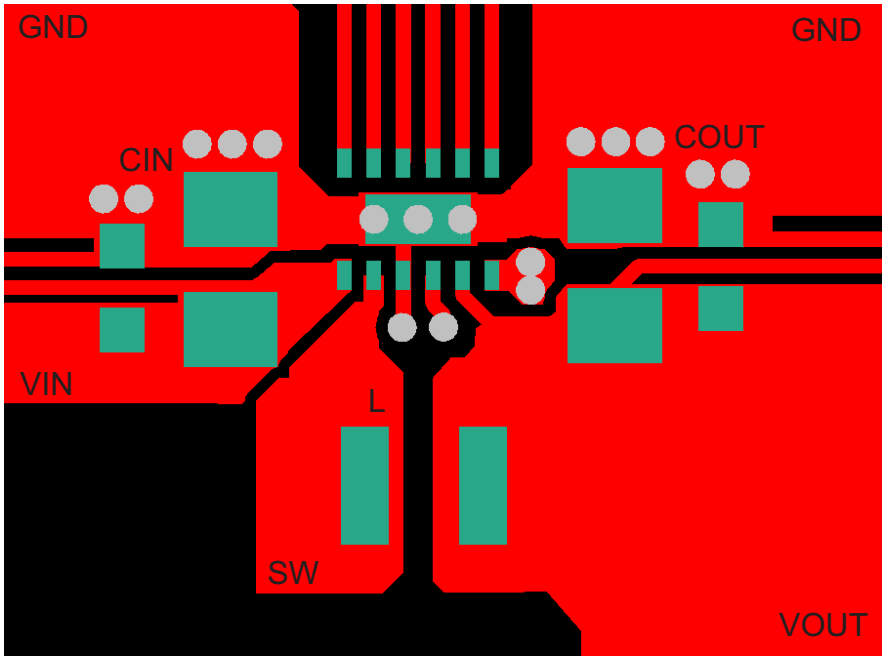


Figure 40. Recommended PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62745	Click here	Click here	Click here	Click here	Click here
TPS627451	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS627451DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD6I	Samples
TPS627451DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD6I	Samples
TPS62745DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD5I	Samples
TPS62745DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD5I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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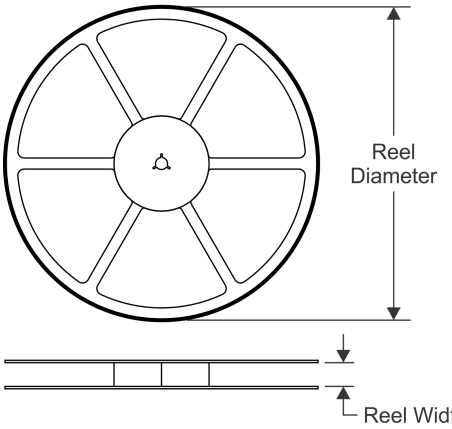
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

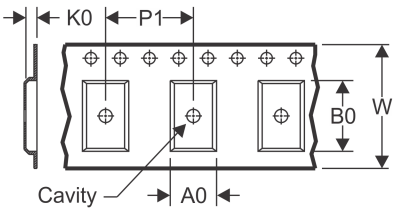
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

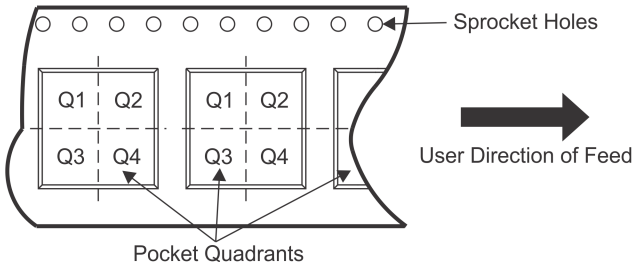


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

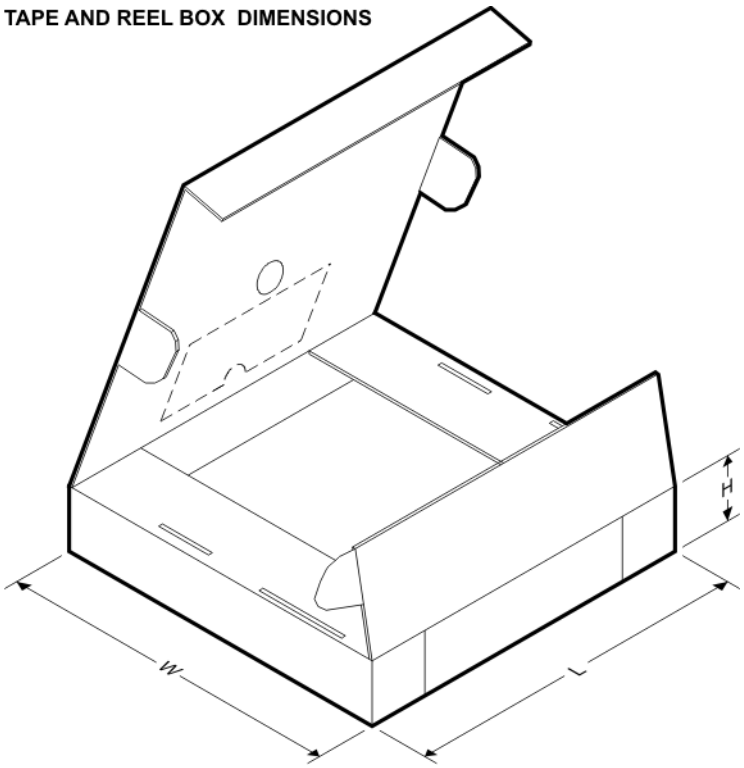
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS627451DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS627451DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62745DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62745DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



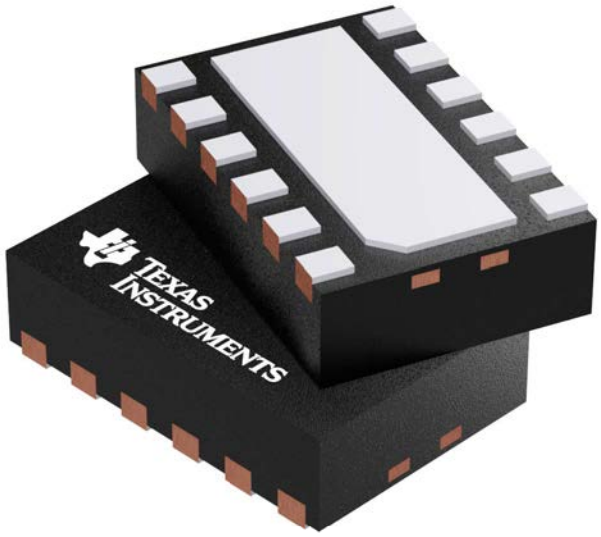
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS627451DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS627451DSST	WSON	DSS	12	250	210.0	185.0	35.0
TPS62745DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS62745DSST	WSON	DSS	12	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



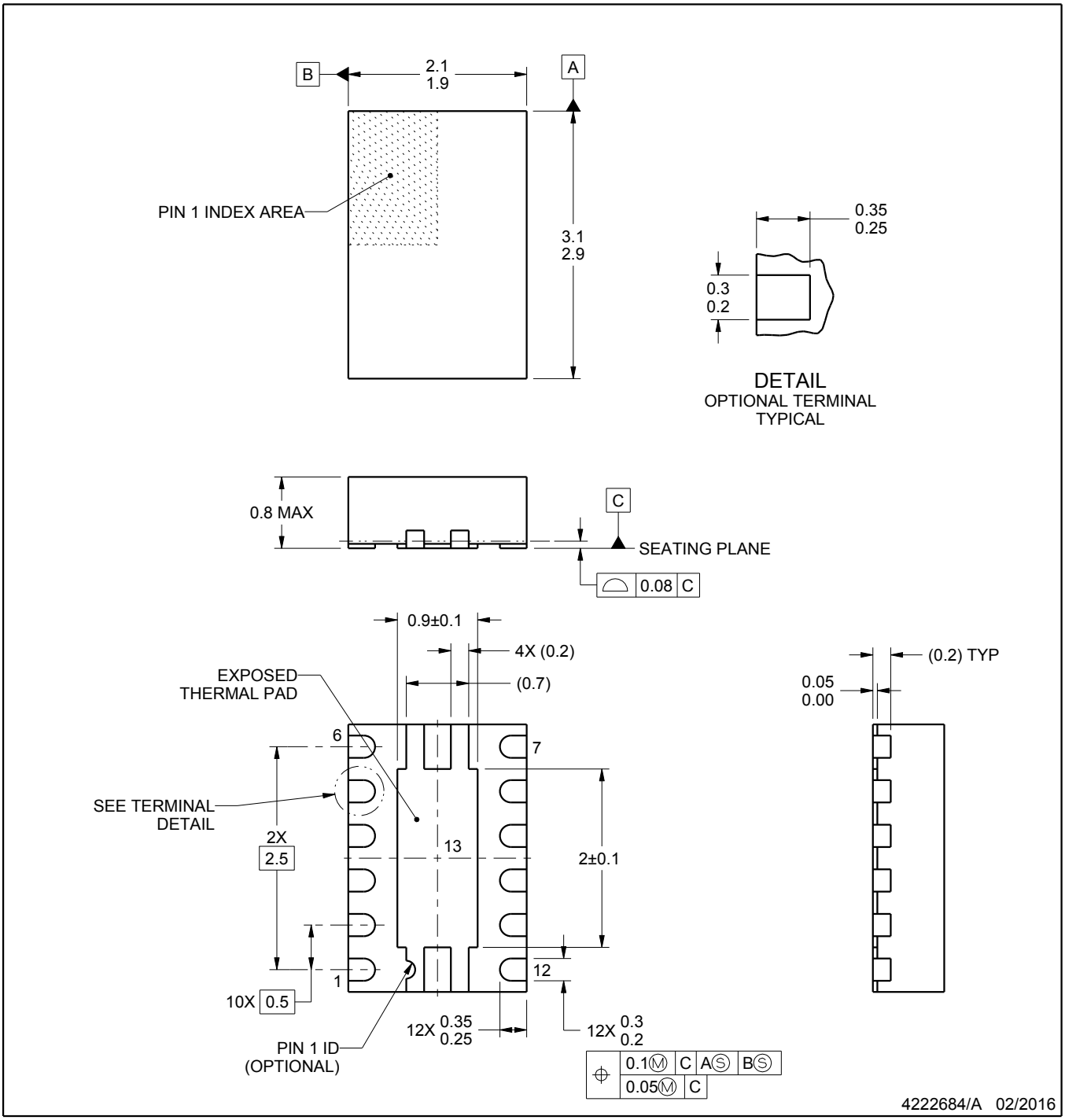
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012A

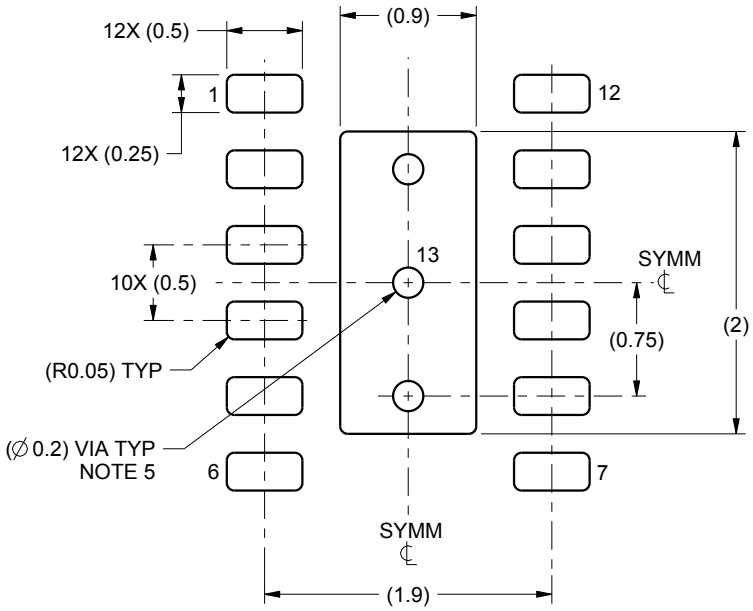
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

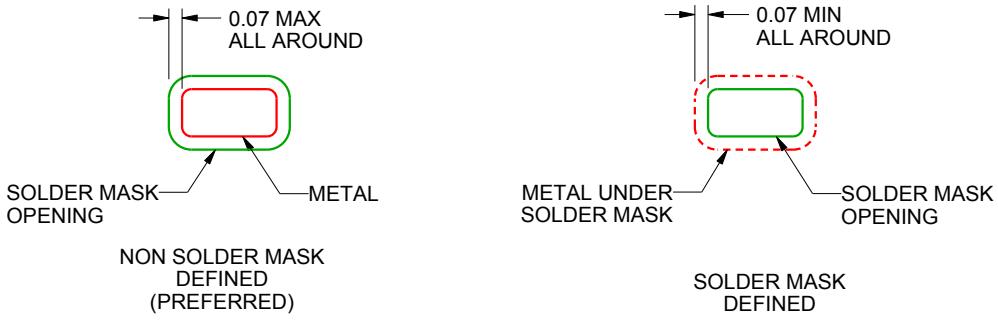


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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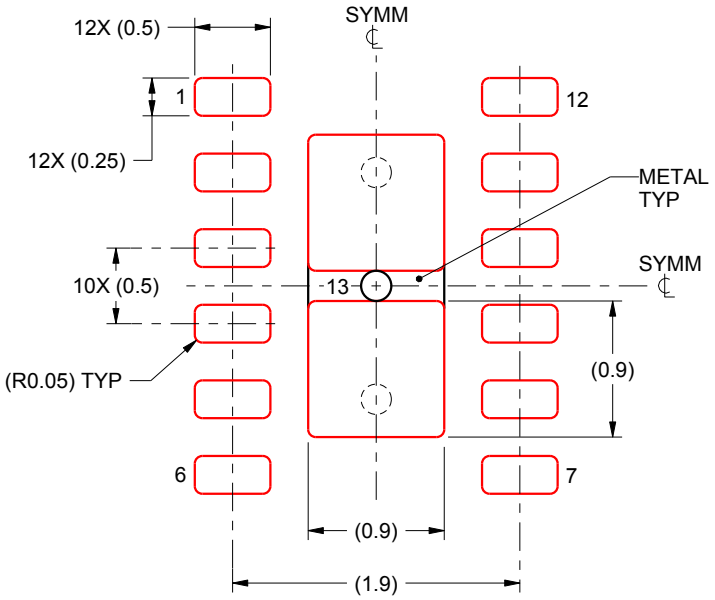
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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