











TPS650842

SWCS132 - AUGUST 2015

TPS650842 PMIC for Intel™ Braswell Platform

Device Overview

1.1 **Features**

- Wide V_{IN} Range From 5.6 V to 21 V
- Three Variable-Output Voltage Synchronous Step-Down Controllers With D-CAP2™ Topology
 - Up to 7-A Output Current for BUCK1 (VCC) and BUCK6 (VDDQ), and 11 A for BUCK2 (VGG) Using External FETs
 - I²C Dynamic Voltage Scaling (DVS) Control (0.5 V to 1.45 V in 10-mV Steps) for BUCK1 BUCK2, and BUCK3
 - Pin-Selectable Dual Output Voltages (1.2 V or 1.35 V) for BUCK6 (VDDQ)
- Three Variable-Output Voltage Synchronous Step-Down Converters With DCS-Control Topology
 - V_{IN} Range From 4.5 V to 5.5 V
 - Up to 3.5 A of Output Current for BUCK3 (VNN) With I²C DVS Control (0.65 V to 1.45 V in 25-mV Steps)
 - Up to 3 A of Output Current for BUCK4 (V1P05A) and up to 1.5 A of Output Current for

1.2 Applications

- 2-, 3-, or 4-Series Cell Li-Ion Battery-Powered Products (NVDC or Non-NVDC)
- Wall-Powered Designs, Particularly From 12-V Supply

BUCK5 (V1P8A)

- Three LDO Regulators With Adjustable Output Voltage
 - LDOA1: I²C-Selectable Output Voltage From 1.35 V to 3.3 V for up to 200 mA of Output Current
 - LDOA2: I²C-Selectable Output Voltage From 1.05 V, 1.1 V, 1.15 V, and 1.2 V
 - LDOA3: I²C-Selectable Output Voltage From 1.1 V, 1.15 V, 1.2 V, and 1.24 V
- VTT LDO for DDR Memory Termination
- Three Load Switches With Slew Rate Control
 - Up to 300 mA of Output Current With Voltage Drop Less Than 1.5% of Nominal Input Voltage
 - R_{DSON} < 96 mΩ at Input Voltage of 1.8 V
- I²C Interface (Device Address 0x5E) Supports:
 - Standard Mode (100 kHz)
 - Fast Mode (400 kHz)
 - Fast Mode Plus (1 MHz)
- Tablets, Ultrabook™, and Notebook Computers
- Mobile PCs and Mobile Internet Devices

Description 1.3

The TPS650842 device is a single-chip solution, power-management integrated chip (PMIC) designed specifically for the latest Intel™ processors targeted for tablets, ultrabooks, notebooks, industrial PCs, and Internet-of-Things (IOT) applications using 2S, 3S, or 4S Li-Ion battery packs (NVDC or non-NVDC power architectures), as well as wall-powered applications. The TPS650842 device is used for essential systems with low-voltage rails merged for the smallest footprint and lowest-cost system-power solution. The TPS650842 device provides the complete power solution based on the Intel Reference Designs. Six highly efficient step-down voltage regulators (VRs), a sink or source LDO (VTT), two LDOs, and three load switches are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The three regulators (BUCK-BUCK3) support dynamic voltage scaling (DVS) for maximum efficiency—including support for Connected Standby. The high-frequency VRs use small inductors and capacitors to achieve a small solution size. An I²C interface allows simple control by an embedded controller (EC) or by a system on chip (SoC). The PMIC comes in an 8-mm × 8-mm single-row VQFN package with a thermal pad for good thermal dissipation and ease of board routing.

Use the following email address to request the full version of this data sheet: ipgmkt@list.ti.com.

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Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) | | |
|-------------|-----------|-------------------|--|--|
| TPS650842 | VQFN (64) | 8.00 mm × 8.00 mm | | |

(1) For more information, see the *Mechanical Packaging and Orderable Information* section.

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1.4 Functional Block Diagram

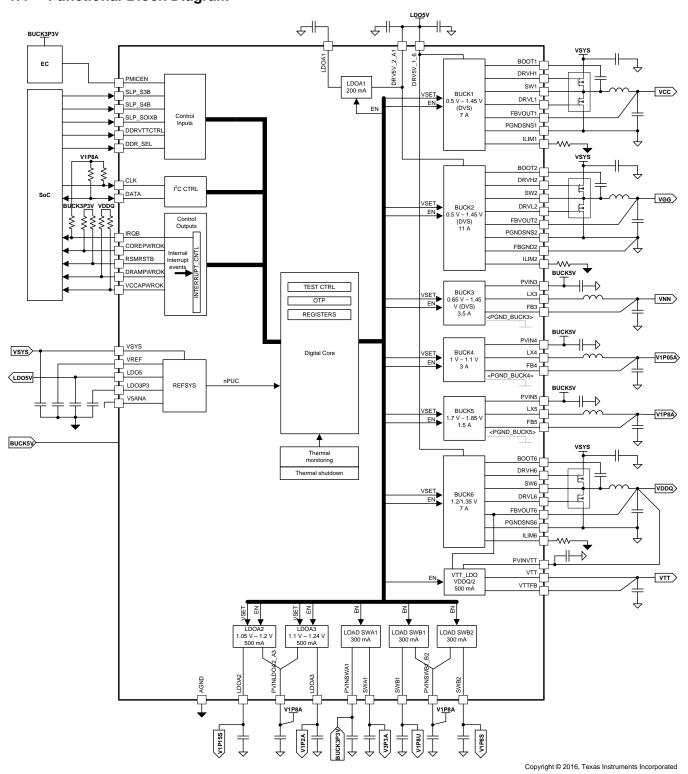


Figure 1-1. PMIC Functional Block Diagram

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TEXAS INSTRUMENTS

2 Device and Documentation Support

2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-ro-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

2.2 Trademarks

D-CAP2, E2E are trademarks of Texas Instruments.
Ultrabook, Intel are trademarks of Intel Corporation.
All other trademarks are the property of their respective owners.

2.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

2.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

3 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGE OPTION ADDENDUM

17-Oct-2018

PACKAGING INFORMATION

| Orderable Device | Status | Package Type | Package Drawing | Pins | Package Qty | Eco Plan | Lead/Ball Finish | MSL Peak Temp | Op Temp (°C) | Device Marking | Samples |
|------------------|--------|--------------|--------------------|------|----------------|----------------------------|------------------|---------------------|--------------|--------------------|---------|
| TPS650842A0RSKT | ACTIVE | VQFN | RSK | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | T650842A0 PG1.0 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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