POWER MANAGEMENT IC FOR DIGITAL STILL CAMERA

FEATURES

- **Highly Efficient, 8-Channel Power Management IC**
- **Fully Integrated Power MOSFETs (Except CH-7)**
- **Minimal External Components**
- **Input Voltage Range: 1.5 to 5 V**
- **Short Circuit Protection (SCP) (Except for CH-6 and CH-8)**
- **Overvoltage Protection (OVP) (CH-2, CH-3, CH-6, and CH-7)**
- **Overcurrent Protection (OCP) (CH-6)**
- **Thermal Shutdown (TSD)**
- **High-Accuracy Output Voltage with Trimming**
- **8 mm x 8 mm BGA Package**

APPLICATIONS

- **Digital Still Cameras**

DESCRIPTION

The TPS65520 is a highly efficient, 8-channel power management IC for digital still cameras (DSCs) integrating power MOSFETs and operating from an input voltage range of 1.5 to 5 V.

Its optimized circuit configuration maintains stable regulation characteristics while minimizing the number of external components required for phase compensation and other purposes.

The TPS65520 controls each output channel by communicating with the Sub-CPU through a serial interface.

NAME(1)	CIRCUIT CONFIGURATION	OUTPUT VOLTAGE [V]	ADJUSTABLE PARAMETER	POWER MOSFET	RECTIFICATION	PURPOSE
CH-1	H-bridge step-up/down	2.65 ~ 3.2	Output voltage	Built-in	Synchronous	CPU, DSP I/F
CH-2	Step-down	1.1 ~ 1.8	Output voltage	Built-in	Synchronous	CPU, DSP core
CH-3	Step-up	4.5 ~ 5.2	Output voltage, duty cycle	Built-in	Synchronous	Motor, audio
CH-4	Step-up	15.0 ~ 16,5	Output voltage, duty cycle	Built-in	Asynchronous, with external rectification diode	LCD, CCD
CH-5	Inversion	–9.0 ~ –7.5	Output voltage, duty cycle	Built-in	Asynchronous, with external rectification diode	LCD, CCD
CH-6	Step-up with constant current control	5.6 ~ 21.0	Output voltage, duty cycle	Built-in	Asynchronous, with external rectification diode	Backlight LED
CH-7	Step-down	2.5 ~ 3.2	Output voltage, duty cycle	External	Synchronous	Reserved/switchable
	Step-up	4.4 ~ 5.1				
CH-8	Step-up/pass-through with skip	3.6 ~ VCC		Built-in	Synchronous	IC internal power supply
LDO-1		2.9				Sub-CPU I/F
LDO-2		2.9				Sub-CPU core
LDO-3		3.1				Charge backup battery
LDO-4		3.1				USB
LDO-5		8.5 ~ 13.5	Output voltage			LCD

(1) CH-N represents switching regulators. LDO-N represents series regulators.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_I	Input voltage range(2)	ROMWR	–0.3 V to 24 V
		MODE7, DIN, CLK, LD, PWR_ON, LDO4_ON, TEST, TLD	–0.3 V to 7 V
		VCH2, VCH7, VCC8	–0.3 V to 6.5 V
		VCC1, VCC2, VCC5, VCC7, VCC_GD	–0.3 V to 6 V
		VCH5	–10.0 V to 0.3 V
V_O	Output voltage range(2)	VCH4, OUT4, VLDO5, VCH6, ICH6, OUT6	–0.3 V to 24 V
		BOOT11, BOOT12, BOOT2	–0.3 V to 11 V
		VOS71, DOUT, XRESET, READY	–0.3 V to 7 V
		ROSC	–0.3 V to 6.5 V
		OUT5	–10.0 V to 5.1 V
		OUT3	–0.3 V to 6 V(3)
		Others	–0.3 V to 6 V
	Peak current of Power Path	VCC1 = OUT11, GND1 = OUT11, OUT12 = VCH1, OUT12 = GND1, OUT3 = VCH3, OUT3 = GND3	–4.5 A to 4.5 A
		OUT8 = VCH8, OUT8 = GND8	–3.0 A to 3 A
		VCC2 = OUT2, GND2 = OUT2, OUT4 = VCH4, OUT4 = GND4, VCC5 = OUT5, OUT6 = VCH6, OUT6 = GND6	–1.5 A to 1.5 A
	Voltage difference between two of any GND pins (name starts with GND)		–0.5 V to 0.5 V
	ESD rating, HBM (Human Body Model)	JEDEC JESD22-A114	1.5 kV
	ESD rating, CDM (Charged Device Model)	JEDEC JESD22-C101	500 V
P_D	Continuous total power dissipation		See Dissipation Rating Table
T_J	Operating virtual junction temperature range		–20°C to 150°C
T_A	Operating ambient temperature range		–20°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.
(2) All voltage values are with respect to network ground terminal.
(3) For the pulse smaller than 5 ns, Maximum rating is 8.6 V.

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C
nFBGA 113(1)	2.99 W	23.9 mW/°C	1.95 W

(1) This data is based on using still air JEDEC environment with 2S2P JEDEC board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC} (1)	Supply voltage	VCC_GD	4.5		5.5	V
		VCC1, VCC2, VCC5, VCC7, VCC8	1.5		5.5	
V_I	Input voltage	TLD,VCH2,VCH7	0.0		5.5	V
		MODE7, DIN, CLK, LD, PWR_ON, LDO4_ON, TEST	0.0		3.3	
		VCH5	–9.5		0.0	
		ROMWR	0.0		0.3	
V_{IH1} (2)	High-level input voltage	ILDO1 = 0 mA	2.4		2.9	V
V_{IL1} (2)	Low-level logic input voltage	ILDO1 = 0 mA	0		0.5	V
V_{IH2}	TLD high-level logic input voltage	Ratio to VCC1A voltage	80%		100 %	
V_{IL2}	TLD low- level logic input voltage		0%		20%	
	Voltage difference between two of any GND pins (name starts with GND)		–0.3		0.3	V
T_A	Operating free-air temperature,		–20		85	°C
	Acceptable number of EEPROM writing (3)				20	Times

(1) These values are defined in stable state. During the start-up, supply voltage sources are OK to be lower than these values.
(2) Logic input pins are PWR_ON, USB ON, DIN, CLK, LD, TEST, and MODE7, except TLD.
(3) This defines the number of customer's writing after TI's shipment.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
ICC1						
ICC CTRL	Supply current for controller	PWR_ON = H, No load current at all outputs (see Table 1)			2.2	mA
IVCC GD	Supply current for gate-drive				5	mA
ICC2A						
IVCH8	Supply current for LDO,control	PWR_ON = L (see Table 2)			40	µA
IVCC8	Supply current for CH-8				1	µA
SUB-CPU CONTROL						
VRDY1	READY threshold, rising edge	Sweep VCH8	3.322	3.4	3.478	V
VRDY2	READY threshold, falling edge		3.234	3.3	3.366	
VRST1	XRESET threshold, rising edge	Sweep VLDO2	2.115	2.184	2.253	V
VRST2	XRESET threshold, falling edge		1.844	1.884	1.924	
IREADY	Sink current of READY	VREADY = 0.5 V	250	500		µA
I_{lkg}	Leakage current of READY	VREADY = 5.25 V, VCH8 = 5.25 V			0.1	µA
IRST	Sink current of XRESET	VXRESET = 0.5 V, VLDO2 = 2 V	150	300		µA
IRSTL	Leakage current of XRESET	VXRESET = 5.25 V, VCH8 = 5.25 V			0.1	µA
REFERENCE AND PROTECTION						
V_{REF}	BG reference voltage, sensed at CBG	I_{REF} = 0 mA	0.842	0.85	0.858	V
ΔVloBG	Load regulation of BG reference voltage buffer	I_{REF} = 0.1 µA ~ 1 mA	–5		5	mV
fosc	Oscillator frequency	ROSC = 150 kΩ	475	500	525	kHz
TSD (1)	Temperature threshold to shutdown		140	155	170	°C

(1) Not production tested. Assured by design.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
I_{SS}	Source current of SS_SYNC	VSS_SYNC = 0.5 V	0.7	1	1.3	µA
	Source current of SS2	VSS2 = 0.5 V	0.7	1	1.3	µA
	Source current of SS3	VSS3 = 0.5 V	0.7	1	1.3	µA
	Source current of SS5	VSS5 = 0.5 V	0.7	1	1.3	µA
	Source current of SS6	VSS6 = 0.5 V	0.7	1	1.3	µA
	Source current of SSLDO5	VSSLDO5 = 0.5 V	0.35		0.65	µA
VSS3OK	SS3OK threshold voltage		1.2	1.6	2	V
LOGIC INPUT/OUTPUT						
V_{OH}(2)	High-level logic output voltage	ILDO1 = 0 mA, IDOUT = –0.5 mA	2.5			V
V_{OL}(2)	Low-level logic output voltage				0.4	
START-UP CIRCUIT						
VWU	Wake-up voltage	Monitoring VCC8			1.6	V
CH-1						
VCH1	Error amp center voltage	Vout1 = 0000(bin), T_A = –10 ~ 65°C	2.744	2.8	2.856	V
		Vout1 = 0001(bin), T_A = –10 ~ 65°C	2.695	2.75	2.805	V
		Vout1 = 0010(bin), T_A = –10 ~ 65°C	2.646	2.7	2.754	V
		Vout1 = 0001(bin), T_A = –10 ~ 65°C	2.597	2.65	2.703	V
		Vout1 = 0100(bin), T_A = –10 ~ 65°C	2.548	2.6	2.652	V
		Vout1 = 0101(bin), T_A = –10 ~ 65°C	2.499	2.55	2.601	V
		Vout1 = 0110(bin), T_A = –10 ~ 65°C	2.450	2.5	2.550	V
		Vout1 = 0111(bin), T_A = –10 ~ 65°C	3.138	3.2	3.264	V
		Vout1 = 1000(bin), T_A = –10 ~ 65°C	3.087	3.15	3.213	V
		Vout1 = 1001(bin), T_A = –10 ~ 65°C	3.038	3.1	3.162	V
		Vout1 = 1010(bin), T_A = –10 ~ 65°C	2.989	3.05	3.111	V
		Vout1 = 1011(bin), T_A = –10 ~ 65°C	2.940	3	3.060	V
		Vout1 = 1100(bin), T_A = –10 ~ 65°C	2.891	2.95	3.009	V
		Vout1 = 1101(bin), T_A = –10 ~ 65°C	2.842	2.9	2.958	V
		Vout1 = 1110(bin), T_A = –10 ~ 65°C	2.793	2.85	2.907	V
		Vout1 = 1111(bin), T_A = –10 ~ 65°C	2.769	2.825	2.88	V
gm1	gm value of error amp		0.8	1	1.2	mS
VOCH1(3)	Output voltage	On EVM, T_A = –10 ~ 65°C	2.744	2.8	2.856	V
ΔVli11(3)	Line regulation (CROSS state)	On EVM	–28		28	mV
ΔVli12(3)	Line regulation (DOWN state)	On EVM	–28		28	mV
ΔVlo11(3)	Load regulation (CROSS state)	On EVM	–28		28	mV
ΔVlo12(3)	Load regulation (DOWN state)	On EVM	–28		28	mV
IOUT1(3)	Minimum Load current	On EVM, VCC1=1.8 V	400			mA
VSCP1	SCP detector threshold	Ratio to VCH1	75%	80%	85%	
Vmod11	Mode selector threshold, rising edge	Ratio to VCH1	130%	135%	137%	
Vmod12	Mode selector threshold, falling edge	Ratio to VCH1	120%	125%	127%	

(2) Logic output pin is DOUT.
(3) Not production tested. Assured by design. Using reference EVM.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CH-2						
VCH2	Error amp center voltage	Vout2 = 0000(bin), T_A = –10 ~ 65°C	1.176	1.2	1.224	V
		Vout2 = 0001(bin), T_A = –10 ~ 65°C	1.127	1.15	1.173	V
		Vout2 = 0010(bin), T_A = –10 ~ 65°C	1.078	1.1	1.122	V
		Vout2 = 0011(bin), T_A = –10 ~ 65°C	1.764	1.8	1.836	V
		Vout2 = 0100(bin), T_A = –10 ~ 65°C	1.715	1.75	1.785	V
		Vout2 = 0101(bin), T_A = –10 ~ 65°C	1.666	1.7	1.734	V
		Vout2 = 0110(bin), T_A = –10 ~ 65°C	1.617	1.65	1.683	V
		Vout2 = 0111(bin), T_A = –10 ~ 65°C	1.568	1.6	1.632	V
		Vout2 = 1000(bin), T_A = –10 ~ 65°C	1.519	1.55	1.581	V
		Vout2 = 0001(bin), T_A = –10 ~ 65°C	1.470	1.5	1.530	V
		Vout2 = 1010(bin), T_A = –10 ~ 65°C	1.421	1.45	1.479	V
		Vout2 = 1011(bin), T_A = –10 ~ 65°C	1.372	1.4	1.428	V
		Vout2 = 1100(bin), T_A = –10 ~ 65°C	1.323	1.35	1.377	V
		Vout2 = 1101(bin), T_A = –10 ~ 65°C	1.274	1.3	1.326	V
		Vout2 = 1110(bin), T_A = –10 ~ 65°C	1.225	1.25	1.275	V
		Vout2 = 1111(bin), T_A = –10 ~ 65°C	1.201	1.225	1.250	V
gm2	gm value of error amp		0.8	1	1.2	mS
VoCH2(3)	Output voltage	On EVM, T_A = –10 ~ 65°C	1.176	1.2	1.224	V
ΔVli12(3)	Line regulation	On EVM	–12		12	mV
ΔVlo2(3)	Load regulation	On EVM	–12		12	mV
IOUT2(3)	Minimum load current	On EVM, VCC2=4.2 V	500			mA
VSCP2	SCP detector threshold	Ratio to VCH2	75%	80%	85%	
VOVP2	OVP detector threshold	Ratio to VCH2	115%	120%	125%	
CH-3						
VCH3	Error amp center voltage	Vout1 = 0000(bin), T_A = –10 ~ 65°C	4.802	4.9	4.998	V
		Vout1 = 0001(bin), T_A = –10 ~ 65°C	4.753	4.85	4.947	V
		Vout1 = 0010(bin), T_A = –10 ~ 65°C	4.704	4.8	4.896	V
		Vout1 = 0001(bin), T_A = –10 ~ 65°C	4.655	4.75	4.845	V
		Vout1 = 0100(bin), T_A = –10 ~ 65°C	4.606	4.7	4.794	V
		Vout1 = 0101(bin), T_A = –10 ~ 65°C	4.557	4.65	4.743	V
		Vout1 = 0110(bin), T_A = –10 ~ 65°C	4.508	4.6	4.692	V
		Vout1 = 0111(bin), T_A = –10 ~ 65°C	4.459	4.55	4.641	V
		Vout1 = 1000(bin), T_A = –10 ~ 65°C	4.410	4.5	4.590	V
		Vout1 = 1001(bin), T_A = –10 ~ 65°C	5.096	5.2	5.304	V
		Vout1 = 1010(bin), T_A = –10 ~ 65°C	5.047	5.15	5.253	V
		Vout1 = 1011(bin), T_A = –10 ~ 65°C	4.998	5.10	5.202	V
		Vout1 = 1100(bin), T_A = –10 ~ 65°C	4.949	5.05	5.151	V
		Vout1 = 1101(bin), T_A = –10 ~ 65°C	4.900	5	5.100	V
		Vout1 = 1110(bin), T_A = –10 ~ 65°C	4.851	4.95	5.049	V
		Vout1 = 1111(bin), T_A = –10 ~ 65°C	4.802	4.9	4.998	V
gm3	gm value of error amp		0.8	1	1.2	mS
VoCH3(4)	Output voltage	On EVM, T_A = –10 ~ 65°C	4.802	4.90	4.998	V
ΔVli3(4)	Line regulation	On EVM	–49		49	mV
ΔVlo3(4)	Load regulation	On EVM	–49		49	mV
IOUT3(4)	Minimum Load current	On EVM, [CH-3 input voltage]=1.8 V	500			mA
VSCP3	SCP detector threshold	Ratio to VCH3	75%	80%	85%	
VOVP3	OVP detector threshold	Ratio to VCH3		5.99		V

(4) Not production tested. Assured by design. Using reference EVM.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CH-4						
VCH4	Error amp center voltage	Vout4 = 00(bin), T_A = –10 ~ 65°C	14.700	15	15.300	V
		Vout4 = 01(bin), T_A = –10 ~ 65°C	15.190	15.5	15.810	V
		Vout4 = 10(bin), T_A = –10 ~ 65°C	15.680	16	16.320	V
		Vout4 = 11(bin), T_A = –10 ~ 65°C	16.170	16.5	16.830	V
gm4	gm value of error amp		0.8	1	1.2	mS
VoCH4(4)	Output voltage	On EVM, T_A = –10 ~ 65°C	14.700	15.0	15.300	V
ΔVli4(4)	Line regulation	On EVM	–150		150	mV
ΔVlo4(4)	Load regulation	On EVM	–150		150	mV
IOUT4(4)	Minimum Load current	On EVM, [CH-4 input voltage] = 1.8 V	50			mA
VSCP4	SCP detector threshold	Ratio to VCH4	75%	80%	85%	
CH-5						
VCH5	Error amp center voltage	Vout5=00(bin), T_A = –10 ~ 65°C	–7.650	–7.5	–7.350	V
		Vout5=01(bin), T_A = –10 ~ 65°C	–8.160	–8.0	–7.840	V
		Vout5=10(bin), T_A = –10 ~ 65°C	–8..670	–8.5	–8.330	V
		Vout5=11(bin), T_A = –10 ~ 65°C	–9.180	–9.0	–8.820	V
gm5	gm value of error amp		0.8	1.0	1.2	mS
VoCH5(5)	Output voltage	On EVM, T_A = –10 ~ 65°C	–7.650	–7.5	–7.350	V
ΔVli5(5)	Line regulation	On EVM	–75		75	mV
ΔVlo5(5)	Load regulation	On EVM	–75		75	mV
IOUT5(5)	Minimum Load current	On EVM,VCC5 = 4.9 V	50			mA
VSCP5	SCP detector threshold		75%	80%	85%	
CH-6						
VFB6	Error amp center voltage	Vout5 = 00(bin), T_A = –10 ~ 65°C	0.2482	0.264	0.2798	V
		Vout5 = 01(bin), T_A = –10 ~ 65°C	0.4136	0.440	0.4664	V
		Vout5 = 10(bin), T_A = –10 ~ 65°C	0.1654	0.176	0.1866	V
gm6	gm value of error amp		0.8	1	1.2	mS
ICH6(5)	Output voltage	On EVM, T_A = –10 ~ 65°C	11.28	12	12.72	mA
ΔVli6(5)	Line regulation of VFB6	On EVM	–120		120	µA
VOCP	OCP detector threshold	Monitor at FB6	0.80	0.85	0.90	V
VOVP6	OVP detector threshold		21.0	22	23.0	V
VREF6L	CH-6 disable threshold, low side		0.16	0.21	0.26	V
VREF6H	CH-6 disable threshold, high side	VCH1 = 2.8 V	1.7	2	2.3	V
VfDI6	Forward voltage of integrated diode	I(OUT6 = VCH6) = 20 mA			0.9	V

(5) Not production tested. Assured by design. Using reference EVM.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CH-7						
VCH7U	Error amp center voltage	Vout7 = 0000(bin), T_A = –10 ~ 65°C, MODE7 = H	4.802	4.9	4.998	V
		Vout7 = 0001(bin), T_A = –10 ~ 65°C, MODE7 = H	4.753	4.85	4.947	V
		Vout7 = 0010(bin), T_A = –10 ~ 65°C, MODE7 = H	4.704	4.8	4.896	V
		Vout7 = 0001(bin), T_A = –10 ~ 65°C, MODE7 = H	4.655	4.75	4.845	V
		Vout7 = 0100(bin), T_A = –10 ~ 65°C, MODE7 = H	4.606	4.7	4.794	V
		Vout7 = 0101(bin), T_A = –10 ~ 65°C, MODE7 = H	4.557	4.65	4.743	V
		Vout7 = 0110(bin), T_A = –10 ~ 65°C, MODE7 = H	4.508	4.60	4.692	V
		Vout7 = 0111(bin), T_A = –10 ~ 65°C, MODE7 = H	4.459	4.55	4.641	V
		Vout7 = 1000(bin), T_A = –10 ~ 65°C, MODE7 = H	4.41	4.50	4.590	V
		Vout7 = 1001(bin), T_A = –10 ~ 65°C, MODE7 = H	4.361	4.45	4.539	V
		Vout7 = 1010(bin), T_A = –10 ~ 65°C, MODE7 = H	4.312	4.40	4.488	V
		Vout7 = 1011(bin), T_A = –10 ~ 65°C, MODE7 = H	4.998	5.10	5.202	V
		Vout7 = 1100(bin), T_A = –10 ~ 65°C, MODE7 = H	4.949	5.05	5.151	V
		Vout7 = 1101(bin), T_A = –10 ~ 65°C, MODE7 = H	4.9	5	5.1	V
		Vout7 = 1110(bin), T_A = –10 ~ 65°C, MODE7 = H	4.851	4.95	5.049	V
		Vout7 = 1111(bin), T_A = –10 ~ 65°C, MODE7 = L	4.802	4.90	4.998	V
VCH7D	Error amp center voltage	Vout7 = 0000(bin), T_A = –10 ~ 65°C, MODE7 = L	3.038	3.1	3.162	V
		Vout7 = 0001(bin), T_A = –10 ~ 65°C, MODE7 = L	2.989	3.05	3.111	V
		Vout7 = 0010(bin), T_A = –10 ~ 65°C, MODE7 = L	2.940	3.00	3.060	V
		Vout7 = 0001(bin), T_A = –10 ~ 65°C, MODE7 = L	2.891	2.95	3.009	V
		Vout7 = 0100(bin), T_A = –10 ~ 65°C, MODE7 = L	2.842	2.9	2.958	V
		Vout7 = 0101(bin), T_A = –10 ~ 65°C, MODE7 = L	2.793	2.85	2.907	V
		Vout7 = 0110(bin), T_A = –10 ~ 65°C, MODE7 = L	2.744	2.8	2.856	V
		Vout7 = 0111(bin), T_A = –10 ~ 65°C, MODE7 = L	2.695	2.75	2.805	V
		Vout7 = 1000(bin), T_A = –10 ~ 65°C, MODE7 = L	2.646	2.7	2.754	V
		Vout7 = 1001(bin), T_A = –10 ~ 65°C, MODE7 = L	2.597	2.65	2.703	V
		Vout7 = 1010(bin), T_A = –10 ~ 65°C, MODE7 = L	2.548	2.6	2.652	V
		Vout7 = 1011(bin), T_A = –10 ~ 65°C, MODE7 = L	2.499	2.55	2.601	V
		Vout7 = 1100(bin), T_A = –10 ~ 65°C, MODE7 = L	2.450	2.5	2.550	V
		Vout7 = 1101(bin), T_A = –10 ~ 65°C, MODE7 = L	3.138	3.2	3.264	V
		Vout7 = 1110(bin), T_A = –10 ~ 65°C, MODE7 = L	3.087	3.15	3.213	V
		Vout7 = 1111(bin), T_A = –10 ~ 65°C, MODE7 = L	3.038	3.1	3.162	V
gm7	gm value of error amp		0.8	1	1.2	mS
VoC71(6)	Output voltage	Mode7 = H, On EVM, T_A = –10 ~ 65°C	4.802	4.9	4.998	V
ΔVli71(6)	Line regulation	Mode7 = H, On EVM	–49		49	mV
ΔVlo71(6)	Load regulation	Mode7 = H, On EVM	–49		49	mV
IOUT71(6)	Minimum Load current	Mode7 = H, On EVM, VCC7=1.8 V	500			mA
VOCH72(6)	Output voltage	Mode7 = L, On EVM, T_A = –10 ~ 65°C	3.038	3.1	3.162	V
ΔVli72(6)	Line regulation	Mode7 = L, On EVM	–31		31	mV
ΔVlo72(6)	Load regulation	Mode7 = L, On EVM	–31		31	mV
IOUT72(6)	Minimum load current	Mode7 = L, On EVM, [CH-7 input voltage] = 4.9 V	150			mA
VSCP7	SCP detector threshold	Ratio to VCH7	75%	80%	85%	
VOVP7	OVP detector threshold	Ratio to VCH7		5.99		V
IOS71H	Source curent of OS71	VOS71 = 0 V, VCH3 = VCH7 = 4.9 V			–6	mA
IOS71L	Sink current of OS71	VOS71 = 4.9 V, VCH3 = VCH7 = 4.9 V	0.2			μA
IOS72H	Source current of OS72	VOS72 = 4.4 V, VCH3 = VCH7 = 4.9 V			–100	mA
IOS72L	Sink current of OS72	VOS72 = 0.5 V, VCH3 = VCH7 = 4.9 V	100			mA

(6) Not production tested. Assured by design. Using reference EVM.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 4.9 V, VCC7 = 4.9 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IOS73H	Source current of OS73	VOS73 = 0.0 V, VCH3 = VCH7 = 4.9 V			–100	mA
IOS73L	Sink current of OS73	VOS73 = 0.5 V, VCH3 = VCH7 = 4.9 V	100			mA
ROS71n	ON resistance	NMOS (OS71, GND GD), VOS71 = 0.1 V, VCH3 = VCH7 = 4.9 V			7.5	kΩ
ROS72n	ON resistance	NMOS(OS72, GND GD), VOS72 = 0.1 V, VCH3 = VCH7 = 4.9 V			5	Ω
ROS73n	ON resistance	NMOS(OS73, GND GD), VOS73 = 0.1 V, VCH3 = VCH7 = 4.9 V			5	Ω
ROS71p	ON resistance	PMOS(VCH7, OS71), VOS71 = 4.8 V, VCH3 = VCH7 = 4.9 V			360	Ω
ROS72p	ON resistance	PMOS(VCC7, OS72), VOS72 = 4.8 V, VCH3 = VCH7 = 4.9 V			5	Ω
ROS73p	ON resistance	PMOS(VCC GD, OS73), VOS73 = 4.8 V, VCH3 = VCH7 = 4.9 V			15	Ω
CH-8						
VCH81	Error amp center voltage (normal)	PWR_ON = H, T_A = –10 ~ 65°C	3.528	3.6	3.672	V
VCH82	Error detector center voltage (skip)		3.492	3.6	3.708	V
gm8	gm value of error amp		0.8	1	1.2	mS
VoCH81(7)	Output voltage (skip)	On EVM, T_A = –10 ~ 65°C, VCC8 = 1.5 ~ 3.6 V	3.492	3.6	3.708	V
VoCH82(7)	Output voltage (normal)		3.528	3.6	3.672	V
ΔVli81(7)	Line regulation (skip)	On EVM, VCC8 = 1.8 ~ 3.6 V (= VoCH81)(8)	–108		180	mV
ΔVli82(7)	Line regulation (normal)	On EVM, VCC8 = 1.8 ~ 3.6 V	–36		36	mV
ΔVlo81(7)	Load regulation (skip)	On EVM, VCC8 = 1.8 ~ 3.6 V, ICH8 < x[mA]	–120		120	mV
ΔVlo82(7)	Load regulation (normal)	On EVM, VCC8 = 1.8 ~ 3.6 V	–36		36	mV
IOUT81(7)	Minimum Load current (skip)	On EVM, VCC8 = 1.8 V	120			mA
IOUT82(7)	Minimum Load current (normal)	On EVM, VCC8 = 1.8 V	170			mA

(7) Not production tested. Assured by design. Using reference EVM.
(8) This parameter ΔVli81 is covered by VoCH81 and adjusted to VoCH81.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO-1						
VLDO1	Output voltage	VCH8 = 3.6 ~ 5.25 V, ILDO1 = 5 mA	2.842	2.9	2.958	V
ΔVliL1	Line regulation	VCH8 = 3.6 ~ 5.25 V, ILDO1 = 5 mA			30	mV
ΔVloL1	Load regulation	VCH8 = 3.6 V, ILOD1 = 0.1 ~ 30 mA			100	mV
	Output current limit	VCH8 = 3.6 ~ 5.25 V	36			mA
LDO-2						
VLDO2	Output voltage	VCH8 = 3.6 ~ 5.25 V, ILDO2 =6 mA	2.842	2.9	2.958	V
ΔVliL2	Line regulation	VCH8 = 3.6 ~ 5.25 V, ILDO2 = 6 mA			30	mV
ΔVloL2	Load regulation	VCH8 = 3.6 V, ILOD2 = 0.1 ~ 50 mA			100	mV
	Output current limit	VCH8 = 3.6 ~ 5.25 V	60			mA
LDO-3						
VLDO3	Output voltage	VCH8 = 3.6 ~ 5.25 V, ILDO3 = 10 mA	3.038	3.1	3.162	V
ΔVliL3	Line regulation	VCH8 = 3.6 ~ 5.25 V, ILDO3 = 10 mA			30	mV
ΔVloL3	Load regulation	VCH8 = 3.6 V, ILOD3 = 0.1 ~ 20 mA			100	mV
	Output current limit	VCH8 = 3.6 ~ 5.25 V	24			mA
LDO-4						
VLDO4	Output voltage	VCH8 = 3.6 ~ 5.25 V, ILDO4 = 5 mA	3.078	3.142	3.202	V
ΔVliL4	Line regulation	VCH8 = 3.6 ~ 5.25 V, ILDO4 = 5 mA			30	mV
ΔVloL4	Load regulation	VCH8 = 3.6 V, ILOD1 = 0.5 ~ 100 mA			100	mV
	Output current limit	VCH8 = 3.6 ~ 5.25 V	120			mA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO-5						
VLDO5	Output voltage	LDO5Vo = 00 (bin), T_A = –10 ~ 65°C, ILDO5 = 15 mA	13.23	13.5	13.778	V
		LDO5Vo = 01 (bin), T_A = –10 ~ 65°C, ILDO5 = 15 mA	12.25	12.5	12.75	
		LDO5Vo = 10 (bin), T_A = –10 ~ 65°C, ILDO5 = 15 mA	11.76	12	12.24	
		LDO5Vo = 11 (bin), T_A = –10 ~ 65°C, ILDO5 = 15 mA	8.33	8.5	8.67	
ΔVliL5	Line regulation	VCH4 = 15 ~ 16.5 V, ILDO5 = 5 mA			50	mV
ΔVloL5	Load regulation	VCH4 = 15 V, ILOD5 = 0.1 ~ 15 mA			50	mV
	Output current limit	VCH4 = 15 ~ 16.5 V	36			mA

EQUIVALENT INPUT/OUTPUT CIRCUIT DIAGRAMS

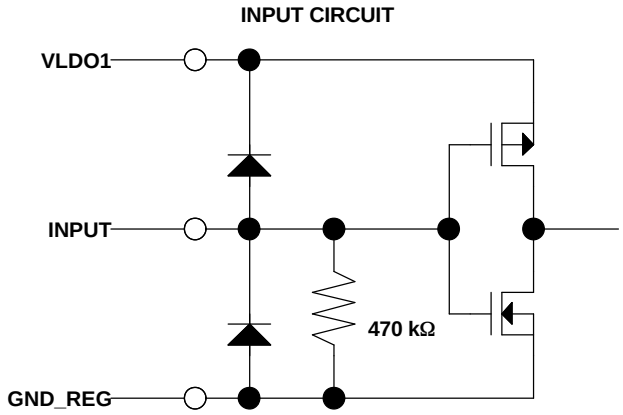


Figure 1. PWR_ON, LDO4_ON, DIN, TEST

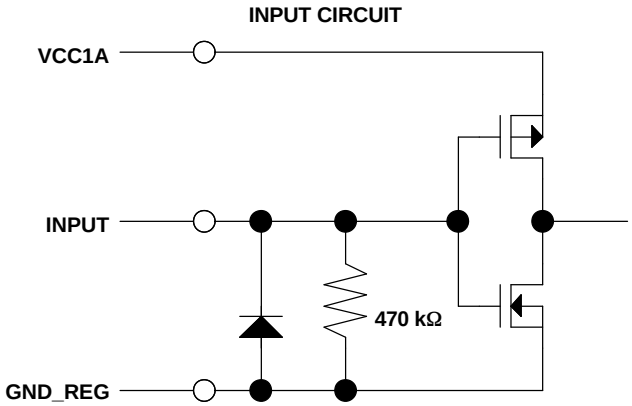


Figure 2. TLD

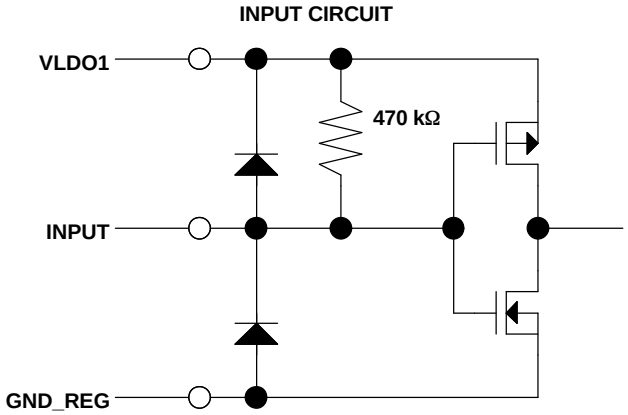


Figure 3. LD

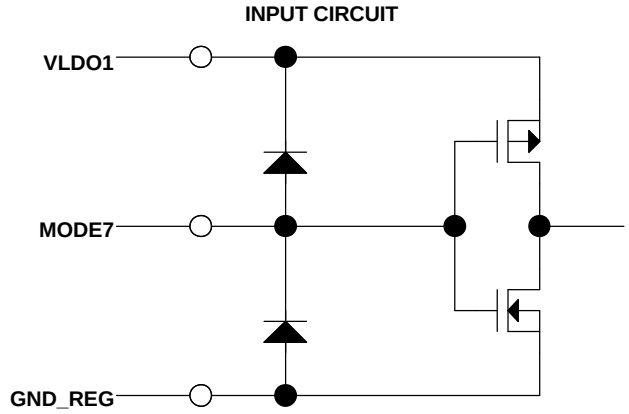


Figure 4. MODE7

EQUIVALENT INPUT/OUTPUT CIRCUIT DIAGRAMS (continued)

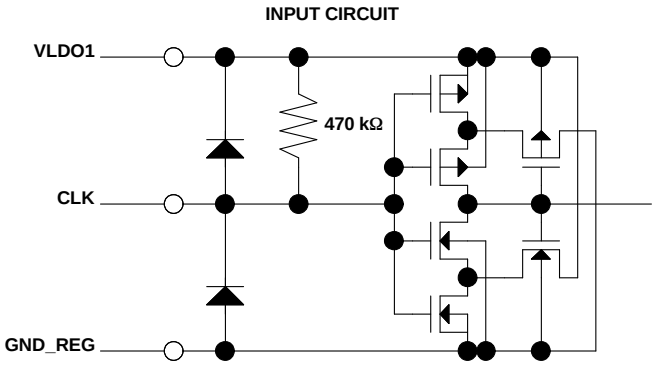


Figure 5. CLK

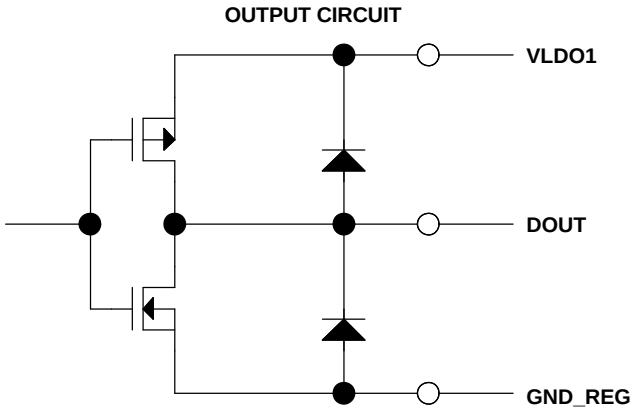


Figure 6. DOUT

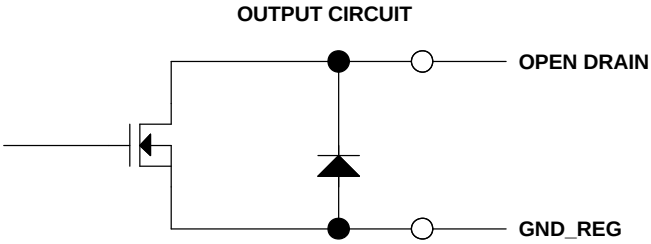


Figure 7. READY, XRESET

ICC1

ICC1 represents the supply current measured when all channels are operating normally with no load. It is difficult to connect coils and other external devices to the TPS65520 . Therefore, in order to measure its characteristics in shipping tests, the desired ICC1 is specified using two testable parameters with the pins handled as shown in Table 1.

ICC_CTRL represents the supply current from the 2.9-V and 4.2-V power supplies shown in the tables. ICC_GD represents the supply current from the 4.2-V power supplies shown in the tables. IVCC_GD is a self-consumed gate drive current from CH-3. Therefore, it is associated with the desired ICC1 through the CH-3 efficiency. The following formula indicates the relationship between IVCC_GD and the supply current from the power supplies in the application circuit (ICC1). ICC1 is specified as the supply current when a voltage of 4.2 V is the input. ICC_CTRL is the current consumed by the TPS65520 (excluding IVCC_GD).

$$ICC1 = \frac{4.9}{4.2} \times \frac{1}{\eta_{CH-3}} \times IVCC\_GD + ICC\_CTRL$$

$$\frac{4.9 \times IVCC\_GD}{4.2 \times (ICC1 - ICC\_CTRL)} = \eta_{CH-3} \quad (1)$$

Table 1. Pin Handling for Measuring ICC1

Pin Name	Connection	Note
POWER SUPPLY		
VCC_GD	4.9 V	Supply gate drive
GND_GD	GND	
GNDANA	GND	
GNDLOG	GND	
GNDREG	GND	
GNDLDOA	GND	
SUB-CPU CONTROL		
PWR_ON	2.9 V	
CSCP	GND	avoid shutdown
ROSC	150 kΩ to GND	recommended part
CREF	Cap	recommended part
CBG	Cap	recommended part
VLDO1	Cap	recommended part
VLDO2	Cap	recommended part
VLDO3	Cap	recommended part
VLDO4	Cap	recommended part
VLDO5	Cap	recommended part
LOGIC		
ROMWR	GND	
TEST	open	pull down internally
TLD	open	pull down internally
CLK	open	pull up internally
DIN	open	pull down internally
LD	open	pull up internally
DOUT	open	(not concerned)
SS, ETC.		
READY	open	(not concerned)
XRESET	open	(not concerned)
LDO4_ON	2.9 V	force LDO-4 ON
SS_SYNC	open	(not concerned)
SS2	open	(not concerned)
SS3	open	(not concerned)
SS5	open	(not concerned)
SS6	open	(not concerned)
SSLDO5	open	(not concerned)
CH-1		
BOOT11	4.9 V	supply gate driver
BOOT12	4.9 V	supply gate driver
VCH1A/B/C	2.9 V	force output
VCC1A/B/C	2.9 V	supply CH-1
GND1A/B/C	GND	
OUT11A/B/C	open	(not concerned)
OUT12A/B/C	open	(not concerned)
ERR1	4.2 V	force MAX DUTY
CH-2		
BOOT2	4.9 V	supply gate driver
VCH2	GND	force MAX DUTY
VCC2	2.9 V	bias power MOS
OUT2	open	(not concerned)
GND2	GND	
ERR2	4.2 V	force MAX DUTY
CH-3		
VCH3A/B/C	4.9 V	supply TAKUMI
VCH3S	open	(not concerned)
OUT3A/B/C	open	(not concerned)
GND3A/B/C	GND	
ERR3	4.2 V	force MAX DUTY
CH-4		
VCH4	4.9 V	force MAX DUTY
OUT4	open	(not concerned)
GND4	GND	
ERR4	open	(not concerned)
CH-5		
VCH5	GND	force MAX DUTY
VCC5	4.9 V	supply gate driver
OUT5	open	(not concerned)
ERR5	open	(not concerned)
CH-6		
OUT6	open	(not concerned)
FB6	GND	force MAX DUTY
VCH6	open	(not concerned)
ICH6	open	(not concerned)
GND6	GND	
REF6	CBG	bias
ERR6	open	(not concerned)
CH-7		
VCH7	open	(not concerned)
VCC7	4.9 V	supply gate driver
ERR7	4.2 V	force MAX DUTY
MODE7	GND	fix logic value
VOS71	open	(not concerned)
VOS72	open	(not concerned)
VOS73	open	(not concerned)
CH-8		
VCH8A/B	4.2 V	force through mode
VCC8	4.2 V	force through mode
ERR8	4.2 V	force MAX DUTY
OUT8A/B	open	(not concerned)
GND8A/B	GND	

ICC2

ICC2 represents the supply current measured when the system operation is minimized with CH-8 placed in Sleep mode. It is difficult to connect coils and other external devices to the TPS65520 to measure its characteristics in shipping tests. Therefore, the desired ICC2 is specified using three testable parameters with the pins handled as shown in the following tables.

IVCC8 and IVCH8 represent the supply currents from the VCC8 and VCH8 pins, respectively.

The following formula indicates the relationship between those currents and the supply current from the power supplies in the application circuit (ICC2). ICC2 is specified as the supply current when a voltage of 3.6 V is input.

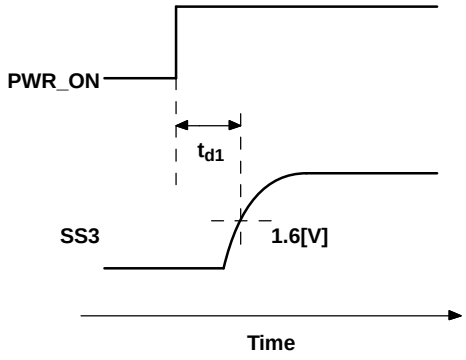
$$ICC2 = \frac{1}{\eta_{CH-8:skip}} \times IVCH8 + IVCC8 \quad (2)$$

Table 2. Pin Handling for Measuring ICC2

Pin Name	Connection	Note
POWER SUPPLY		
VCC_GD	open	(not concerned)
GND_GD	GND	
GNDANA	GND	
GNDLOG	GND	
GNDREG	GND	
GNDLDOA	GND	
LOGIC		
ROMWR	GND	
TEST	open	pull down internally
TLD	open	pull down internally
CLK	open	pull up internally
DIN	open	pull down internally
LD	open	pull up internally
DOUT	open	(not concerned)
SUB-CPU CONTROL		
PWR_ON	GND	
CSCP	GND	avoid shutdown
ROSC	150 kΩ to GND	recommended part
CREF	Cap	recommended part
CBG	Cap	recommended part
VLDO1	Cap	recommended part
VLDO2	Cap	recommended part
VLDO3	Cap	recommended part
VLDO4	Cap	recommended part
VLDO5	Cap	recommended part
SS, ETC.		
READY	open	(not concerned)
XRESET	open	(not concerned)
LDO4_ON	GND	
SS_SYNC	open	(not concerned)
SS2	open	(not concerned)
SS3	open	(not concerned)
SS5	open	(not concerned)
SS6	open	(not concerned)
SSLDO5	open	(not concerned)
CH-1		
BOOT11	open	(not concerned)
BOOT12	open	(not concerned)
VCH1A/B/C	open	(not concerned)
VCC1A/B/C	open	(not concerned)
GND1A/B/C	GND	
OUT11A/B/C	open	(not concerned)
OUT12A/B/C	open	(not concerned)
ERR1	open	(not concerned)
CH-2		
BOOT2	open	(not concerned)
VCH2	open	(not concerned)
VCC2	open	(not concerned)
OUT2	open	(not concerned)
GND2	GND	
ERR2	open	(not concerned)
CH-3		
VCH3A/B/C	open	(not concerned)
VCH3S	open	(not concerned)
OUT3A/B/C	open	(not concerned)
GND3A/B/C	GND	
ERR3	open	(not concerned)
CH-4		
VCH4	open	(not concerned)
OUT4	open	(not concerned)
GND4	GND	
ERR4	open	(not concerned)
CH-5		
VCH5	open	(not concerned)
VCC5	open	(not concerned)
OUT5	open	(not concerned)
ERR5	open	(not concerned)
CH-6		
OUT6	open	(not concerned)

Pin Name	Connection	Note
FB6	GND	
VCH6	open	(not concerned)
ICH6	open	(not concerned)
GND6	GND	
REF6	open	(not concerned)
ERR6	open	(not concerned)
CH-7		
VCH7	open	(not concerned)
VCC7	open	(not concerned)
ERR7	open	(not concerned)

Pin Name	Connection	Note
MODE7	GND	fix logic value
VOS71	open	(not concerned)
VOS72	open	(not concerned)
VOS73	open	(not concerned)
CH-8		
VCH8A/B	3.7 V	stop skip switching
VCC8	3.6 V	supply to CH-8 circuit
ERR8	open	(not concerned)
OUT8A/B	open	(not concerned)
GND8A/B	GND	



A. t_{d1} (Measure SS3 when it is left open.)

Figure 8. t_{d1} Measurement Reference

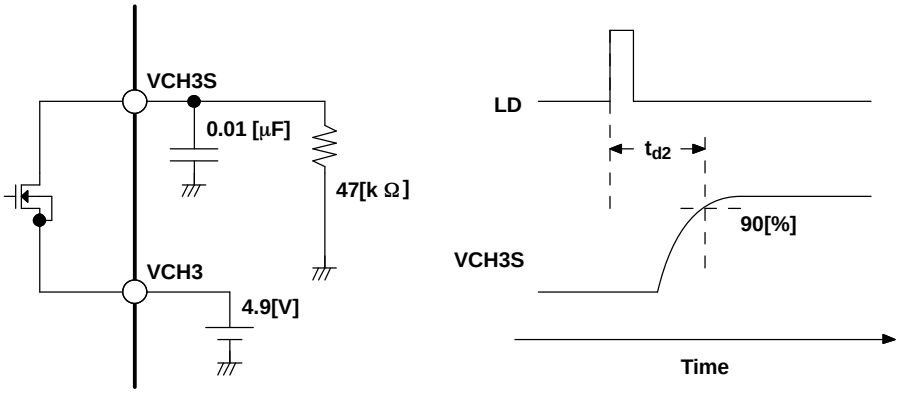
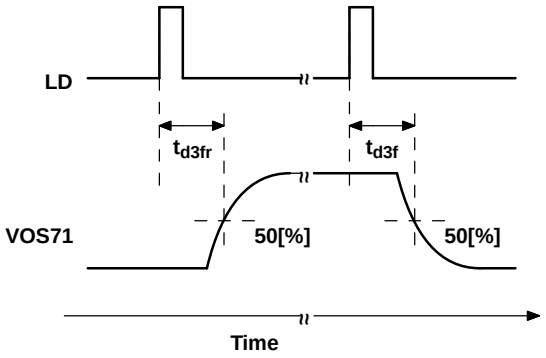
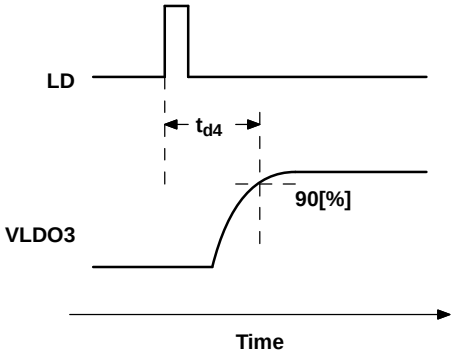


Figure 9. t_{d2} Measuring Circuit and Measurement Reference



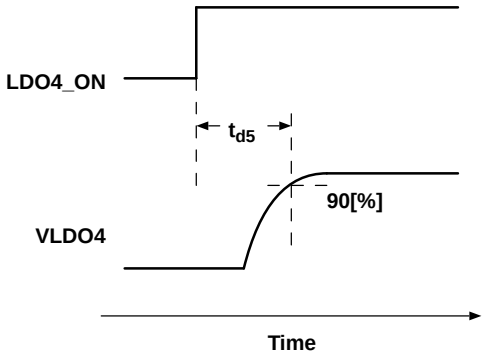
A. t_{d3r}, t_{d3f} (Measure VOS71 when it is left open.)

Figure 10. t_{d3r} and t_{d3f} Measurement References



A. t_{d4} (Connect a capacitor, 4.7 µF recommended, to VLDO3.)

Figure 11. t_{d4} Measurement Reference



A. t_{d5} (Connect a capacitor, 4.7 µF recommended, to VLDO4.)

Figure 12. t_{d5} Measurement Reference

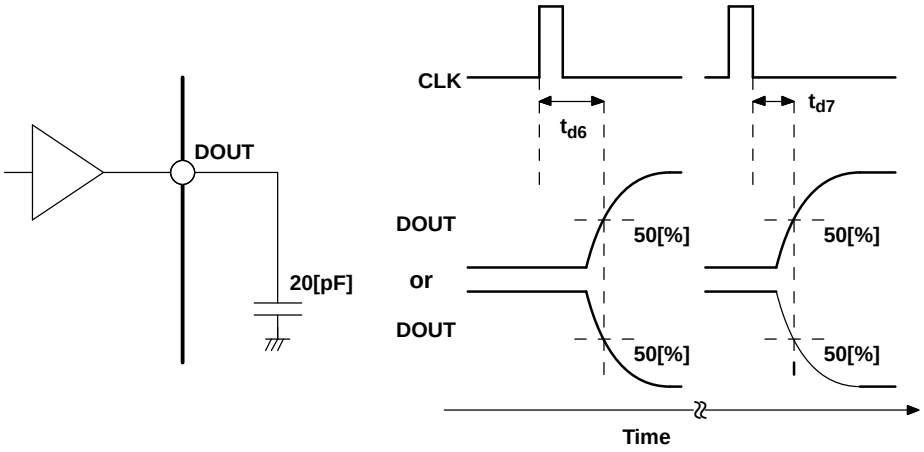


Figure 13. t_{d6} and t_{d7} Measuring Circuit and Measurement References

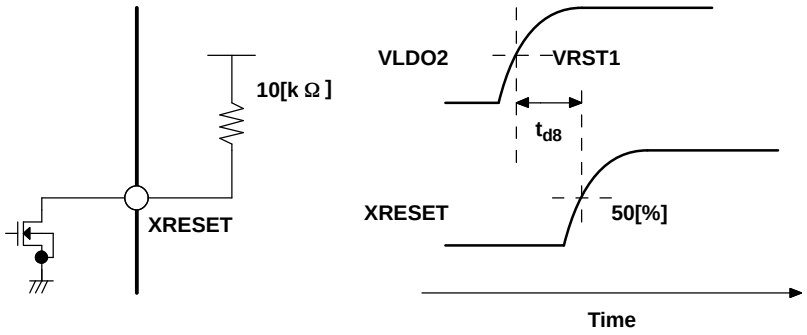


Figure 14. t_{d8} Measuring Circuit and Measurement Reference

TIMING REQUIREMENTS

T_A = 25°C, VCC1 = 3.6 V, VCC2 = 3.6 V, VCC5 = 3.6 V, VCC7 = 3.6 V, VCC8 = 3.6 V, VCH8 = 3.6 V, VCH3 = 4.9 V, VCH_GD = 4.9 V, LDO4_ON = L, and all register bits are default value (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{s1}	Setup time, LD ↓ before CLK ↑ (see Figure 33)	400		ns
t_{s2}	Setup time, DIN valid before CLK ↑ (see Figure 33)	200		ns
t_{s3}	Setup time, TLD ↑ after CLK ↑ (see Figure 39)	50		ns
t_{s4}	Setup time, TLD ↑ before CLK ↑ (see Figure 39)	50		ns
t_{s5}	Setup time, ROMWR ↑ before TLD↑ (see Figure 43)	10		µs
t_{h1}	Hold time, DIN valid after CLK ↑ (see Figure 33)	50		ns
t_{h2}	Hold time, LD ↑ after last CLK ↑ (see Figure 33)	50		ns
t_{h3}	Hold time, ROMWR ↓ after last TLD ↓ (see Figure 33)	10		µs
t_{w1}	Pulse width of TLD = H for Test0 ~ Test5 (see Figure 39)	50		ns
t_{w2}	Pulse width of TLD = H for Test6,Test7 (see Figure 43)	20		ms
t_{w3}	Pulse width of CLK = H (see Figure 33)	100		ns
t_{cyc}	Period of CLK ↑ (see Figure 33)	500		ns

SWITCHING CHARACTERISTICS

	PARAMETER	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, PWR_ON ↑ to start of charging SS3 (see Figure 8 and Figure 30)		1.1	1.15	ms
t_{d2}	Delay time, LD ↑ to VCH3S ↑ (see Figure 9 and Figure 30)		500	750	µs
t_{d3r}	Delay time, LD ↑ to VOS71↑ , VCH7 = 4.9 V (see Figure 10 and Figure 30)		500	1000	ns
t_{d3f}	Delay time, LD ↑ to VOS71↓ , VCH7 = 4.9 V (see Figure 10 and Figure 30)		60	100	µs
t_{d4}	Delay time, LD ↑ to VLDO3 ↑ (see Figure 11 and Figure 30)		300	650	µs
t_{d5}	Delay time, LDO4_ON ↑ to VLDO4 ↑ (see Figure 12 and Figure 30)		300	650	µs
t_{d6}	Delay time, last CLK ↑ to DOUT valid for Normal Mode (see Figure 13, Figure 33, and Figure 39)		100	200	ns
t_{d7}	Delay time, CLK ↓ to DOUT valid for Test0, Test2, Test3, Test5 (see Figure 13, Figure 33, and Figure 39)		100	200	ns
t_{d8}	Delay time, VLDO2 exceeds VRST1 to XRESET ↑ (see Figure 14)	200	300	600	µs

PIN LAYOUT
(TOP VIEW)

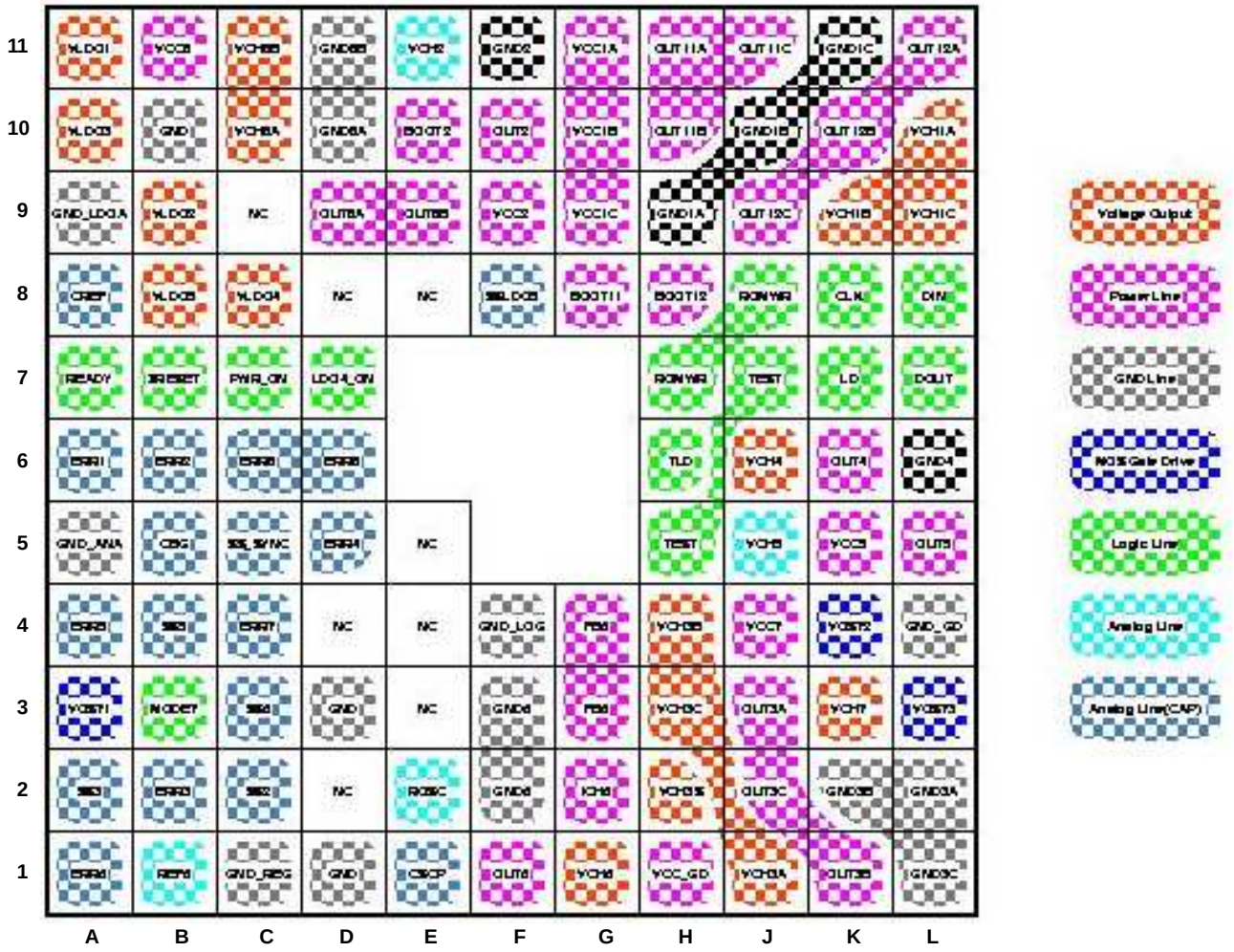


Figure 15. Pin Layout

TERMINAL FUNCTIONS

TERMINAL		NAME	I/O	DESCRIPTION
NO.	PIN ADDRESS			
1	1-A	ERR6	O	Output of gm amp for CH-6
2	1-B	REF6	IO	Reference resistor of CH-6
3	1-C	GND_REG	G	Ground for Analog circuit of Regulators
4	1-D	NC		No connection (recommended to be GND)
5	1-E	CSCP	IO	Current Source of Short Circuit Protection
6	1-F	OUT6	IO	Output Side Terminal of coil L6 for CH-6
7	1-G	VCH6	O	Output voltage of CH-6
8	1-H	VCC_GD	V	Power Supply for Gate Driver of Internal Power MOS-FET
9	1-J	VCH3A	O	Output of CH-3 (1/3)
10	1-K	OUT3B	IO	Output Side Terminal of coil L3 for CH-3 (2/3)
11	1-L	GND3C	G	Ground for CH-3 (3/3)
12	2-A	SS3	O	Current Source of Soft Start for CH-3
13	2-B	ERR3	O	Output of gm amp for CH-3
14	2-C	SS2	I	Current Source of Soft Start for CH-2
15	2-D	NC		No connection (recommended to be GND)
16	2-E	ROSC	O	Reference resistor for PWM Oscillator
17	2-F(= 3-F)	GND6	G	Ground for CH-6(same pin as No.28, 3-F)
18	2-G	ICH6	IO	LEDs cathod of CH-6
19	2-H	VCH3S	O	Analog Switched Output of CH-3
20	2-J	OUT3C	IO	Output Side Terminal of coil L3 for CH-3 (3/3)
21	2-K	GND3B	G	Ground for CH-3 (2/3)
22	2-L	GND3A	G	Ground for CH-3 (1/3)n
23	3-A	VOS71	O	Gate Drive of External PMOS Switch for CH-7
24	3-B	MODE7	I	Mode Selection of CH-7
25	3-C	SS6	O	Current Source of Soft Start for CH-6
26	3-D	NC		No connection (recommended to be GND)
27	3-E	NC		No connection (recommended to be GND)
28	3-F(= 2-F)	GND6	G	Ground for CH-6 (same pin as No.17, 2-F)
29	3-G(= 4-G)	FB6	IO	Current Sense input of CH-6 (same pin as No.40, 4-G)
30	3-H	VCH3C	O	Output of CH-3 (3/3)
31	3-J	OUT3A	IO	Output Side Terminal of coil L3 for CH-3 (1/3)
32	3-K	VCH7	O	Output of CH-7
33	3-L	VOS73	O	Gate Drive of Low Side NMOS Switch for CH-7
34	4-A	ERR5	O	Output of gm amp for CH-5
35	4-B	SS5	O	Current Source of Soft Start for CH-5
36	4-C	ERR7	O	Output of gm amp for CH-7
37	4-D	NC		No connection (recommended to be GND)
38	4-E	NC		No connection (recommended to be GND)
39	4-F	GND_LOG	G	Ground for General Logic circuit
40	4-G(= 3-G)	FB6	IO	Current Sense input of CH-6(same pin as No.29, 3-G)
41	4-H	VCH3B	O	Output of CH-3 (2/3)
42	4-J	VCC7	V	Power Supply of CH-7
43	4-K	VOS72	O	Gate Drive of High Side PMOS Switch for CH-7
44	4-L	GND_GD	G	Ground for Gate Driver of Internal Power MOS-FET
45	5-A	GND_ANA	G	Ground for General Analog circuit

TERMINAL FUNCTIONS (continued)

TERMINAL		NAME	I/O	DESCRIPTION
NO.	PIN ADDRESS			
46	5-B	CBG	IO	Output of BG Reference Voltage Buffer
47	5-C	SS_SYNC	O	Current Source of Soft Start for CH-1, CH-4 and CH-7
48	5-D	ERR4	O	Output of gm amp for CH-4
49	5-E	NC		No connection (recommended to be GND)
50	5-H(= 7-J)	TEST	I	Test Mode selection Input of Serial I/F (same pin as No.67, 7-J)
51	5-J	VCH5	O	Output of CH-5
52	5-K	VCC5	V	Power Supply of CH-5
53	5-L	OUT5	IO	Primary Side Terminal of coil L5 for CH-5
54	6-A	ERR1	O	Output of gm amp for CH-1
55	6-B	ERR2	O	Output of gm amp for CH-2
56	6-C(= 6-D)	ERR8	O	Output of gm amp for CH-8(same pin as No.57, 6-D)
57	6-D(= 6-C)	ERR8	O	Output of gm amp for CH-8(same pin as No.56, 6-C)
58	6-H	TLD	I	Test Mode Latch Input of Serial I/F
59	6-J	VCH4	O	Output of CH-4
60	6-K	OUT4	IO	Output Side Terminal of coil L4 for CH-4
61	6-L	GND4	G	Ground for CH-4
62	7-A	READY	O	READY output for Sub-CPU
63	7-B	XRESET	O	Low Active RESET output for Sub-CPU
64	7-C	PWR_ON	I	TPS65520 device enable input
65	7-D	LDO4_ON	I	Enable of LDO-4
66	7-H(= 8-J)	ROMWR	I	Voltage Bias to write EEPROM (same pin as No.78, 8-J)
67	7-J(= 5-H)	TEST	I	Test Mode selection Input of Serial I/F (same pin as No.50, 5-H)
68	7-K	LD	I	Latch Input of Serial I/F
69	7-L	DOUT	O	Data Output of Serial I/F
70	8-A	CREF	IO	Capacitor of RC filter for Band-Gap Reference
71	8-B	VLDO5	O	Output of LDO-5
72	8-C	VLDO4	O	Output of LDO-4
73	8-D	NC		No connection (recommended to be GND)
74	8-E	NC		No connection (recommended to be GND)
75	8-F	SSLDO5	O	Current Source of Soft Start for LDO-5
76	8-G	BOOT11	IO	Bootstrap for Primary Side of CH-1
77	8-H	BOOT12	IO	Bootstrap for Output Side of CH-1
78	8-J(= 7-H)	ROMWR	I	Voltage Bias to write EEPROM (same pin as No.66, 7-H)
79	8-K	CLK	I	Clock Input of Serial I/F
80	8-L	DIN	I	Data Input of Serial I/F
81	9-A	GND_LDOA	G	Ground for Analog circuit of LDO-1,LDO-2,LDO-3
82	9-B	VLDO2	O	Output of LDO-2
83	9-C	NC		No connection (recommended to be GND)
84	9-D	OUT8A	IO	Output Side Terminal of coil L8 for CH-8 (1/2)
85	9-E	OUT8B	IO	Output Side Terminal of coil L8 for CH-8 (2/2)
86	9-F	VCC2	V	Power Supply of CH-2
87	9-G	VCC1C	V	Power Supply of CH-1 (3/3)
88	9-H	GND1A	G	Ground for CH-1 (1/3)
89	9-J	OUT12C	IO	Output Side Terminal of coil L1 for CH-1 (3/3)
90	9-K	VCH1B	O	Output of CH-1 (2/3)

TERMINAL FUNCTIONS (continued)

TERMINAL		NAME	I/O	DESCRIPTION
NO.	PIN ADDRESS			
91	9-L	VCH1C	O	Output of CH-1 (3/3)
92	10-A	VLDO3	O	Output of LDO-3
93	10-B	NC		No connection (recommended to be GND)
94	10-C	VCH8A	O	Output of CH-8 (1/2)
95	10-D	GND8A	G	Ground for CH-8 (1/2)
96	10-E	BOOT2	IO	Bootstrap for CH-2
97	10-F	OUT2	IO	Primary Side Terminal of coil L2 for CH-2
98	10-G	VCC1B	V	Power Supply of CH-1 (2/3)
99	10-H	OUT11B	IO	Primary Side Terminal of coil L1 for CH-1 (2/3)
100	10-J	GND1B	G	Ground for CH-1 (2/3)
101	10-K	OUT12B	IO	Output Side Terminal of coil L1 for CH-1 (2/3)
102	10-L	VCH1A	O	Output of CH-1 (1/3)
103	11-A	VLDO1	O	Output of LDO-1
104	11-B	VCC8	V	Power Supply of CH-8
105	11-C	VCH8B	O	Output of CH-8 (2/2)
106	11-D	GND8B	G	Ground for CH-8 (2/2)
107	11-E	VCH2	O	Output of CH-2
108	11-F	GND2	G	Ground for CH-2
109	11-G	VCC1A	V	Power Supply of CH-1 (1/3)
110	11-H	OUT11A	IO	Primary Side Terminal of coil L1 for CH-1 (1/3)
111	11-J	OUT11C	IO	Primary Side Terminal of coil L1 for CH-1 (3/3)
112	11-K	GND1C	G	Ground for CH-1 (3/3)
113	11-L	OUT12A	IO	Output Side Terminal of coil L1 for CH-1 (1/3)

REGISTER MAP

Some switching regulators allow the output voltage to be changed according to control register settings. Changing the voltage setting while a regulator is operating may, however, cause the output to overshoot and exceed the rating. Be careful when dynamically changing the regulator output voltage.

LIST OF REGISTERS

NAME	POSITION	DESCRIPTION
parity	D[47] - D[40]	parity data
CH7-SW	D[38]	VOS71, Load side switch of CH-7
Dmax7	D[37] - D[36]	duty setting of CH-7
Dmax5	D[35] - D[34]	duty setting of CH-5
Dmax4	D[33] - D[32]	duty setting of CH-4
CH3-SW	D[31] - D[30]	Load side switch of CH-3
Dmax3	D[29] - D[28]	duty setting of CH-3, CH-1(UP,CROSS) and CH-8
Vout7	D[27] - D[24]	Voltage setting of CH-7
Vout5	D[23] - D[22]	Voltage setting of CH-5
Vout4	D[21] - D[20]	Voltage setting of CH-4
Vout3	D[19] - D[16]	Voltage setting of CH-3
Vout2	D[15] - D[12]	Voltage setting of CH-2
Vout1	D[11] - D[08]	Voltage setting of CH-1
LDO5Vo	D[07] - D[06]	Voltage setting of LDO-5
LDOSW5	D[05]	LDO-5 ON/OFF switch
LDOSW3	D[04]	LDO-3 ON/OFF switch
Dmax6	D[03] - D[02]	duty setting of CH-6
Vout6B	D[01] - D[00]	Back-Light LED current of CH-6

CH7-SW

D[39]	D[38]	D[37]	D[36]	ON/OFF	
*	0	*	*	OFF	default
*	1	*	*	ON	

Dmax7

D[39]	D[38]	D[37]	D[36]	DUTY [%]			
				MIN	TYP	MAX	
*	*	0	0	82	86	91	default
*	*	0	1	77	81	86	
*	*	1	0	72	76	81	
*	*	1	1	67	71	76	

Dmax5

D[35]	D[34]	D[33]	D[32]	DUTY [%]			
				MIN	TYP	MAX	
0	0	*	*	84	88	92	default
0	1	*	*	79	83	87	
1	0	*	*	74	78	82	
1	1	*	*	69	73	77	

Dmax4

D[35]	D[34]	D[33]	D[32]	DUTY [%]			
				MIN	TYP	MAX	
*	*	0	0	92	94	96	default
*	*	0	1	90	92	94	
*	*	1	0	88	90	92	
*	*	1	1	86	88	90	

CH3-SW

D[31]	D[30]	D[29]	D[28]	ON/OFF	
0	0	*	*	OFF	default
0	1	*	*	OFF	
1	0	*	*	OFF	
1	1	*	*	ON	

Dmax3

D[31]	D[30]	D[29]	D[28]	DUTY [%]			
				MIN	TYP	MAX	
*	*	0	0	82	86	91	default
*	*	0	1	77	81	86	
*	*	1	0	72	76	81	recommend
*	*	1	1	67	71	76	

Vout7

D[27]	D[26]	D[25]	D[24]	Output Voltage [V]		
				DOWN	UP	
0	0	0	0	3.10	4.90	default
0	0	0	1	3.05	4.85	
0	0	1	0	3.00	4.80	
0	0	1	1	2.95	4.75	
0	1	0	0	2.90	4.70	
	1	0	1	2.85	4.65	
0	1	1	0	2.80	4.60	
0	1	1	1	2.75	4.55	
1	0	0	0	2.70	4.50	
1	0	0	1	2.65	4.45	
1	0	1	0	2.60	4.40	
1	0	1	1	2.55	5.10	
1	1	0	0	2.50	5.05	
1	1	0	1	3.20	5.00	
1	1	1	0	3.15	4.95	
1	1	1	1	3.10	4.90	

Vout5

D[23]	D[22]	D[21]	D[20]	Output Voltage [V]	
0	0	*	*	-7.5	default
0	1	*	*	-8.0	

Vout5 (continued)

D[23]	D[22]	D[21]	D[20]	Output Voltage [V]	
1	0	*	*	-8.5	
1	1	*	*	-9.0	

Vout4

D[19]	D[18]	D[17]	D[16]	Output Voltage [V]	
*	*	0	0	15.0	default
*	*	0	1	15.5	
*	*	1	0	16.0	
*	*	1	1	16.5	

Vout3

D[19]	D[18]	D[17]	D[16]	Output Voltage [V]	
0	0	0	0	4.90	default
0	0	0	1	4.85	
0	0	1	0	4.80	
0	0	1	1	4.75	
0	1	0	0	4.70	
0	1	0	1	4.65	
0	1	1	0	4.60	
0	1	1	1	4.55	
1	0	0	0	4.50	
1	0	0	1	5.20	
1	0	1	0	5.15	
1	0	1	1	5.10	
1	1	0	0	5.05	
1	1	0	1	5.00	
1	1	1	0	4.95	
1	1	1	1	4.90	

Vout2

D[15]	D[14]	D[13]	D[12]	Output Voltage [V]	
0	0	0	0	1.20	default
0	0	0	1	1.15	
0	0	1	0	1.10	
0	0	1	1	1.80	
0	1	0	0	1.75	
0	1	0	1	1.70	
0	1	1	0	1.65	
0	1	1	1	1.60	
1	0	0	0	1.55	
1	0	0	1	1.50	
1	0	1	0	1.45	
1	0	1	1	1.40	
1	1	0	0	1.35	
1	1	0	1	1.30	
1	1	1	0	1.25	
1	1	1	1	1.225	

Vout1

D[11]	D[10]	D[09]	D[08]	Output Voltage [V]	
0	0	0	0	2.80	default
0	0	0	1	2.75	
0	0	1	0	2.70	
0	0	1	1	2.65	
0	1	0	0	2.60	not recommended
0	1	0	1	2.55	not recommended
0	1	1	0	2.50	not recommended
0	1	1	1	3.20	
1	0	0	0	3.15	
1	0	0	1	3.10	
1	0	1	0 3.05	3.05	
1	0	1	1	3.00	
1	1	0	0	2.95	
1	1	0	1	2.90	
1	1	1	0	2.85	
1	1	1	1	2.825	

LDO5Vo

D[07]	D[06]	D[05]	D[04]	Output Voltage [V]	
0	0	*	*	13.5	default
0	1	*	*	12.5	
1	0	*	*	12.0	
1	1	*	*	8.5	

LDOSW5

D[07]	D[06]	D[05]	D[04]	ON / OFF	
*	*	0	*	OFF	default
*	*	1	*	ON	

LDOSW3

D[07]	D[06]	D[05]	D[04]	ON / OFF	
*	*	*	0	ON	default
*	*	*	1	OFF	

Dmax6

D[03]	D[02]	D[01]	D[00]	DUTY [%]			
				MIN	TYP	MAX	
0	0	*	*	87	89	91	default
0	1	*	*	89	91	93	
1	0	*	*	91	93	95	
1	1	*	*	93	95	97	

Vout6B

D[03]	D[02]	D[01]	D[00]	Output Current [mA]	
*	*	0	0	12.0	default
*	*	0	1	20.0	
*	*	1	0	8.0	
*	*	1	1	OFF	

EEPROM MAP

Note: TI is shipping ICs with recommended values.

DEFAULT VALUE SETUP BITS

NAME	POSITION	DESCRIPTION
Test Mode	D[47] - D[45]	001: Test1 (write), 010: Test2(read)
(none)	(D[44])	(not used)
TRIM_DTC0	D[43] - D[42]	Trimming for DTC of Tr/Tf, CH-1,CH-2
TRIM_DTCR0	D[41] - D[40]	Trimming for DTC of Tr, CH-3,CH-8
TRIM_DTCR1	D[39] - D[38]	Trimming for DTC of Tr, CH-7
TRIM_DTCF0	D[37] - D[36]	Trimming for DTC of Tf, CH-3,CH-8
TRIM_DTCF1	D[35] - D[34]	Trimming for DTC of Tf, CH-7

TRIMMING BITS

NAME	POSITION	DESCRIPTION
TestMode	D[47] - D[45]	100: Test1(write), 101: Test2(read)
TRIM_BG	(5[bit])	Trimming for Band-Gap Reference Voltage
TRIM_OSC	(3[bit])	Trimming for Oscillator Frequency
TRIM_GAIN0	(2[bit])	Trimming for AMP Gain of CH-1
TRIM_VOFF0	(2[bit])	Trimming for AMP Offset Voltage of CH-1

PROTECTION STATUS READ MAP

NAME	POSITION	DESCRIPTION
TestMode	D[47] - D[45]	011: Test3
SCP7	D[12]	SCP7 to Previous System Down
(none)	(D[11])	(not assigned, always *L*)
SCP5	D[10]	SCP5 to Previous System Down
SCP4	D[09]	SCP4 to Previous System Down
SCP3	D[08]	SCP3 to Previous System Down
SCP2	D[07]	SCP2 to Previous System Down
SCP1	D[06]	SCP1 to Previous System Down
OVP7	D[05]	OVP7 to Previous System Down
OVP6	D[04]	OVP6 to Previous System Down
OVP3	D[03]	OVP3 to Previous System Down
OVP2	D[02]	OVP2 to Previous System Down
TSD	D[01]	TSD to Previous System Down

TPS65520 BLOCK CONFIGURATION

Figure 16 shows the overall block configuration of the TPS65520. Note that the figure is simplified for clarity and does not necessarily show accurate details for the IC wiring, pin layout, and internal component layout.

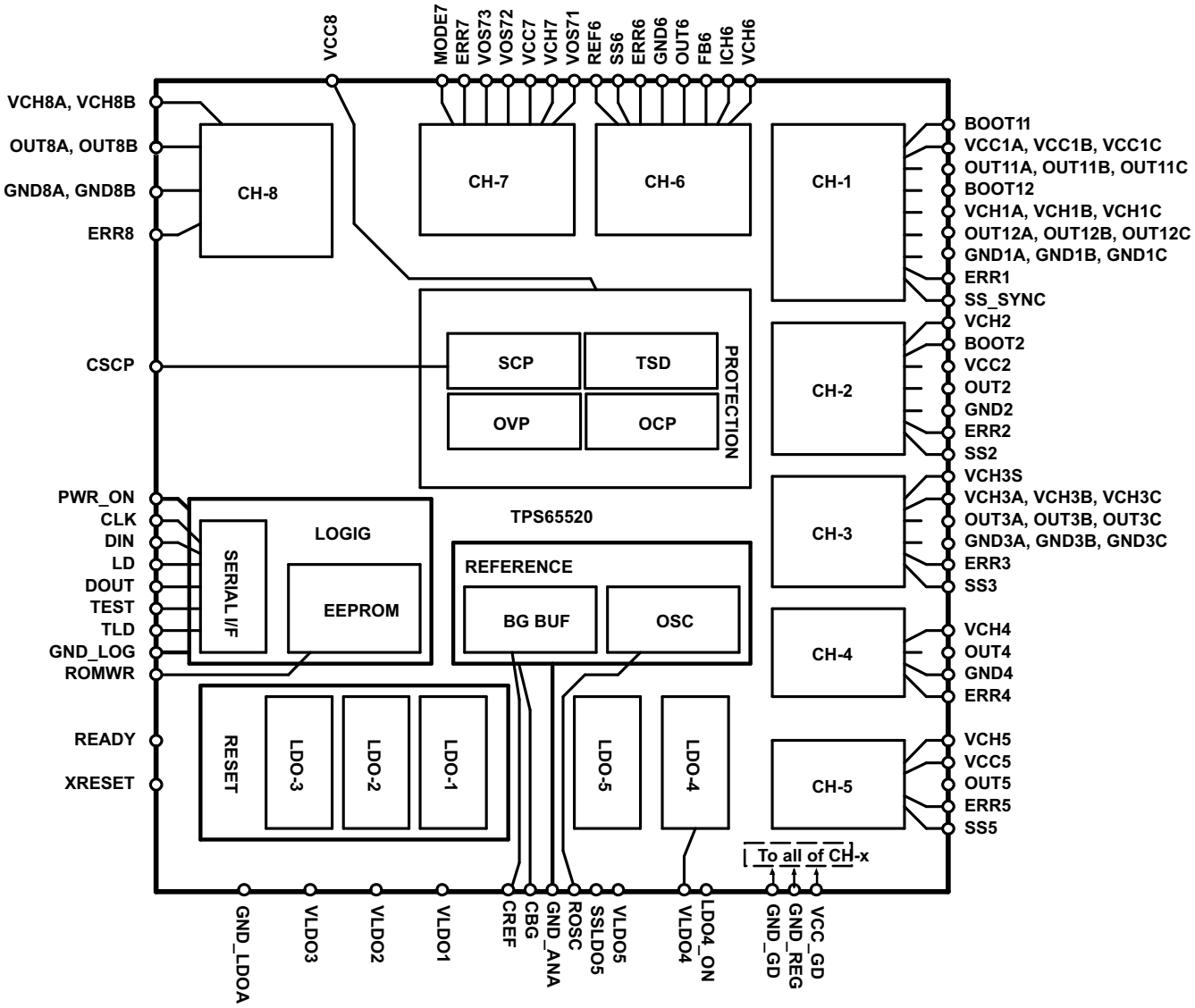


Figure 16. TPS65520 Block Diagram

FUNCTIONAL DESCRIPTION

COMMON SWITCHING REGULATOR FUNCTIONS

The following describes common features for all switching regulators.

MAXIMUM DUTY CYCLE CONTROL

Maximum duty cycle control is applied to each channel to prevent a 100%-on condition.

For CH-3, CH-4, CH-5, CH-6, and CH-7, control registers are provided to adjust the maximum duty cycle settings, affecting the channel characteristics substantially.

For CH-1 (step-up and step-up/down) and CH-8, which have relatively large margins for maximum duty cycle control, settings are linked to CH-3 to simplify circuits.

The following table lists settings for each channel:

Table 3. Settings for Each Channel

CHANNEL CONTROL	SETTINGS
CH-1 (step-up, step-up/down)	(Dmax3)
CH-1 (step-down)	Fixed at 95%
CH-2	Fixed at 95%
CH-3	Dmax3
CH-4	Dmax4
CH-5	Dmax5
CH-6	Dmax6
CH-7	Dmax7
CH-8	(Dmax3)

DEAD TIME CONTROL

The synchronous rectification channels are subjected to dead time control to prevent a flow-through current. The dead time for each channel is fixed by the EEPROM, as shown in the following table:

Channel	CH-1	CH-2	CH-3	CH-7	CH-8
Dead time	30[ns]	30[ns]	30[ns]	40[ns]	30[ns]

CH-1

CH-1 is a step-up/down switching regulator for I/F 3-V power supplies, including those for the main processor, DSP, and ASIC. Figure 17 shows its block diagram and the connection of external devices.

CH-1 operates by automatically switching between two modes: step-up to step-up/down mode and step-down mode. In Step-up to step-up/down mode, the channel smoothly shifts between step-up and step-up/down operations within the single mode.

The following table shows the rough relationship between the input voltage and CH-1 mode. Note that the threshold values shown in the table are merely guidelines because the actual CH-1 circuit finely adjusts the threshold voltages to maximize efficiency. *Electrical Characteristics* section for the voltage specifications of thresholds for switching between step-up to step-up/down mode and step-down mode (Vmod11 and Vmod12).

CH-1 incorporates a voltage retention circuit that maintains the boosting power supply voltage when the channel is performing step-up only or step-down only operation.

CH-1 supports the SCP and soft start functions. The soft start function is common to CH-1, CH-4, and CH-7.

VCC1 [V] (1)	CH-1 MODE	OPERATION
~ 2.3	Step-up to step-up/Down	Step-up
2.3 ~ 3.78	Step-up to step-up/down	Step-up/down
3.5 ~	Step-down	-

(1) The voltages shown are merely guidelines.

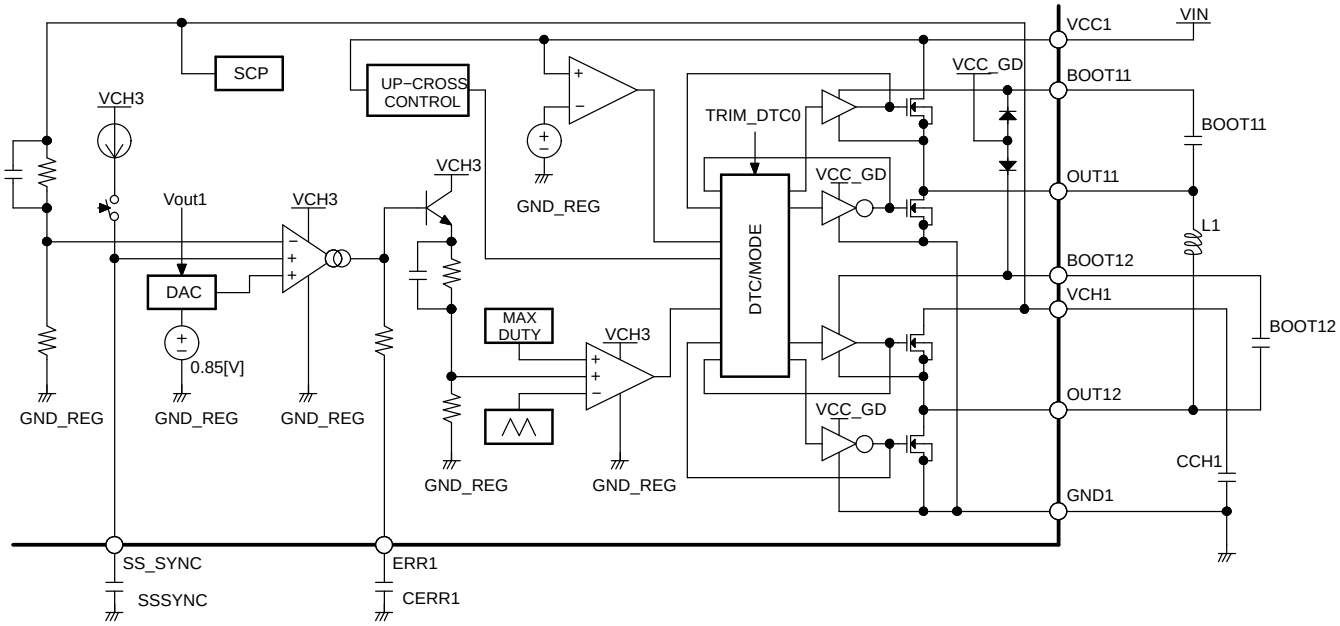


Figure 17. CH-1 Block Diagram

CH-2

CH-2 is a step-down switching regulator for core 1.x-V power supplies, including those for the main processor, DSP, and ASIC. Figure 18 shows the block diagram and the connection of external devices.

CH-2 supports the OVP, SCP and soft start functions.

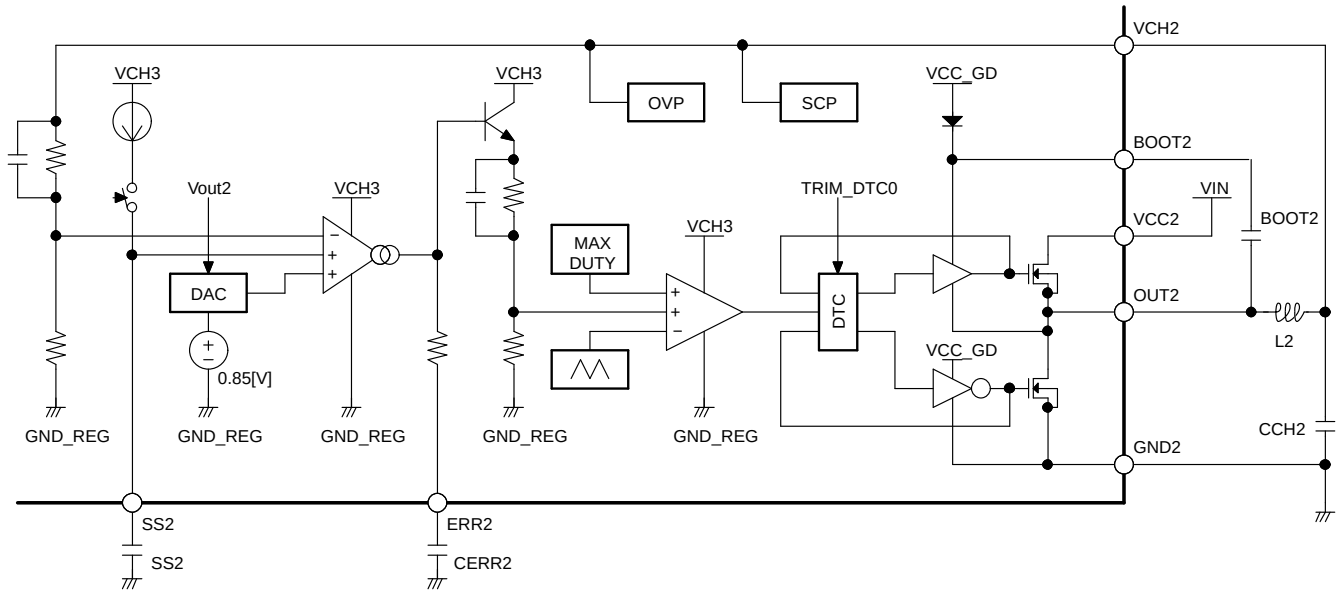


Figure 18. CH-2 Block Diagram

CH-3

CH-3 is a step-up switching regulator for 5-V power supplies, including those for the motor and audio IC. Figure 19 shows its block diagram and the connection of external devices.

CH-3 incorporates a PMOS switch, which prevents the input voltage from appearing on the output side when the channel is turned off. Without the switch, the parasitic diode in the internal PMOS would carry the input voltage from coil L3 and cause a current to flow into the load. This switch turns the VCH3S output pin on or off according to the settings in the CH3-SW control register.

The motor driver, as a load for CH-3, is a switch itself. It does not have a current path so that it can be connected to the VCH3 pin. Other current loads, which may have current paths, are intended to be connected to the VCH3S pin.

When CH-3 is activated, CH-8 supplies power to CH-3. To prevent overload on CH-8 during startup, CH-3 compares VCH8 and VCH3 and performs asynchronous rectification using a body diode until VCH3 exceeds VCH8.

CH-3 supports the OVP, SCP and soft start functions.

When using the TPS65520, note the following:

- The following conditions must be satisfied to use a 5-V AC adaptor:
  - An appropriate voltage drop circuit is provided so that the input voltages for step-up CH-3 are at least 0.3 V lower than the values specified with the control register.

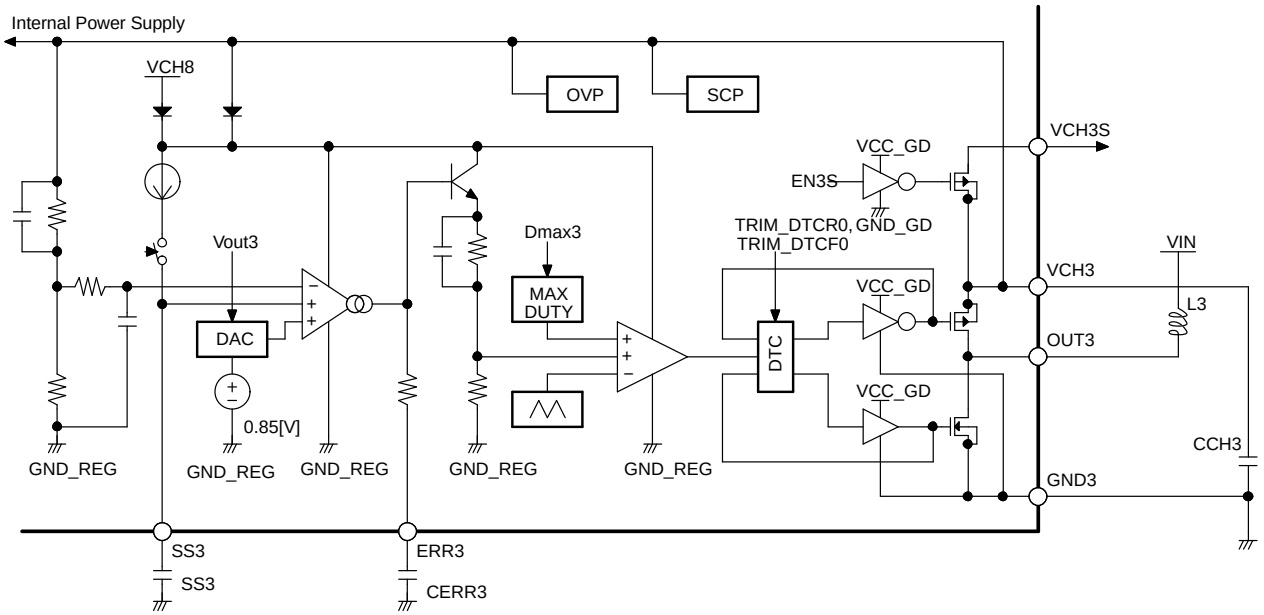


Figure 19. CH-3 Block Diagram

CH-4

CH-4 is a step-up switching regulator for 15-V power supplies the LCD and CCD. Figure 20 shows its block diagram and the connection of external devices.

CH-4 is controlled by asynchronous rectification because it outputs a high voltage and does not benefit much from synchronous rectification. An external SBD is connected between the OUT4 and VCH4 pins as a rectification device for CH-4.

CH-4 supports the SCP and soft start functions. The soft start function is common to CH-1, CH-4, and CH-7.

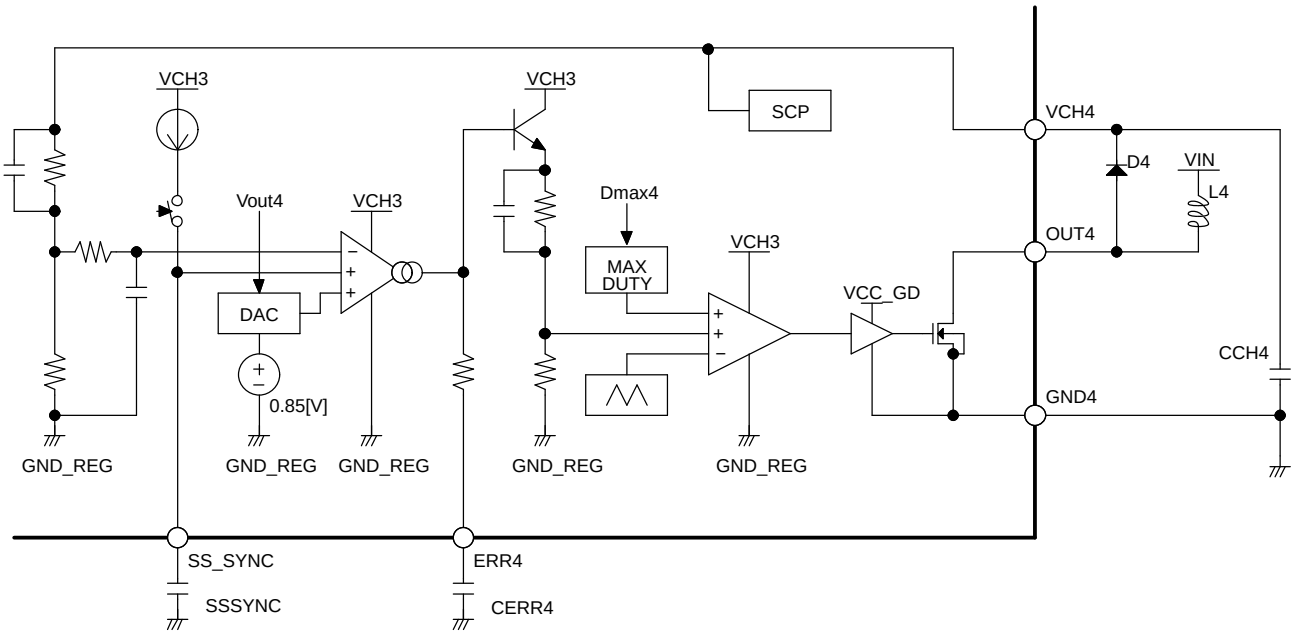


Figure 20. CH-4 Block Diagram

CH-5

CH-5 is an inversion switching regulator for -8-V power supplies for the LCD and CCD. Figure 21 shows its block diagram and the connection of external devices.

CH-5 supports the SCP and soft start functions.

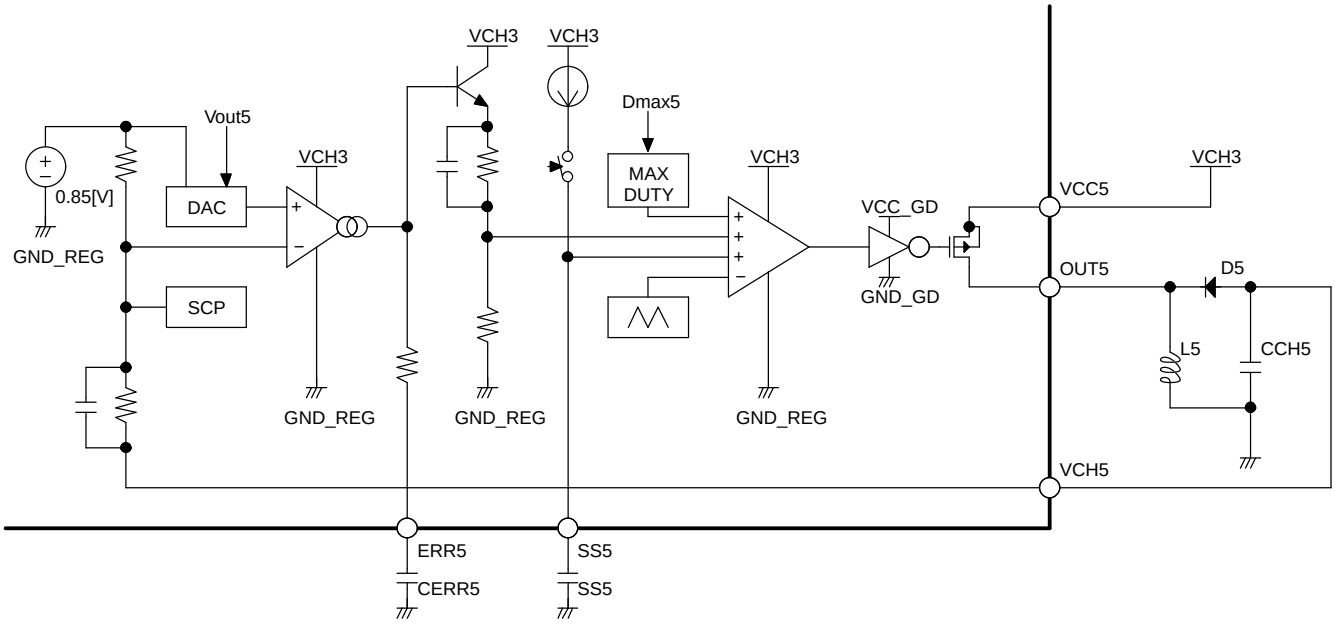


Figure 21. CH-5 Block Diagram

CH-6

CH-6 is a step-up switching regulator for driving the power supply for the LCD backlight LED. CH-6 is controlled by monitoring the current flowing through the LED so that it operates as a constant-current driver. Figure 22 shows the block diagram and the connection of external devices.

The output current for CH-6 can be finely adjusted using the REF6 pin. The output current becomes the value specified with the Vout6B control register when the potential of the REF6 pin equals that of the CBG pin. Note that the REF6 pin always expects a voltage being applied to it. To ensure that an appropriate voltage is applied to the REF6 pin, for example, connect it to a DAC or to the CBG pin through a resistor. The following formulas show the relationship between the voltage on the REF6 pin and that on the FB6 pin, which senses the output current:

20 mA setting	V(FB6) = 0.52 × V(REF6) – 0.002
12 mA setting	V(FB6) = 0.52 × V(REF6) – 0.177
8 mA setting	V(FB6) = 0.52 × V(REF6) – 0.265

For example, when using 0.85V of CBG as reference voltage and using 22Ω of recommended sense resistor, the caluculation is like this: Iout = V(FB6) / Rsense = (0.52 x 0.85[V] - 0.002) / 22[Ω] = 20[mA].

CH-6 supports the OVP, SCP and soft start functions.

Without serial I/F control, CH-6 is controlled by the voltage of REF6. When the potential of REF6 is out of range between VREF6L and VREF6H, CH-6 is OFF in logical. Soft start is reset.

CH-7

According to the state of the MODE7 pin, CH-7 operates either as a step-up switching regulator for 5-V power supplies, including those for the motor and audio IC, or as a step-down switching regulator for I/F 3-V power supplies, including those for the main processor, DSP, and ASIC. The following table shows the relationship between the state and mode:

MODE7	MODE
H	Step-up
L	Step-down

CH-7 requires different external component connections depending on the MODE7 pin state. Figure 23 shows its block diagram and the connection of external devices for Step-up mode. Figure 24 shows its block diagram and the connection of external devices for Step-down mode.

When using the TPS65520, note the following:

- The following conditions must be satisfied to use a 5-V AC adaptor:
  - An appropriate voltage drop circuit is provided so that the input voltages for step-up CH-7 (MODE7 = H) are at least 0.3 V lower than the values specified with the control register.

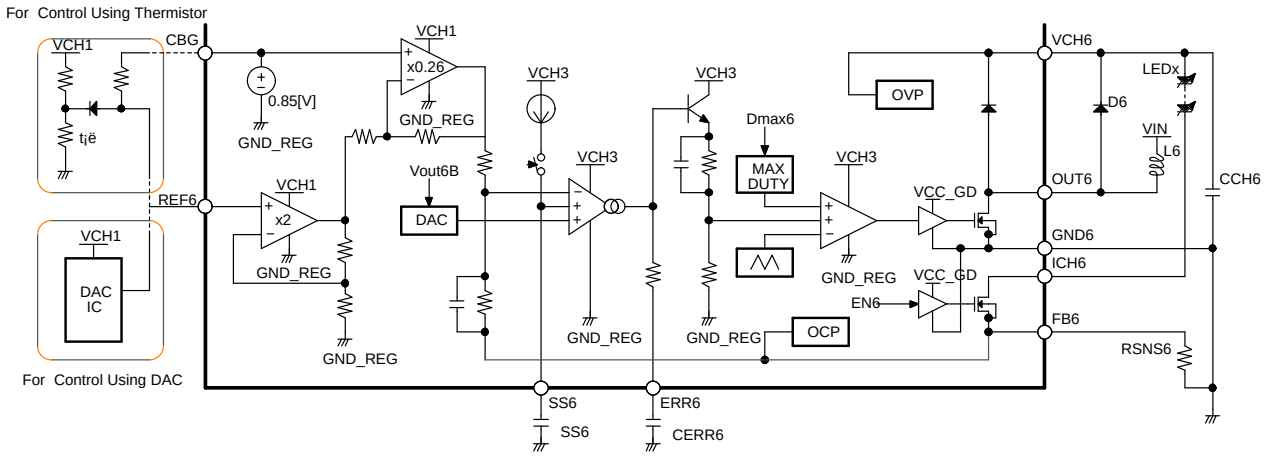


Figure 22. CH-6 Block Diagram

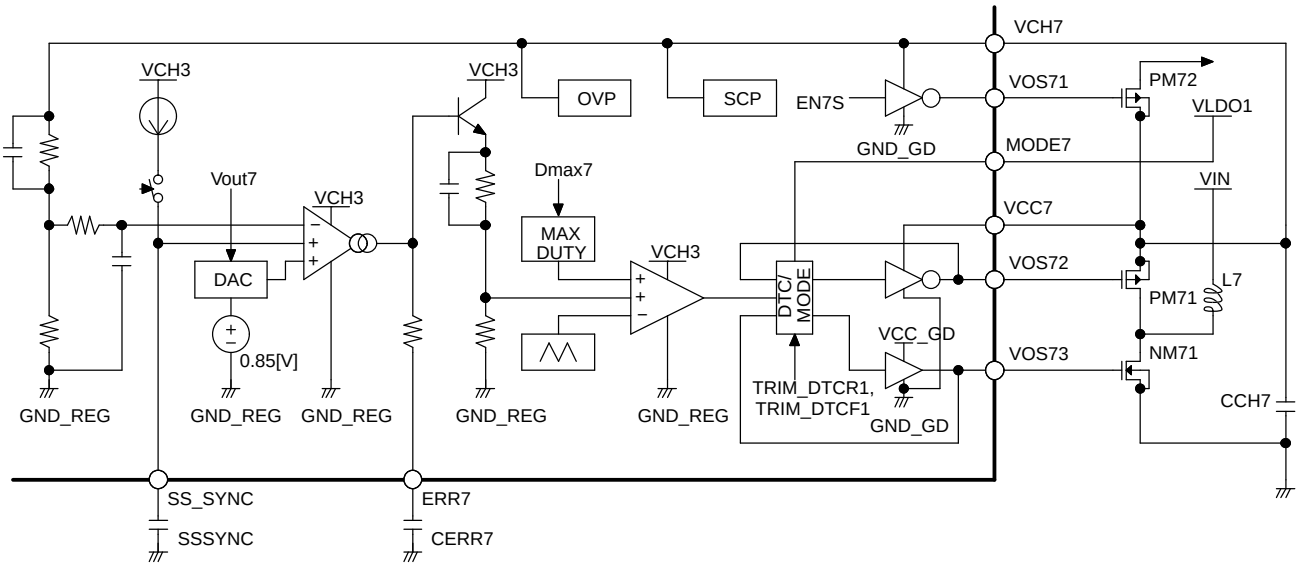


Figure 23. CH-7 Block Diagram (Step-up)

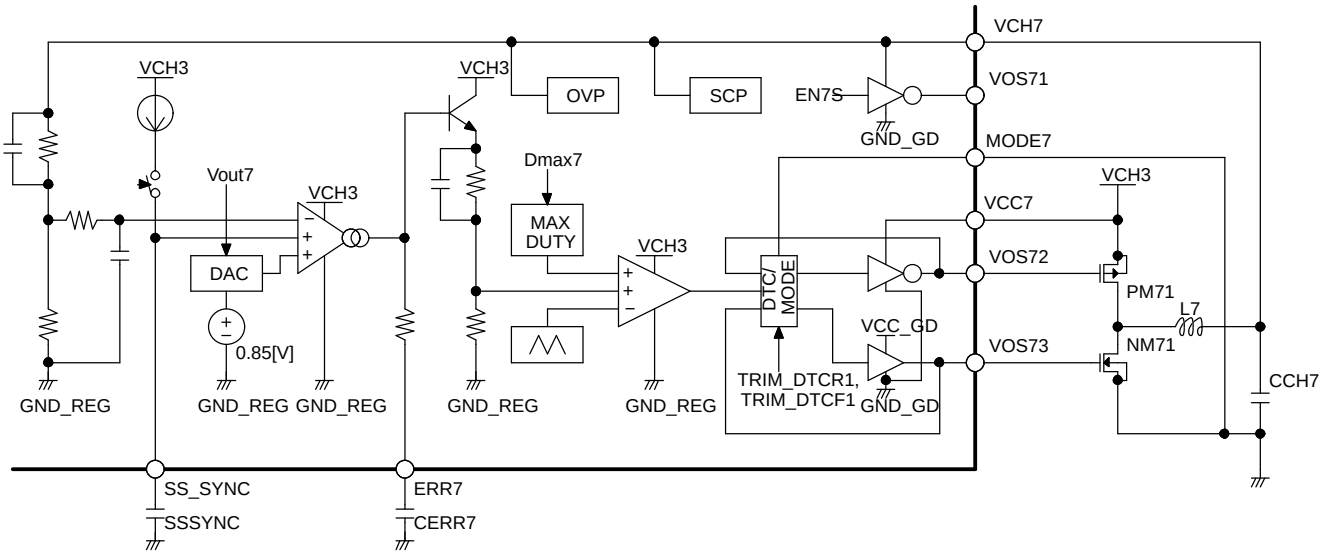


Figure 24. CH-7 Block Diagram (Step-down)

As shown in Figure 24, the step-down circuit configuration uses CH-3 as an input power supply that assures a voltage higher than the output voltage.

CH-7 has the VOS71 pin for controlling a separate PMOS switch, preventing the input voltage from appearing on the output side when the channel is turned off (MODE7 = H). Without the switch, the parasitic diode in the external PMOS would carry the input voltage from coil L7 and cause a current to flow into the load. This switch turns on or off according to the settings in the CH7-SW control register.

When CH-7 is activated, CH-8 supplies power to CH-7. To prevent overload on CH-8 during startup, CH-7 compares VCH8 and VCH7 and performs asynchronous rectification using a body diode until VCH7 exceeds VCH8.

CH-7 supports the OVP, SCP and soft start functions. The soft start function is common to CH-1, CH-4, and CH-7.

When CH-7 is not used, handle the pins as shown below. CH-7 will enter Step-down mode with its state equal to the stable output state, stopping operation.

PIN	HANDLING
ERR7	0.1 µF - Connect a 0.1-µF capacitor between the pin and the ground
VCH7	VCH1 - Short-circuit to VCH1
VOS71	Open
MODE7	Short-circuit to the ground
VCC7	Open
VOS72	Open
VOS73	Open

CH-8

CH-8 is a step-up switching regulator for LDO-1, LDO-2, LDO-3, LDO-4, and the internal power supplies of the TPS65520. CH-8 is a 3.6-V output regulator and outputs the input voltage (VCC8) when it is higher than 3.6 V.

CH-8 is turned on whenever the battery and/or ac adaptor is connected. It operates in Skip mode while the PWR_ON pin is low, meaning that only the Sub-CPU real-time clock is operating. Once the PWR_ON pin is driven high, CH-8 enters Synchronous rectification mode, where it can supply the maximum load current.

CH-8 has a startup circuit that can start with a low input voltage because the startup of CH-8 enables the entire DSC system to start up. It outputs 3.6 V from a minimum input voltage (VCC8) of 1.6 V.

See the CH-8 operating sequence for details of starting CH-8.

Figure 25 shows its block diagram and the connection of external devices.

CH-8 supports the soft start function.

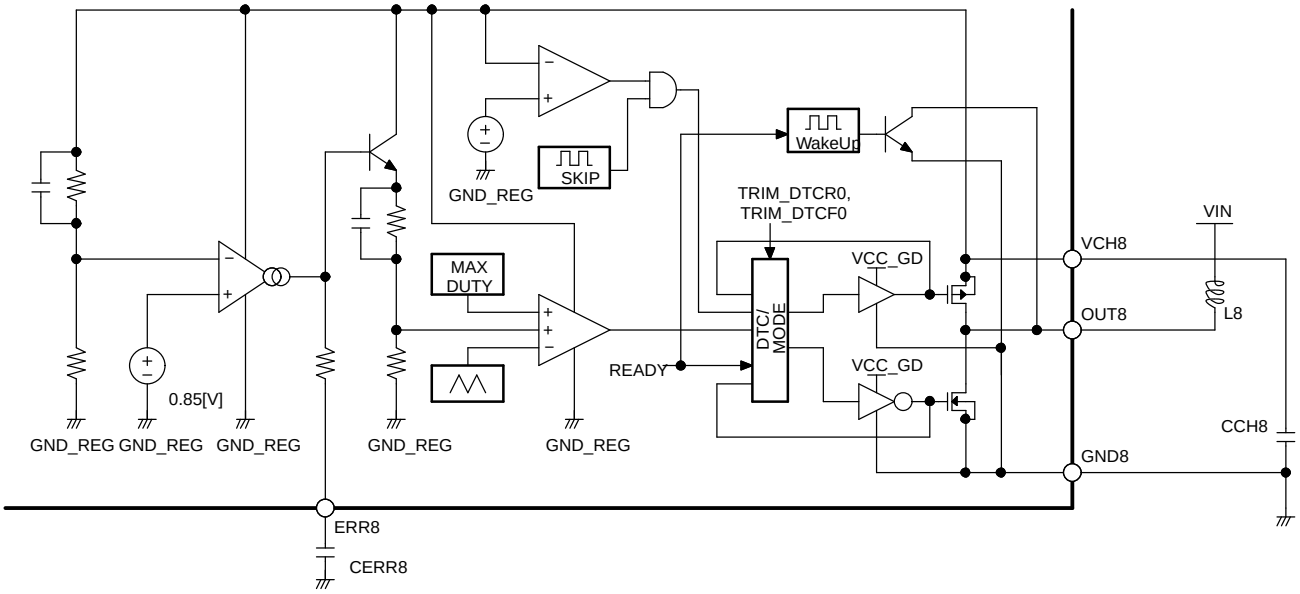


Figure 25. CH-8 Block Diagram

LDO-1

LDO-1 takes the CH-8 output voltage as an input and outputs a voltage of 2.9 V. LDO-1 supports a current limit function, which reduces the output voltage when the current exceeds the specified value.

LDO-2

LDO-2 takes the CH-8 output voltage as an input and outputs a voltage of 2.9 V. LDO-2 supports a current limit function, which reduces the output voltage when the current exceeds the specified value.

LDO-3

LDO-3 takes the CH-8 output voltage as an input and outputs a voltage of 3.1 V. LDO-3 supports a current limit function, which reduces the output voltage when the current exceeds the specified value. LDO-3 can be turned on/off using the LDOSW3 control register.

A delay is inserted before LDO-3 is turned on so that the entire system can start up and be stable. LDO-3 cannot be turned on until approximately 30 µs elapse after the detection of READY. DELAY2 in Figure 29 represents this delay.

LDO-4

LDO-4 takes the CH-8 output voltage as an input and outputs a voltage of 3.1 V. LDO-4 supports a current limit function, which reduces the output voltage when the current exceeds the specified value.

To prevent an inrush current during startup, LDO-4 has a delay so that it is not turned on simultaneously with LDO-3. LDO-4 cannot be turned on until 1.03 ms elapses after the detection of READY. This ensures that LDO-4 is not turned on until 1 ms elapses after the startup of LDO-3, which is turned on 30 µs after READY detection. DELAY3 in Figure 29 represents this delay.

LDO-4 is controlled using the LDO4_ON pin, as follows:

USB ON	ON/OFF
H	On
L	Off

LDO-5

LDO-5 takes the CH-4 output voltage as an input and outputs a voltage of 8.5V to 13.5V for the LCD panel. LDO-5 supports a current limit function, which reduces the output voltage when the current exceeds the specified value. LDO-5 can be turned on/off using the LDOSW5 control register. LDO-3 has a soft start pin because it drives a lot of power.

PROTECTION FUNCTIONS

TSD

The thermal shutdown (TSD) function protects the TPS65520 from overheat.

If the TSD activates, the TPS65520 stops all channels other than CH-8. CH-8 expects that the Sub-CPU drives PWR_ON low due to the stop of CH-1 and CH-2, causing the TPS65520 to enter Skip mode.

SCP

The short-circuit protection (SCP) function protects the output of each switching regulator from short-circuiting. If the SCP activates, the TPS65520 stops all channels other than CH-8. CH-8 expects that the Sub-CPU drives PWR_ON low due to the stop of CH-1 and CH-2, causing the TPS65520 to enter Skip mode.

Figure 26 shows the block diagram and the connection of external devices.

Per-channel short-circuit information from control section for each switching regulator

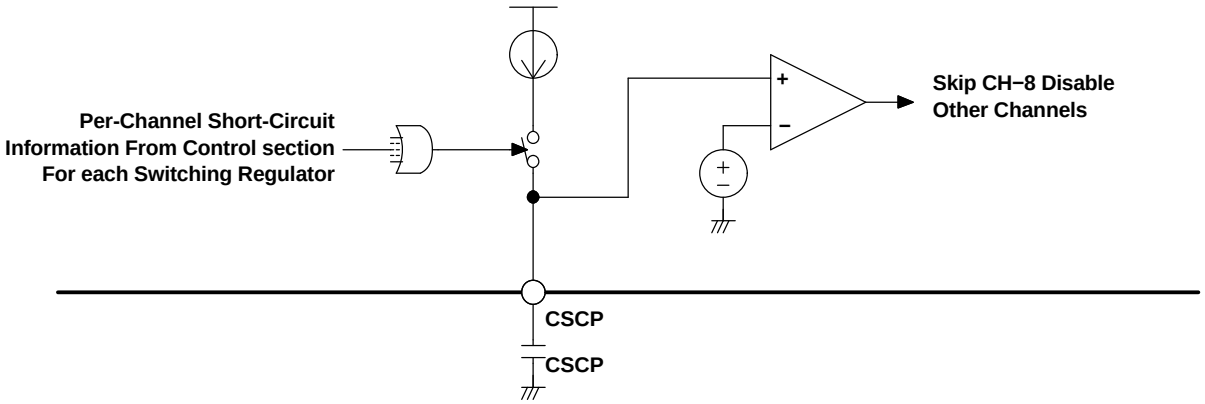


Figure 26. SCP Block Diagram

OVP

The overvoltage protection (OVP) function protects the CH-2, CH-3, CH-6, and CH-7 outputs from overvoltage.

If the OVP for CH-6 activates, the TPS65520 internally latches the CH-6 OVP and disables CH-6. The MOS switch between ICH6 and FB6 is designed to remain on if the OVP activates and discharges the VCH6 potential through a diode and sense resistor. To cancel the OVP for CH-6, drive PWR_ON low. The OVP for CH-6 affects the CH-6 output only.

If the OVP for a channel other than CH-6 activates, the TPS65520 disables the power MOS-FET switching for that channel while still allowing the operation of the channel.

The OVP for channels other than CH-6 does not have a latch function so that the TPS65520 automatically restores normal operation once it exits from the overvoltage state.

OCP

The overcurrent protection (OCP) function protects the CH-6 output from overcurrent.

The OCP monitors the FB6 pin and, if its voltage exceeds 0.85 V, it determines that an overcurrent is flowing through CH-6. If the OCP activates, the TPS65520 disables power MOS-FET switching for CH-6 while still allowing the operation of CH-6. In the same way as with the OVP, the MOS switch between ICH6 and FB6 is designed to remain on if the OCP activates and discharges the VCH6 potential through a diode and sense resistor.

The TPS65520 restarts switching once the voltage on the FB6 pin falls below 0.85 V. The OCP does not have a latch function so that the TPS65520 automatically restores normal operation once it exits from the overcurrent state.

SUB-CPU CONTROL (RESET)

The Sub-CPU function monitors the LDO-2 voltage to output XRESET, and it monitors VCH8 to output READY.

Figure 27 shows a block diagram of this function.

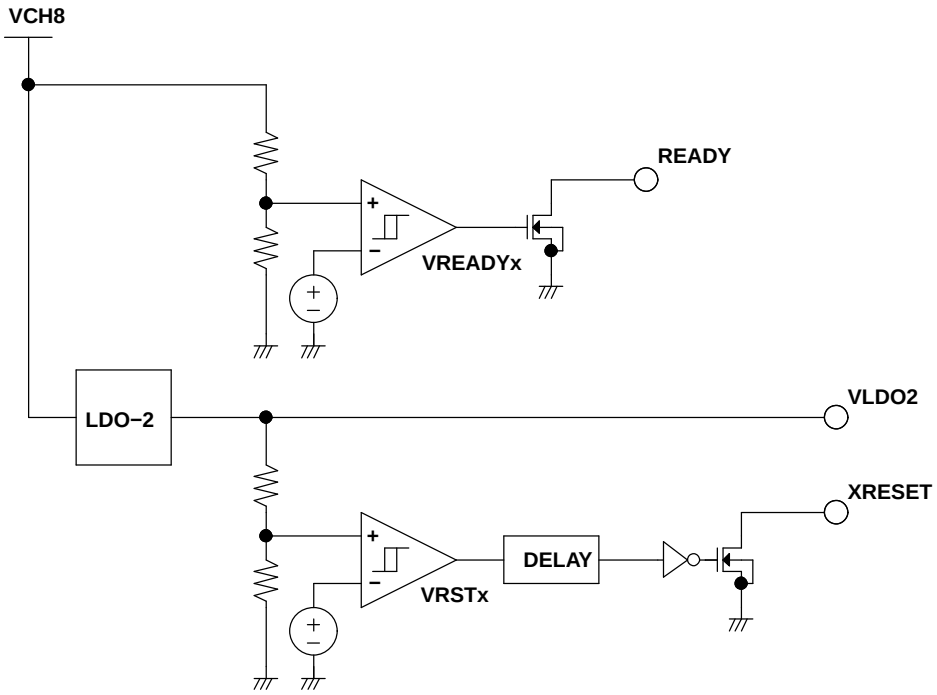


Figure 27. Sub-CPU Control Block Diagram

OPERATION SEQUENCE

SOFT START

The soft start function of the TPS65520 controls the constant-current charging of the capacitors connected to the SS_SYNC, SS2, SS3, SS5, SS6, and SSLDO5 pins based on their pin voltages. When the voltage at a soft start pin becomes approximately 0.85 V, its corresponding regulator output becomes 100%.

SOFT START OK SIGNAL FOR CH-3

The soft start circuit for CH-3 has a logic output (internal signal) function that indicates the end of soft start for sequence control.

Figure 28 shows the entire soft start circuit. As shown, the voltage on the SS3 pin is used as a reference for the CH-3 control section. The control section operates based on the SS3 voltage or the band gap buffer reference voltage for the CBG pin, whichever is lower.

In Figure 28, the comparator that outputs the SS3OK signal implements the logic output function for sequence control. The threshold value for the comparator is set to a value (VSS3OK) that is sufficiently higher than the band gap buffer reference voltage. It can be assumed that CH-3 has been started when the comparator outputs the SS3OK signal, except when the CH-3 load is heavy or short-circuited.

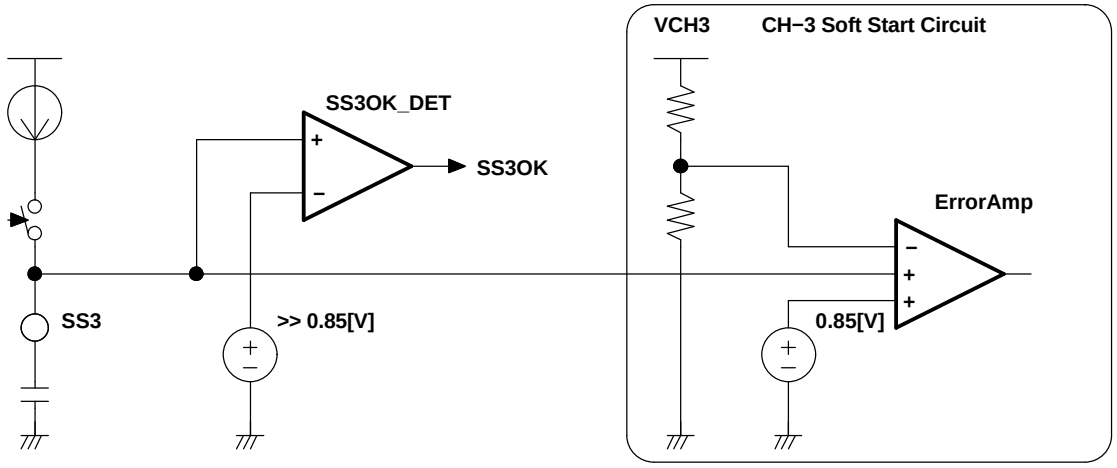


Figure 28. CH-3 Soft Start Circuit

SEQUENCE CONTROL

Most operations of the TPS65520 are controlled by the Sub-CPU. When a valid power supply, ac adaptor, or battery is inserted, the TPS65520 automatically activates the Sub-CPU. If a Sub-CPU does not exist, the TPS65520 automatically activates the regulators and LDOs using the default values for control registers.

Figure 29 shows the connection of enable signals for the TPS65520. Figure 30 shows a timing chart. In Figure 30, ENREGs, EN3S, EN6, EN7, ENLDO3, and ENLDO5 represent the internal enable signals shown in Figure 29.

The following describes the relationship among enable signals in

1. Upon power-up, the TPS65520 starts the wake-up circuit for CH-8 and activates the VCH8 potential. In the figure, only CH-8 is operating.
2. Once VCH8 rises, the READY detection circuit is activated and detects READY.
3. Upon the detection of READY, CH-8 exits from the wake-up state and enters Skip mode. At this time, the blocks in the upper half of the figure can operate; they are turned on if the enable logic signal is valid.
4. In Skip mode after wake-up, CH-8 enters PWM mode when PWR_ON is driven high.
   a. PWR_ON has a delay of approximately 60 µs to ensure that the OSC starts completely before channels start operating. DELAY0 in the figure represents this delay.
   b. A delay of approximately 1 ms is inserted to ensure that CH-8 enters PWM mode completely before channels start operating. DELAY1 in the figure represents this delay.
5. Once CH-8 enters PWM mode, each switching regulator channel starts operating. CH-3 starts first. The SS3OK signal from CH-3 causes other channels to start.

In Figure 30, the TPS65520 performs the following operation, described along the time axis in the figure:

1. In response to CH-8 starting up, the internal logic reset signal is generated at the same time as READY being canceled, thus resetting the maintained status values.
2. On the rising edge of PWR_ON, CH-8 exits from Skip mode and enters PWM mode. The DELAY0 and DELAY1 blocks, shown in the upper part of Figure 29, insert delays to ensure that the mode transition is over before channels start operating, resulting in a total delay of 544 PWM pulses to complete this process.
3. Upon the mode transition of CH-8, CH-3 starts using the soft start procedure.
4. The SS3OK signal output during the soft start of CH-3 causes all other blocks to be enabled at one time, after which normal operation starts.
5. On the falling edge of SYDDON, all channels are disabled at one time.

The shaded portions of Figure 30 represent the on/off control applied by the Sub-CPU (if used) through the serial interface. If a Sub-CPU is used, control registers are written between the rising edges of XRESET and PWR_ON. Any channels that have been turned off will not start until the Sub-CPU turns them on again. If the Sub-CPU specifies *off* for a channel that has been active from the startup, the channel goes off from that instant.

If a Sub-CPU is not used, the timing waveforms do not have the shaded portions. All channels are turned on with default values set in the control registers.

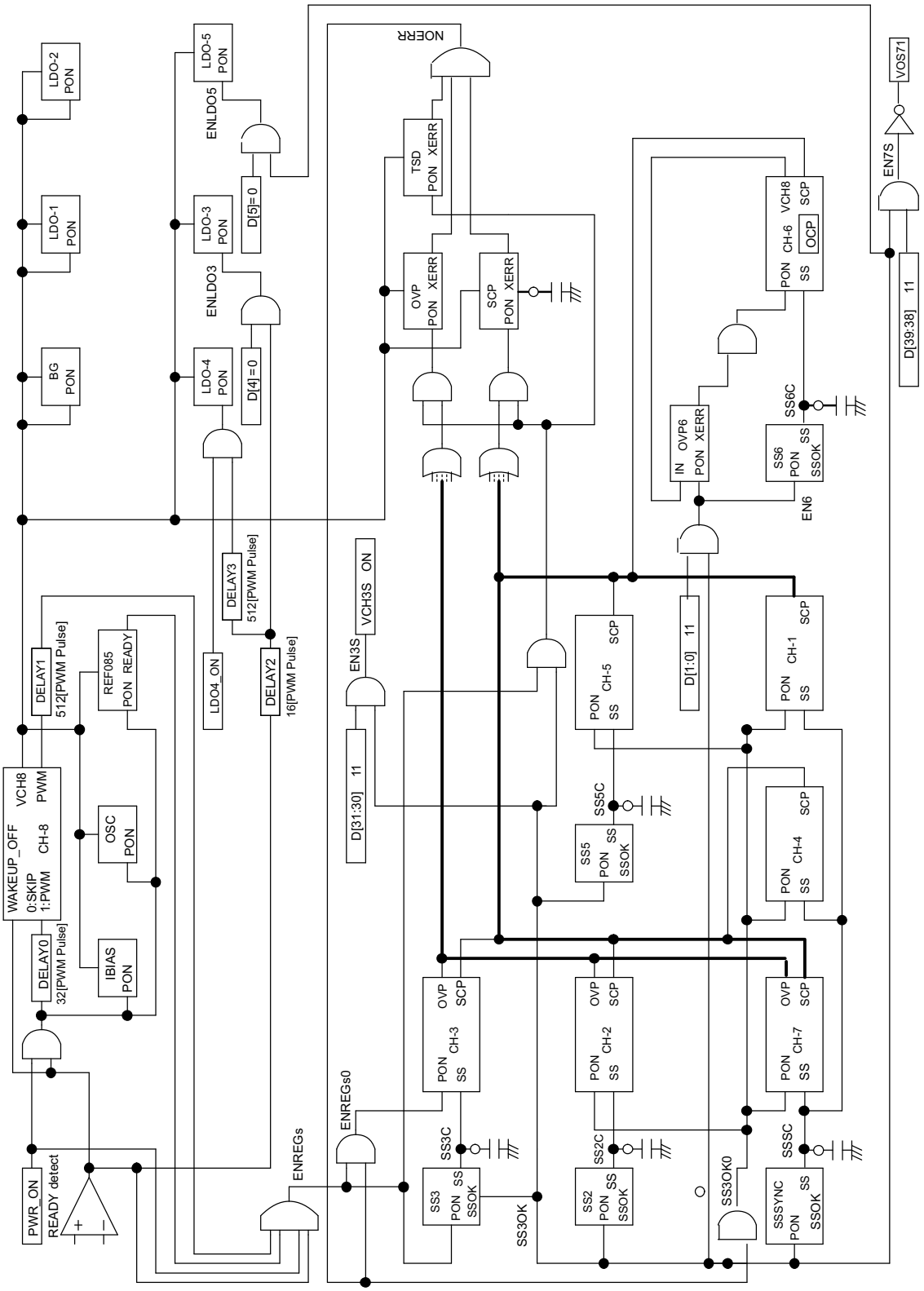


Figure 29. Enable Signal Connections

The shaded portions apply only when a Sub-CPU is used.

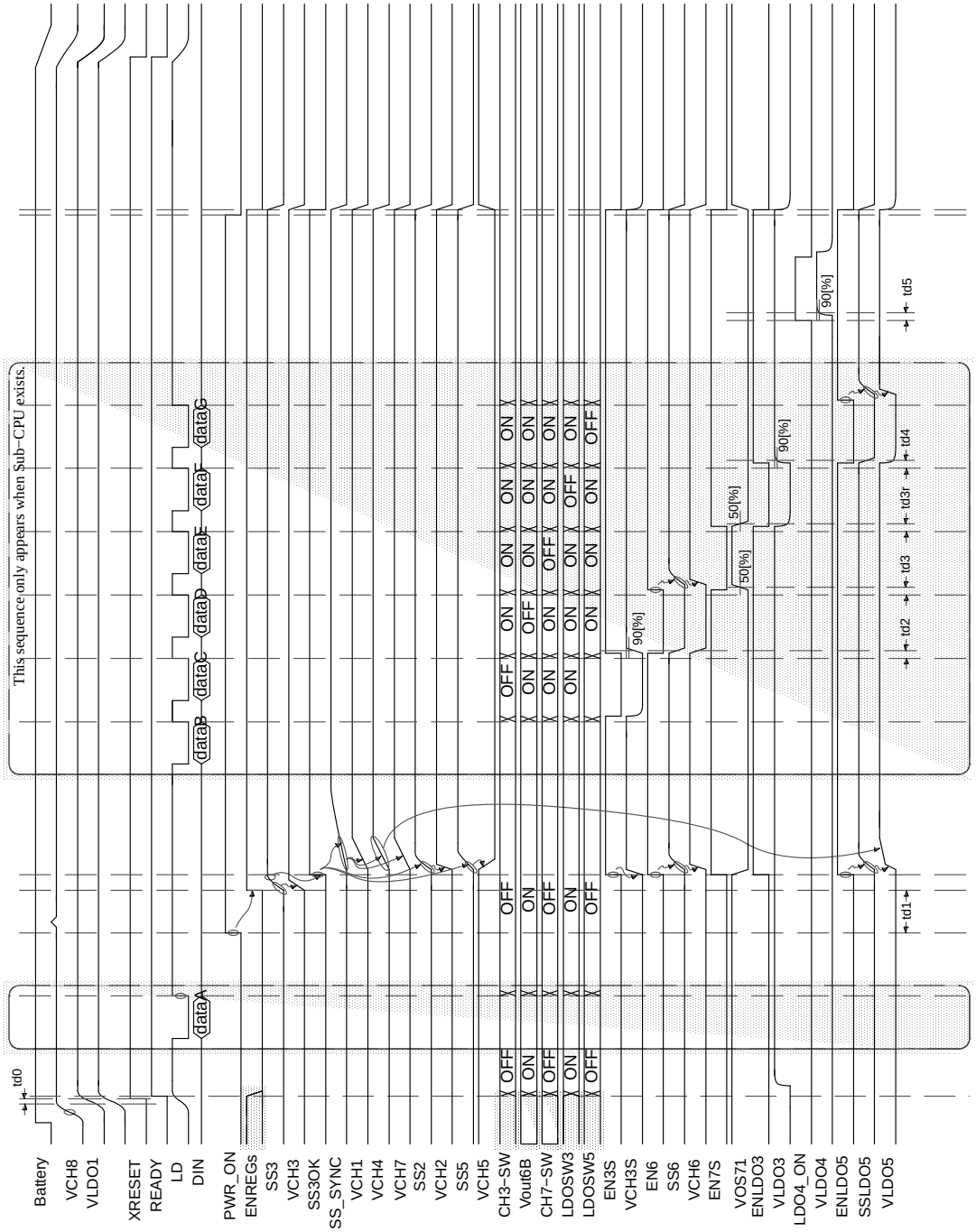


Figure 30. Operation Sequence Chart

SERIAL INTERFACE, CONTROL REGISTERS, AND EEPROMS

The logic control section of the TPS65520 consists of the serial interface, control registers, and EEPROMs. See the *EEPROM MAP* section for details of control registers, EEPROMs, and the bit assignment for reading the protection states.

The logic section operates in either of two operating modes: Para mode or Test mode. Each mode is described below.

Figure 34 shows the overall block configuration. In the figure, the 48-bit Shift Register block accepts D[47] (MSB) last in the time sequence. Figure 31 shows the configuration of the parity judgment circuit.

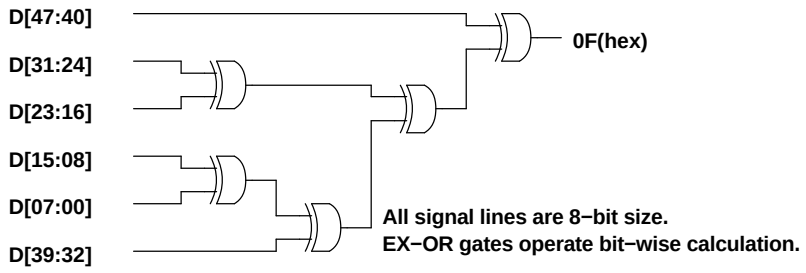


Figure 31. Configuration for Parity Bit Calculation

NORMAL MODE

Driving the TEST input signal low selects Para mode. In this mode, the TPS65520 allows access to the control registers.

Figure 32 shows the shift register configuration from input DIN to output DOUT. Figure 33 shows a single access cycle. As shown in Figure 33, once 48 bits have been input to the shift register, the TPS65520 determines the parity according to the output from DOUT and latches the input data using the LD input signal.

In Para mode, DOUT directly reflects the output from the parity check block, which is a random logic circuit. Note, therefore, that any circuit that responds to the edge of DOUT may cause malfunctioning connections.

In Para mode, the EEPROMs send the written data to each internal block.

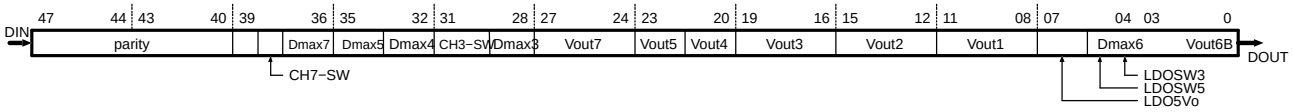


Figure 32. Shift Register Configuration in Para Mode

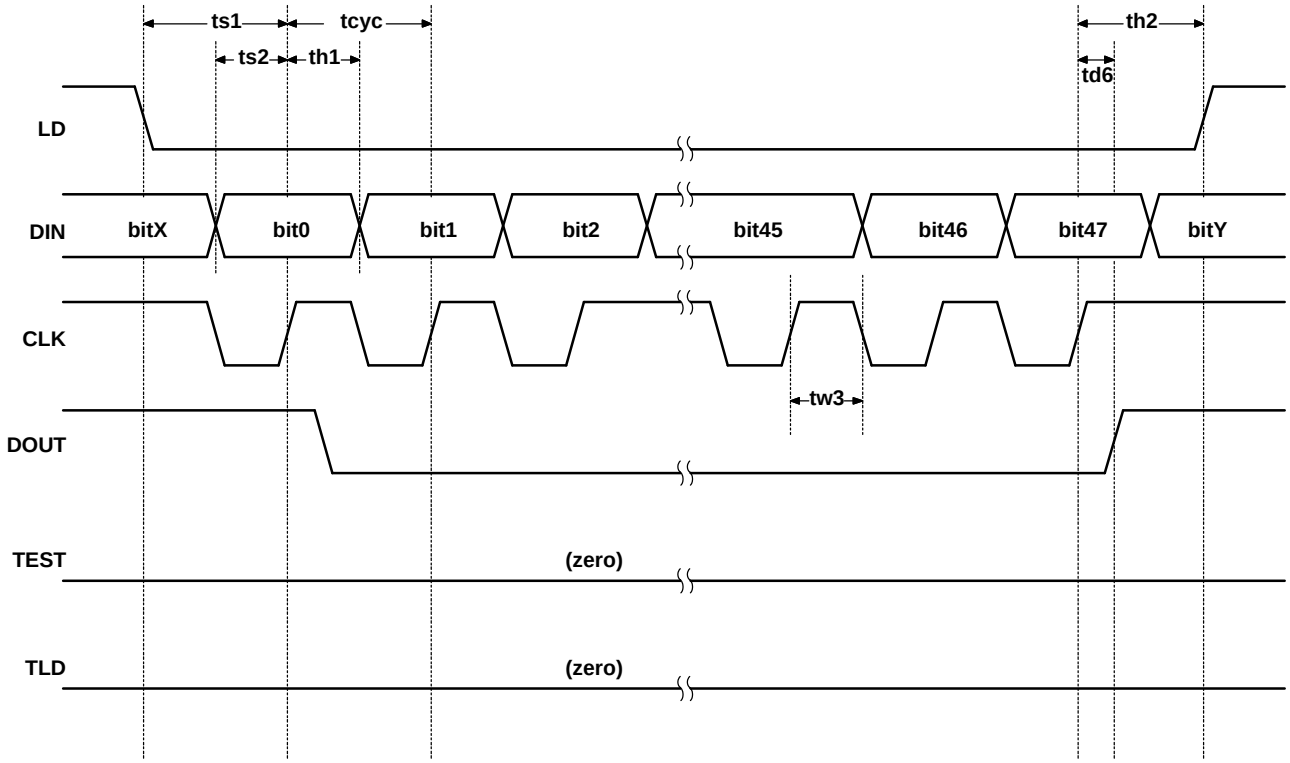


Figure 33. Serial Interface Timing Chart in Para Mode

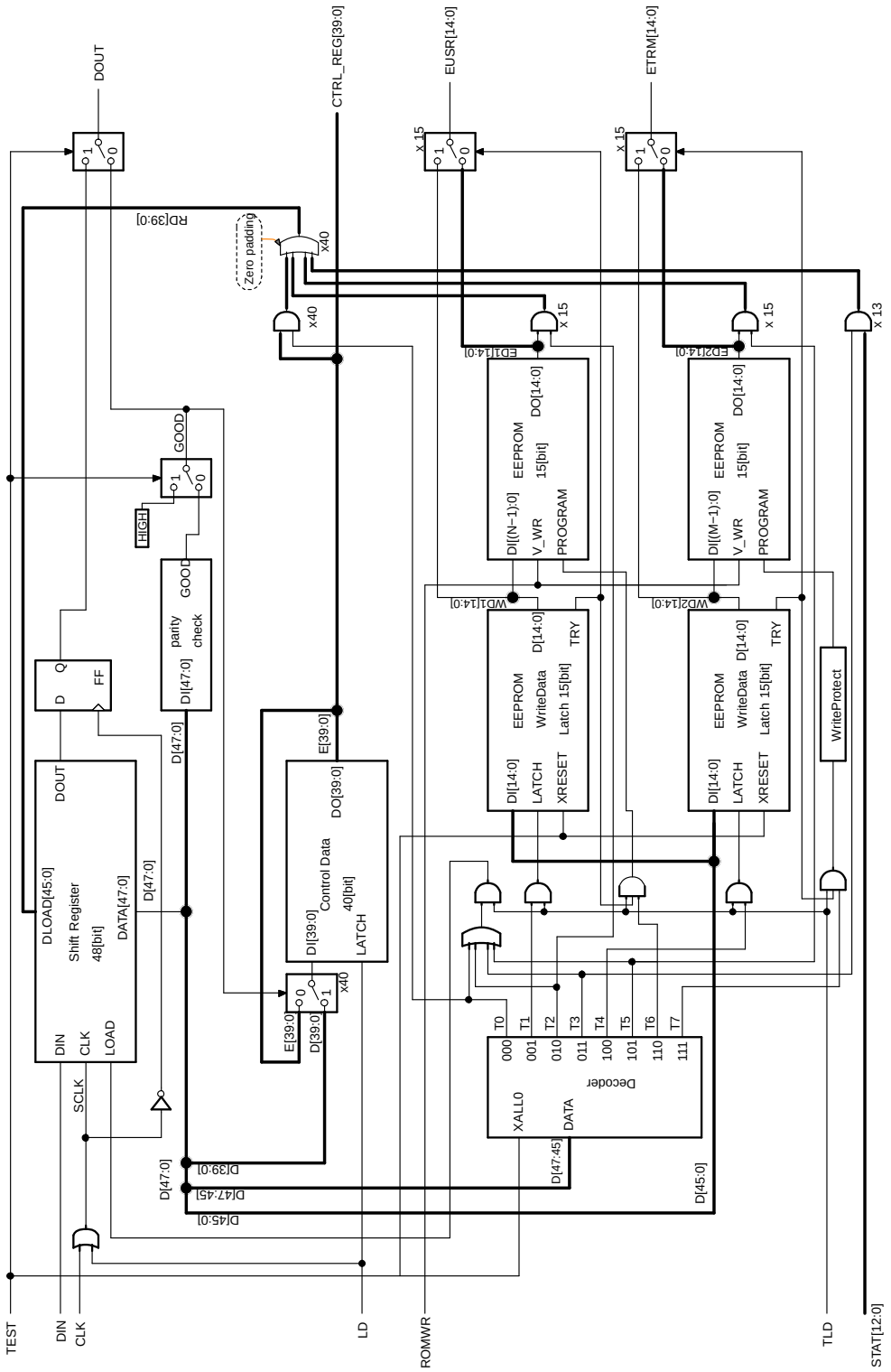


Figure 34. Serial Interface Block Diagram

TEST MODE

Driving the TEST input signal high selects Test mode. In this mode, the TPS65520 allows access to all logic functions, including EEPROMs. The following test operations are supported:

- Test A: In the same way as Para mode, the TPS65520 allows access to the control registers. Unlike Para mode, however, no parity check is performed. The parity judgment result is internally fixed to "OK" and the contents of the shift register are sent to DOUT.
- Test 0: The contents of the control registers are copied to the shift register in synchronization with the TLD input signal. After copying, a CLK input causes the control register value to appear at DOUT.
- Test 1: Prepare (latch) the data to be written to the user setup EEPROM. When Test 6 is performed subsequently, the latched data is written to the EEPROM. After the data is latched, any internal blocks that reference values from EEPROM will see the latched data, instead of the data stored in EEPROM.
- Test 2: The contents of the user setup EEPROM are copied to the shift register in synchronization with the TLD input signal. After copying, a CLK input causes the value from the user setup EEPROM to appear at DOUT.
- Test 3: The states of the protection functions are copied to the shift register in synchronization with the TLD input signal. After copying, a CLK input causes the protection state value to appear at DOUT.
- Test 4: Prepare (latch) the data to be written to the trimming EEPROM. When Test 7 is performed subsequently, the latched data is written to the EEPROM. After the data is latched, any internal blocks that reference values from EEPROM will see the latched data, instead of the data stored in EEPROM.
- Test 5: The contents of the trimming EEPROM are copied to the shift register in synchronization with the TLD input signal. After copying, a CLK input causes the value from the trimming EEPROM to appear at DOUT.
- Test 6: Data is written to the user setup EEPROM.
- Test 7: Data is written to the trimming EEPROM.
- Test Mode Switching: Test A does not require a transition to a special mode. Its operation is the same as in normal mode, except the difference in the DOUT output.
- Tests 0 to 7 require explicit mode switching using the Decoder shown in Figure 34. The Decoder uses the three high-order bits in the shift register to change the mode. Table 4 shows the bit assignment.

Table 4. Bit Assignments

D[47]	D[46]	D[45]	MODE
*	*	*	Test A
0	0	0	Test 0
0	0	1	Test 1
0	1	0	Test 2
0	1	1	Test 3
1	0	0	Test 4
1	0	1	Test 5
1	1	0	Test 6
1	1	1	Test 7

- Information Read Mode: In Test mode, Tests 0, 2, 3, and 5 have a common function: copy some TPS65520 internal logic values to the shift register and read them from DOUT. Because their operations are nearly the same, this section describes them together.

Figure 35 to Figure 38 shows the shift register configuration from input DIN and output DOUT as well as changes in the shift register caused by a TLD input pulse.

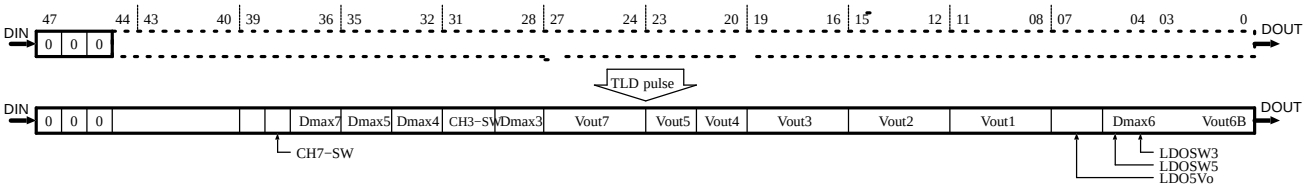


Figure 35. Shift Register Configuration and Changes for Test 0

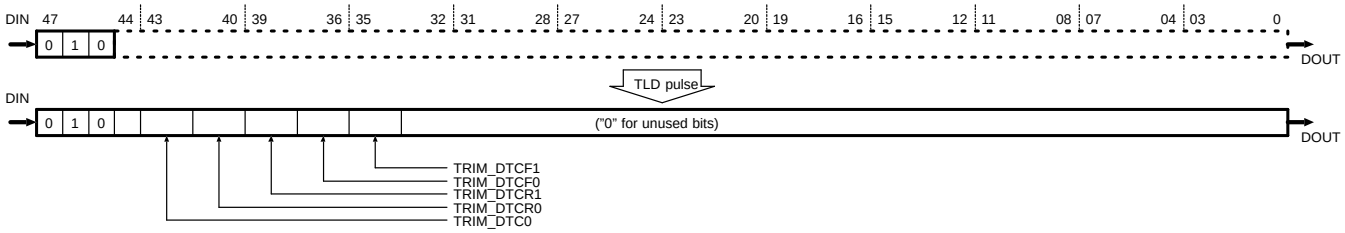


Figure 36. Shift Register Configuration and Changes for Test 2

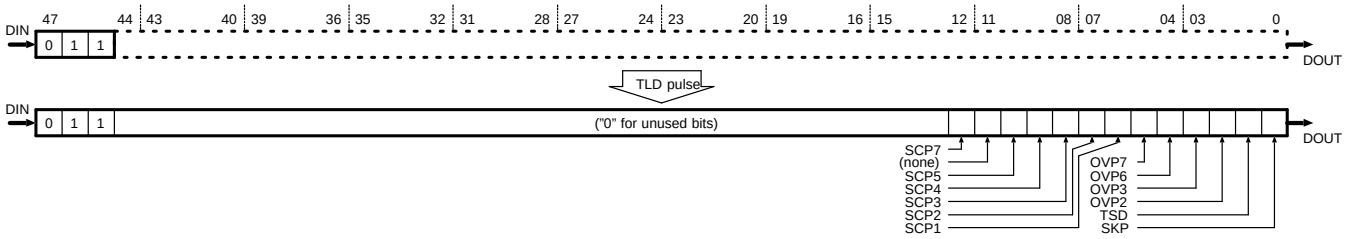


Figure 37. Shift Register Configuration and Changes for Test 3

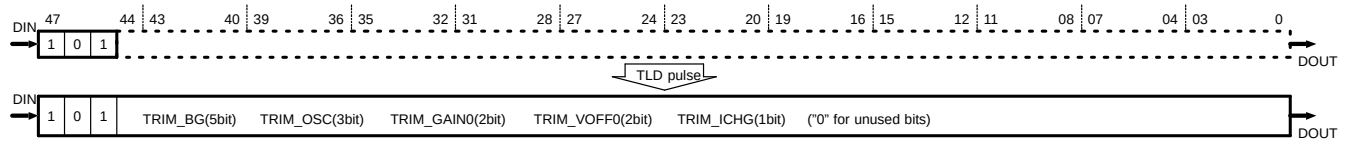


Figure 38. Shift Register Configuration and Changes for Test 5

Figure 39 takes Test 0 as an example and shows a single access cycle. As shown in the figure, a TLD input from DIN, following the input of the data 000 (bin) to select Test 0, causes the contents of the control registers to be copied to the shift register. Subsequent 48-bit CLK inputs enables the user to read data sequentially from DOUT.

The values read in Test 3 are cleared once PWR_ON is pulled high. Data should, therefore, be read while PWR_ON is low after protection activates.

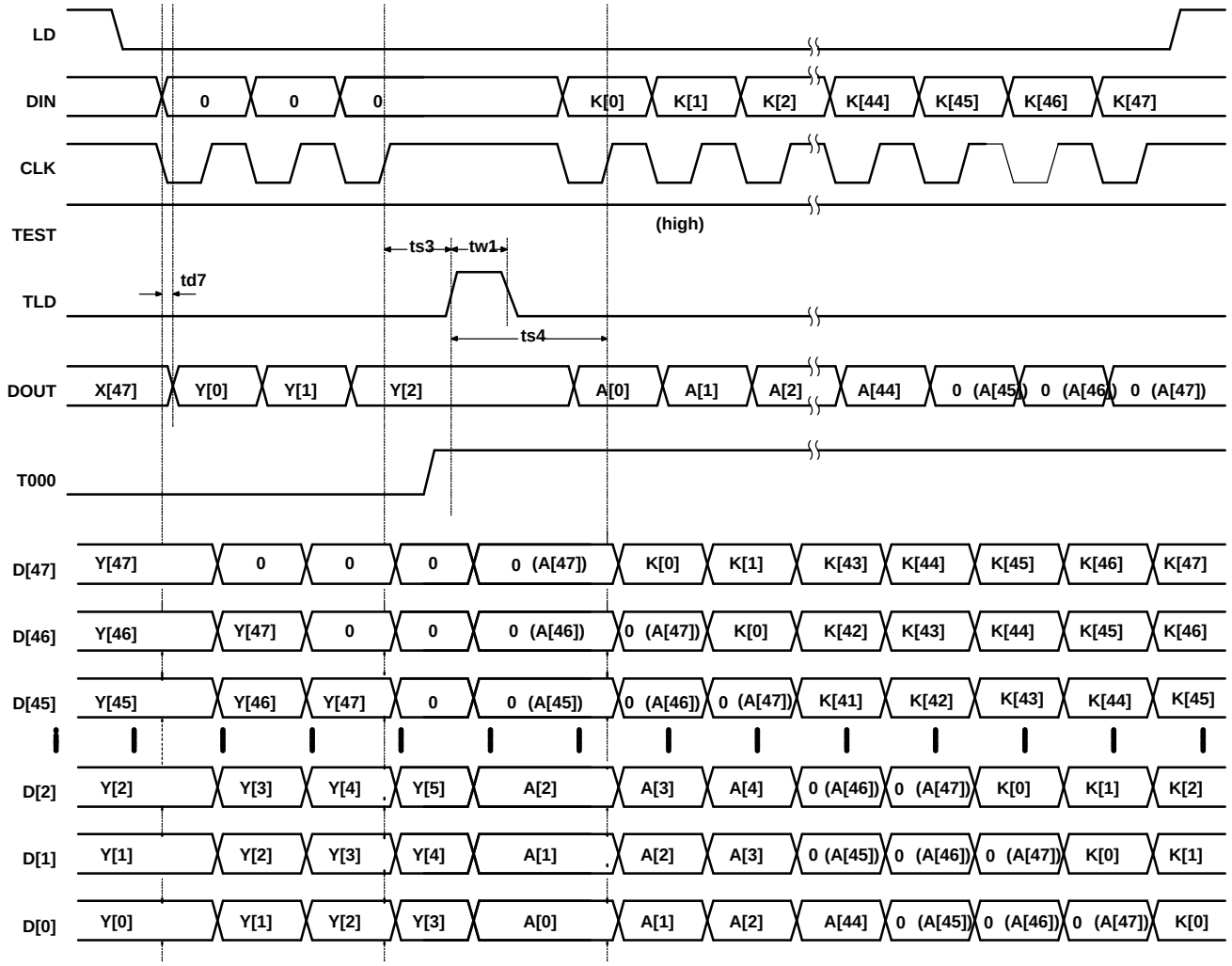


Figure 39. Serial Interface Timing Chart in Test Mode: Information Read

EEPROM Data Input Mode: In Test mode, Tests 1 and 4 have a common function: internally latch the data to be written to an EEPROM in the TPS65520 temporarily. Because their operations are nearly the same, this section describes them together.

Figure 40 and Figure 41 show the shift register configuration from input DIN and output DOUT.

Figure 40. Shift Register Configuration for Test 1

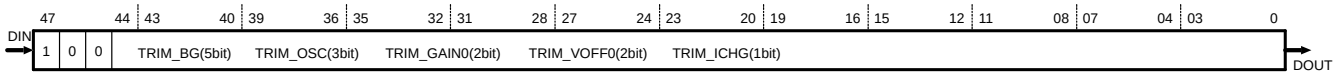


Figure 41. Shift Register Configuration for Test 4

Figure 42 takes Test 1 as an example and shows a single access cycle. As shown in the figure, a TLD input from DIN, following the input of the data to be written to the EEPROM and then *001* (bin) to select Test 1, causes the TPS65520 to internally latch the data to be written temporarily. If data is latched at least once by TLD, any internal blocks that reference values from EEPROM will see the latched data, instead of the data stored in EEPROM, until TEST is driven low.

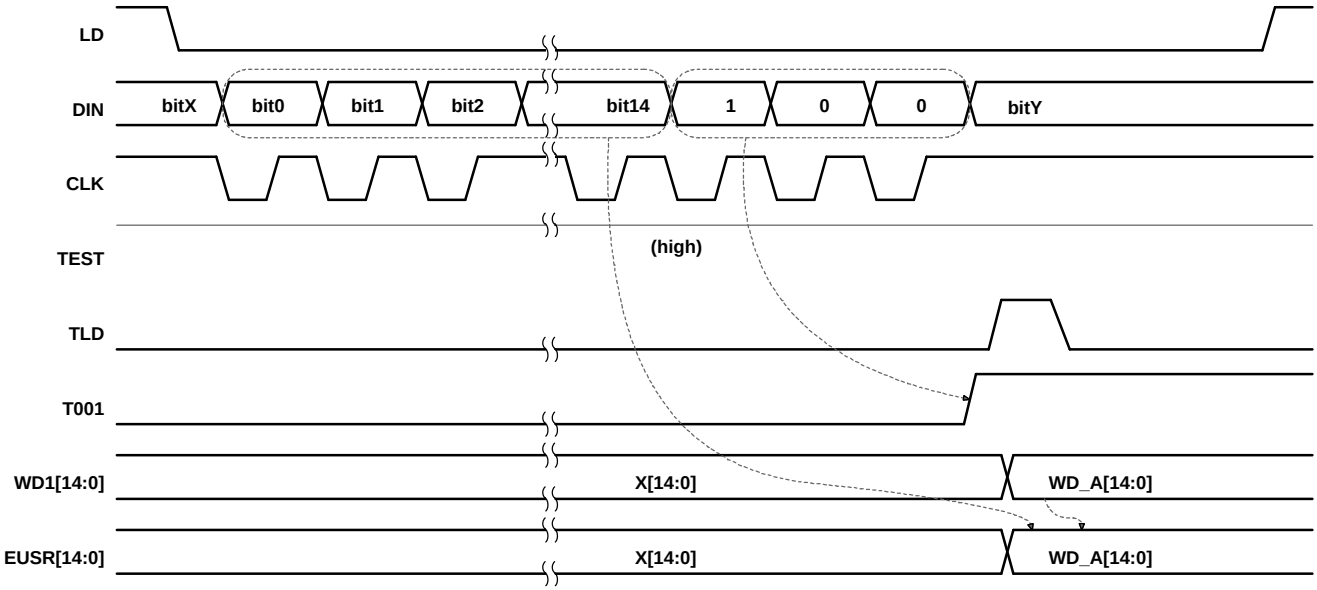


Figure 42. Serial Interface Timing Chart in Test Mode: EEPROM Data Input

EEPROM Data Write Mode: In Test mode, Tests 6 and 7 have a common function: write data to an EEPROM in the TPS65520. Because their operations are nearly the same, this section describes them together.

Figure 43 takes Test 6 as an example and shows a single access cycle. As shown in the figure, the EEPROM write voltage, ROMWR, is applied after the data *110* (bin) is input from DIN to select Test 6. A TLD input following the rise of ROMSW triggers a write to the EEPROM. The duration of the write depends on the TLD pulse width. Once the write is finished, stop applying ROMWR.

For Test 7, write protection is applied to the write timing signal generated using TLD.

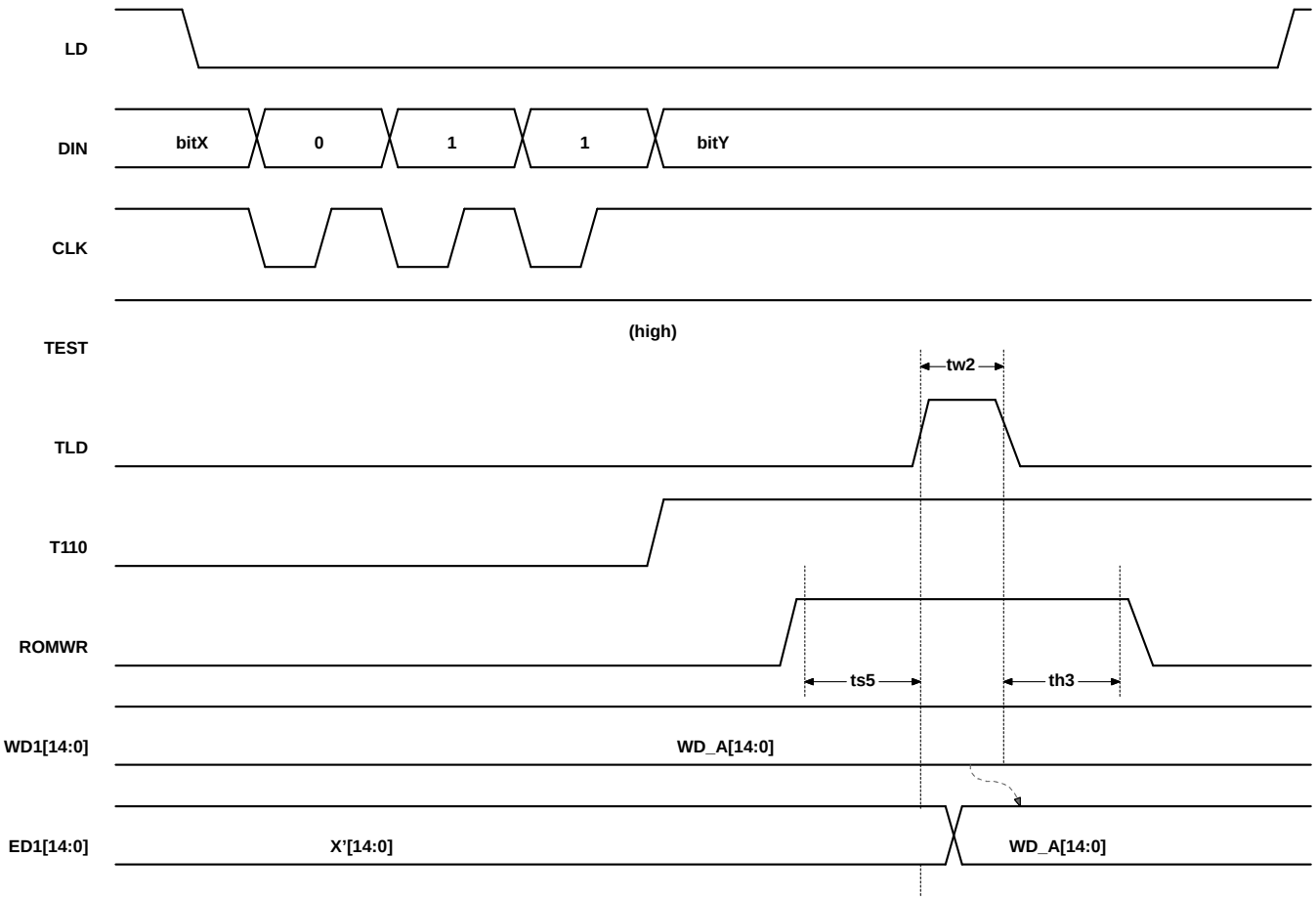


Figure 43. Serial Interface Timing Chart in Test Mode: EEPROM Data Write

Table 5. EVM-XX LIST OF MATERIALS

NAME	VALUE	DEVICE TYPE	EXAMPLE PART NAME
PM71	(CH-7 PMOS)	PMOS	SANYO MCH3306/CPH5802
PM72	(CH-7 Load SW)	PMOS	SANYO MCH3306/CPH5802
NM71	(CH-7 NMOS)	NMOS	SANYO MCH3406/MCH5801
D4	(CH-4)	SBD	SANYO SBS004M
D5	(CH-5)	SBD	SANYO SBS004M
D6	(CH-6)	SBD	SANYO SBS004M
LED6	(CH-6)	White LED	NICHIA NSCW100-T38,NSCW100-T39
ROSC	150 kΩ	Resistor	
RSNS6	22 kΩ	Resistor	
CERR1	0.01 µF	Ceramic capacitor	TDK C0603[B, 6.3V], Murata GRP03[0603, B, 6.3]
CERR2	0.01 µF	Ceramic capacitor	TDK C0603[B, 6.3V], Murata GRP03[0603, B, 6.3]
CERR3	0.022 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
CERR4	0.01 µF	Ceramic capacitor	TDK C0603[B, 6.3V], Murata GRP03[0603, B, 6.3]
CERR5	0.022 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
CERR6	1 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
CERR7	0.1 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
CERR8	0.01 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]

Table 5. EVM-XX LIST OF MATERIALS (continued)

NAME	VALUE	DEVICE TYPE	EXAMPLE PART NAME
CCH1	22 µF	Ceramic capacitor	TDK C3225[B, 6.3V]
CCH2	10 µF	Ceramic capacitor	TDK C2012[B, 6.3V]
CCH3	22 µF	Ceramic capacitor	TDK C3225[22 µF, B, 6.3V]
CCH4	10 µF	Ceramic capacitor	TDK C3225[10 µF, B, 25V]
CCH5	10 µF	Ceramic capacitor	(unknown)[10 µF, B, 10V]
CCH6	10 µF	Ceramic capacitor	TDK C3225[10 µF, B, 25V]
CCH7	22 µF	Ceramic capacitor	TDK C3225[22 µF, B, 6.3V]
CCH8	10 µF	Ceramic capacitor	TDK C2012[B, 6.3V]
CLDO1	4.7 µF	Ceramic capacitor	TDK C2012[B, 6.3V], Murata GRM21[2012, B, 6.3V]
CLDO2	22 µF	Tantalium capacitor	
CLDO3	4.7 µF	Ceramic capacitor	TDK C2012[B, 6.3V], Murata GRM21[2012, B, 6.3V]
CLDO4	10 µF	Ceramic capacitor	TDK C2012[B, 6.3V]
CLDO5	22 µF		
SS_SYNC		Ceramic capacitor	
SS2		Ceramic capacitor	
SS3		Ceramic capacitor	
SS5		Ceramic capacitor	
SS6		Ceramic capacitor	
SSLDO5		Ceramic capacitor	
BOOT11	0.01 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
BOOT12	0.01 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
BOOT2	0.01 µF	Ceramic capacitor	TDK C1005[B, 25V], Murata GRP15[1005, B, 16V]
CSCP		Ceramic capacitor	
CBG	1 µF	Ceramic capacitor	TDK C0603[B, 6.3V], Murata GRP03[0603, B, 6.3]
CREF	0.1 µF	Ceramic capacitor	TDK C0603[B, 6.3V], Murata GRP03[0603, B, 6.3]
L1	10 µH		TDK RLF5018
L2	10 µH		TDK RLF5018
L3	10 µH		Sumida CDRH6D28
L4	4.7 µH		TDK RLF5018
L5	33 µH		DK RLF5018
L6	4.7 µH		TDK RLF5018
L7	10 µH		Sumida CDRH6D28 L8
L8	10 µH		TDK RLF5018

TYPICAL CHARACTERISTICS

CH-1 Efficiency vs Load Current

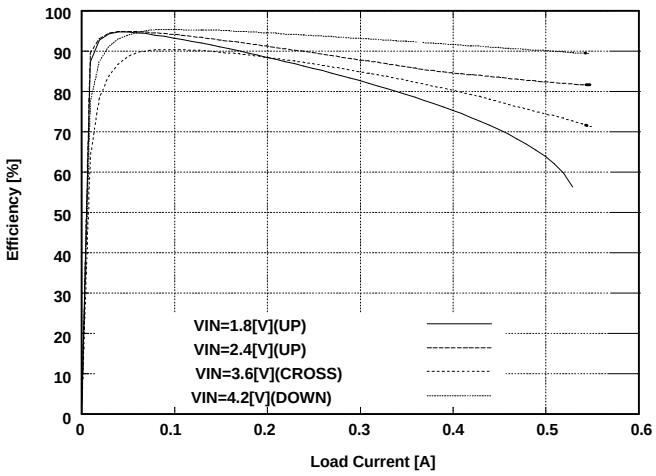


Figure 44.

CH-1 Efficiency vs Input Voltage (Load Current: 200 mA)

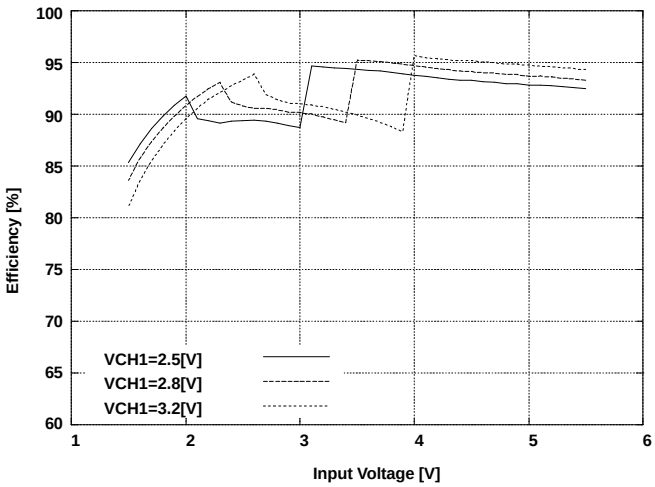


Figure 45.

CH-2 Efficiency vs Load Current

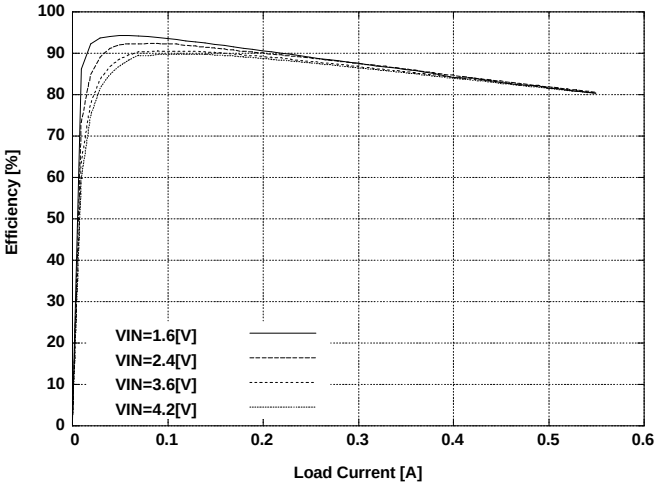


Figure 46.

CH-3 Efficiency vs Load Current

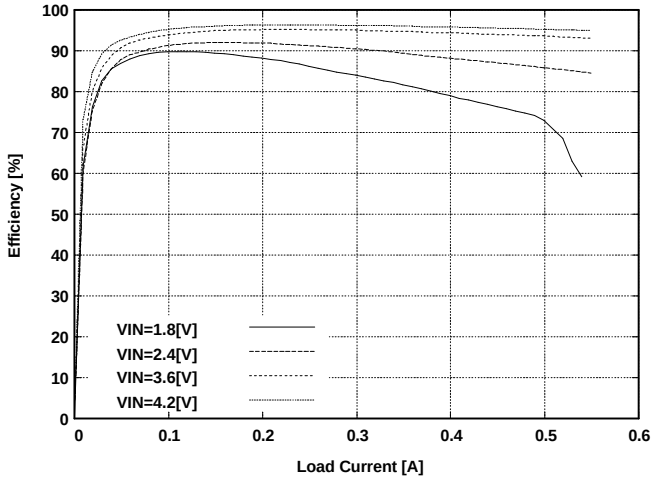


Figure 47.

TYPICAL CHARACTERISTICS (continued)

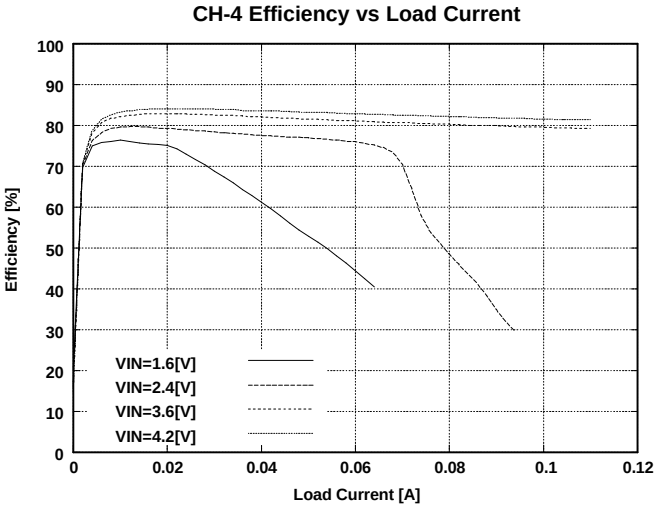


Figure 48.

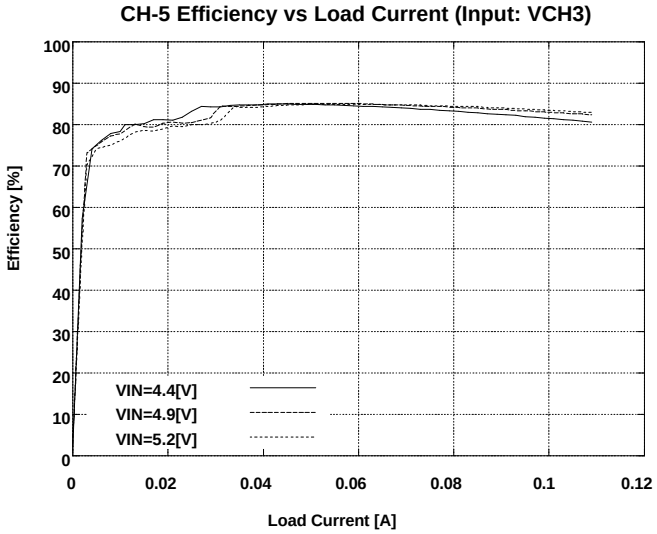


Figure 49.

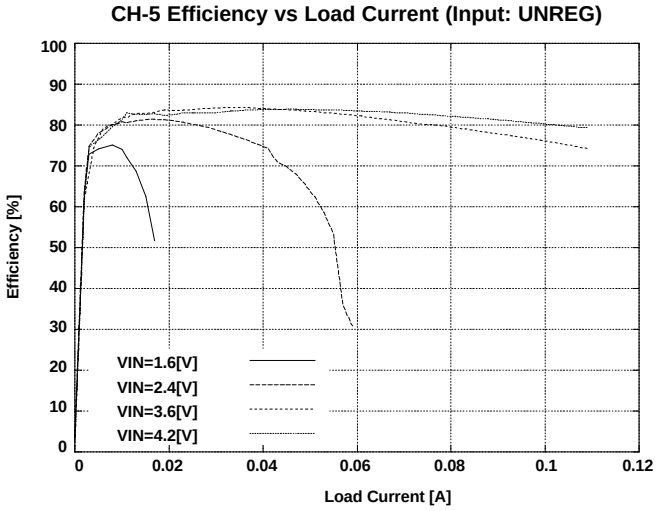


Figure 50.

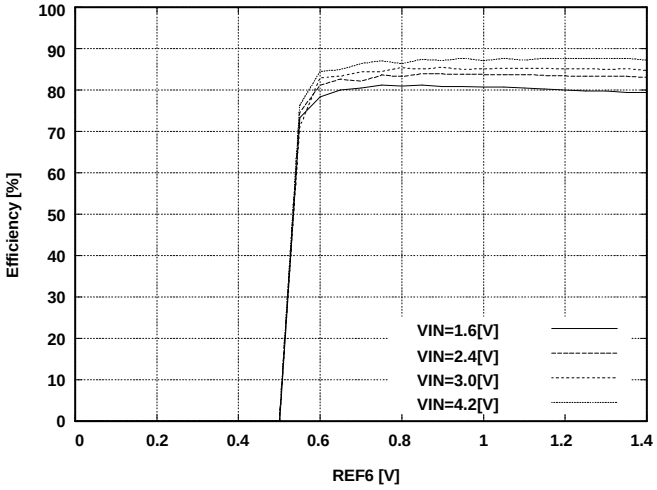


Figure 51.

TYPICAL CHARACTERISTICS (continued)

CH-6 Efficiency vs REF6 (Output: 8 mA, LED4/5 on)

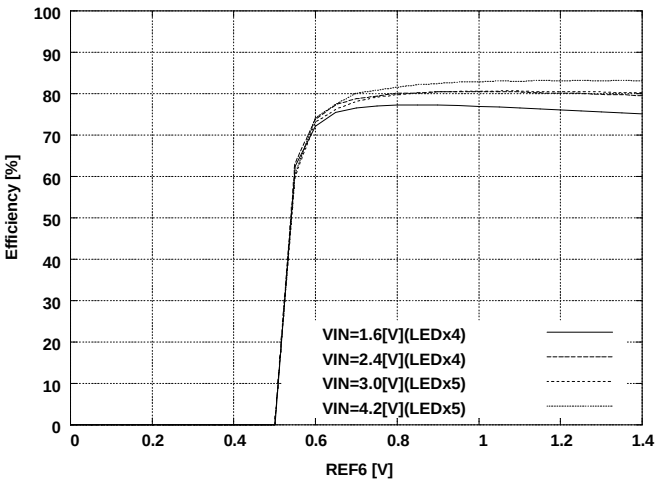


Figure 52.

CH-6 Efficiency vs REF6 (Output: 12 mA, LED2 on)

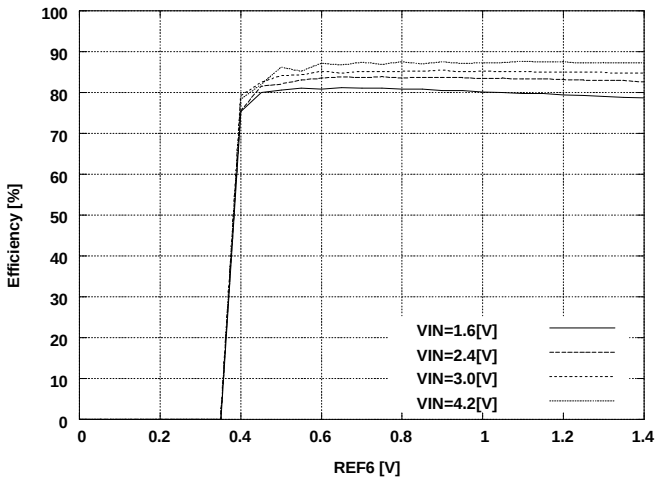


Figure 53.

CH-6 Efficiency vs REF6 (Output: 12 mA, LED4/5 on)

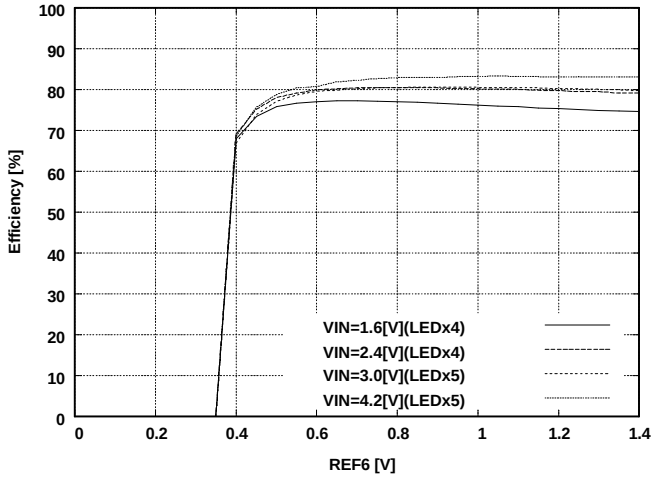


Figure 54.

CH-6 Efficiency vs REF6 (Output: 20 mA, LED2 on)

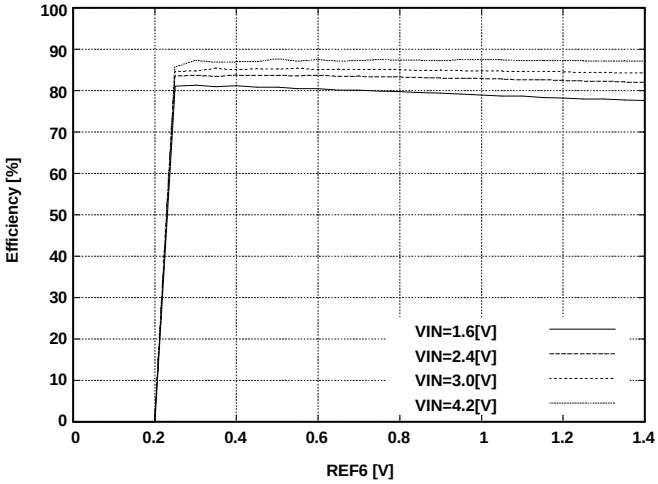


Figure 55.

TYPICAL CHARACTERISTICS (continued)

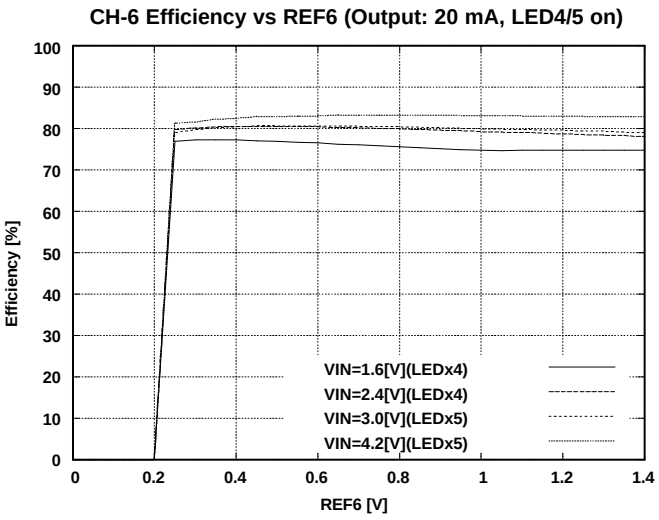


Figure 56.

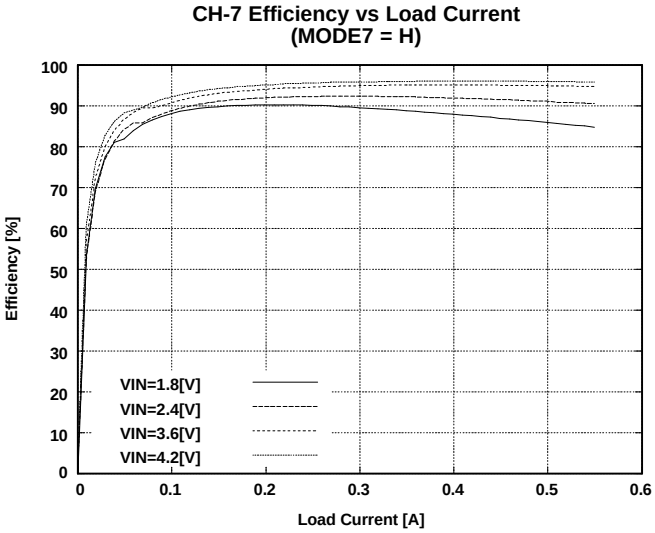


Figure 57.

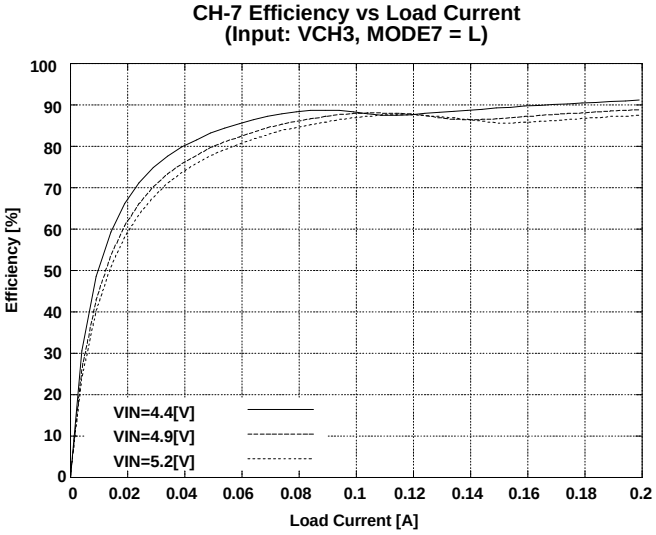


Figure 58.

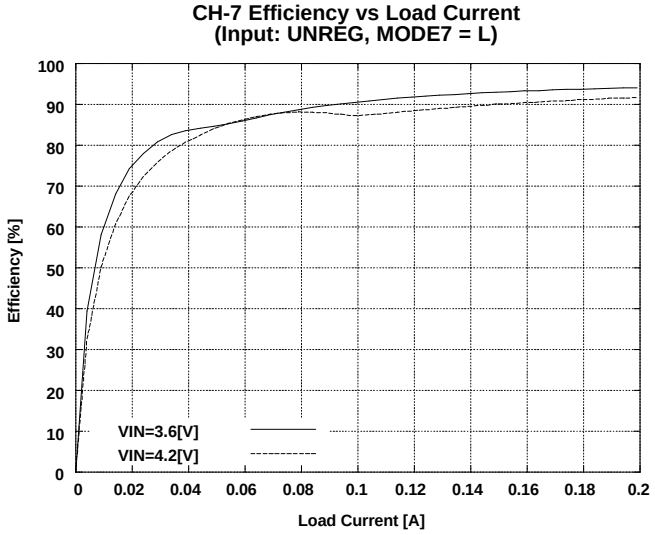


Figure 59.

TYPICAL CHARACTERISTICS (continued)

CH-8 Efficiency vs Load Current (PWM Mode)

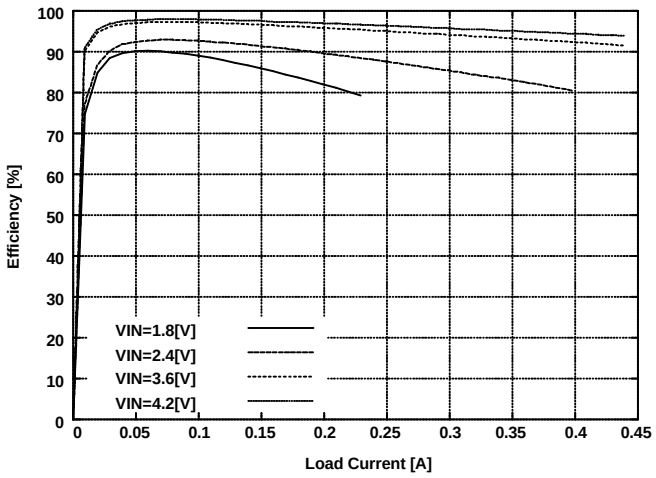


Figure 60.

CH-8 Efficiency vs Load Current (Skip Mode)

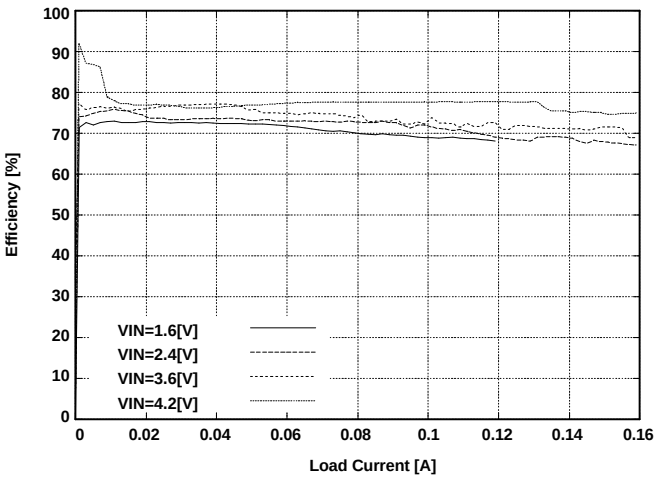


Figure 61.

CH-1 Output Voltage vs Load Current (±2% Axis)

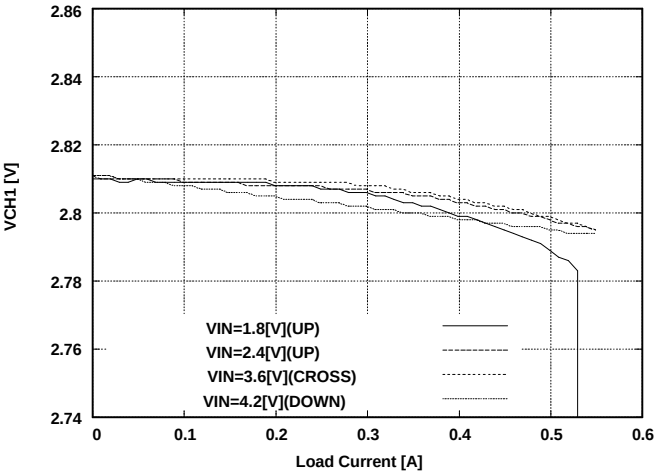


Figure 62.

CH-2 Output Voltage vs Load Current (±2% Axis)

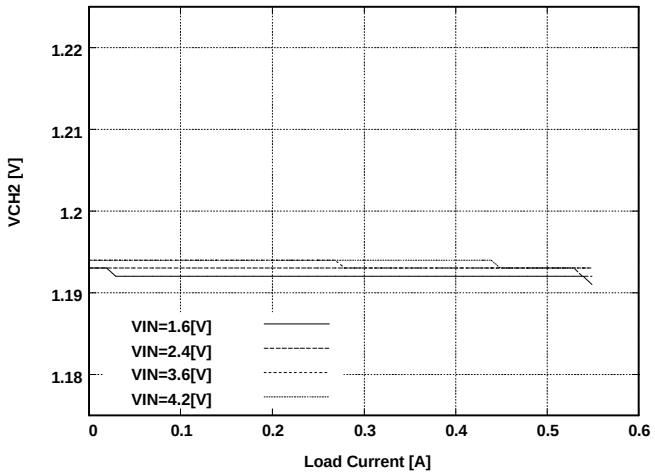


Figure 63.

TYPICAL CHARACTERISTICS (continued)

CH-3 Output Voltage vs Load Current (±2% Axis)

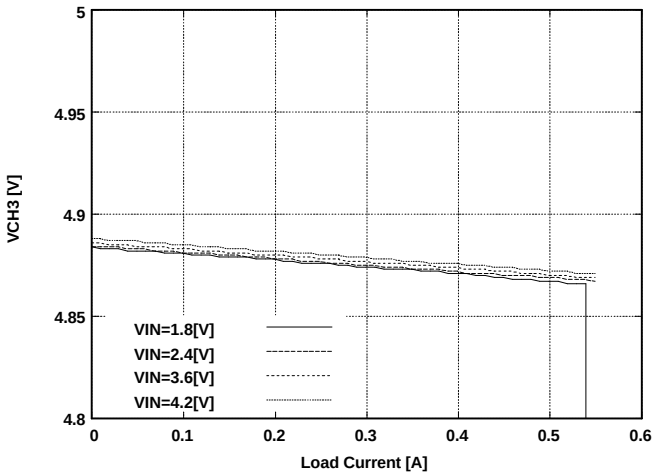


Figure 64.

CH-4 Output Voltage vs Load Current (±2% Axis)

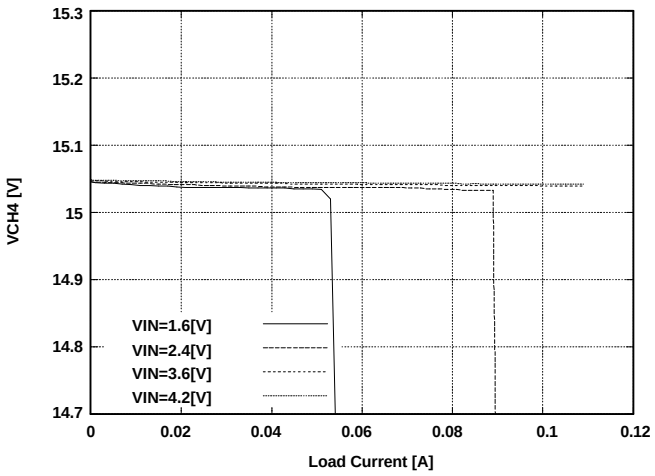


Figure 65.

CH-5 Output Voltage vs Load Current (Input: VCH3, ±2% Axis)

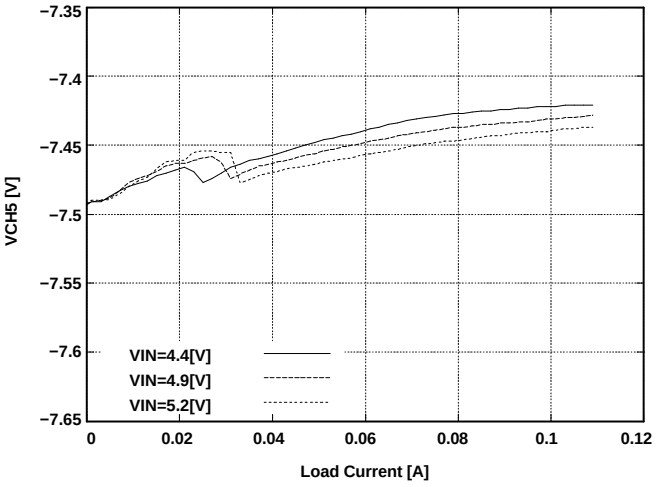


Figure 66.

CH-5 Output Voltage vs Load Current (Input: UNREG, ±2% Axis)

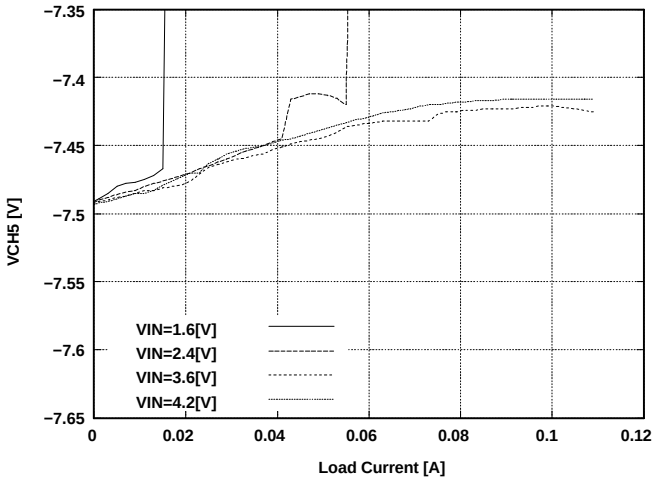


Figure 67.

TYPICAL CHARACTERISTICS (continued)

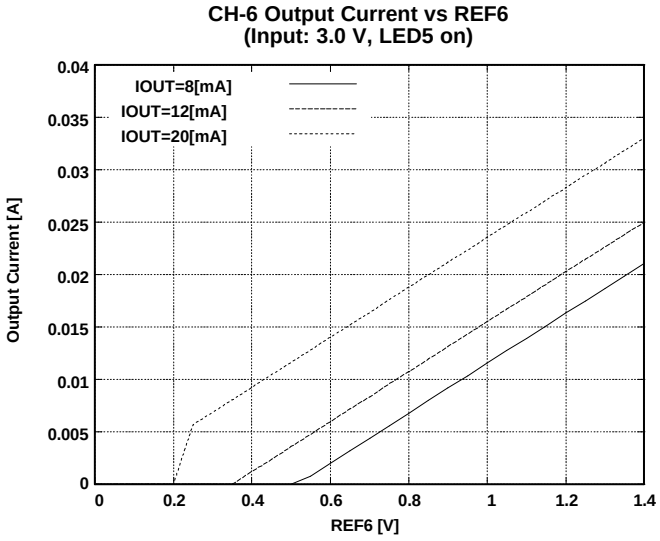


Figure 68.

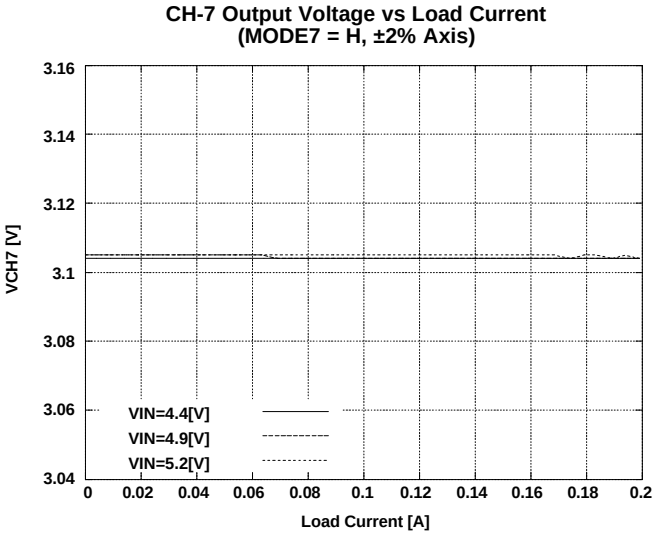


Figure 69.

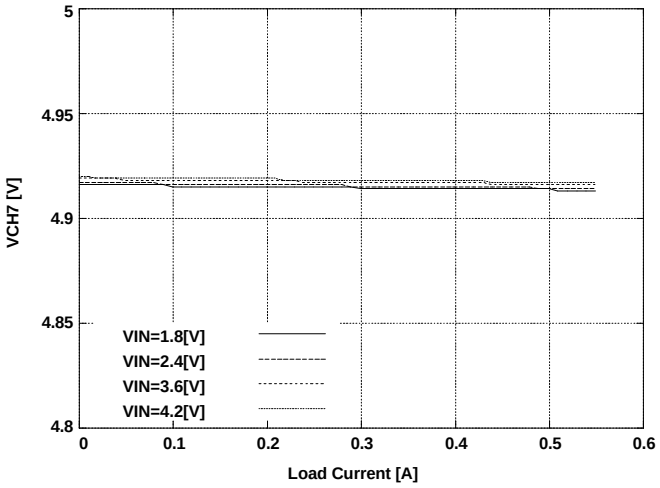


Figure 70.

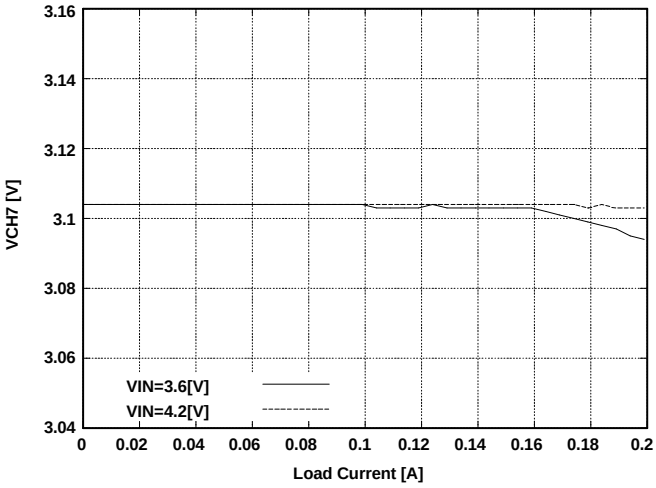


Figure 71.

TYPICAL CHARACTERISTICS (continued)

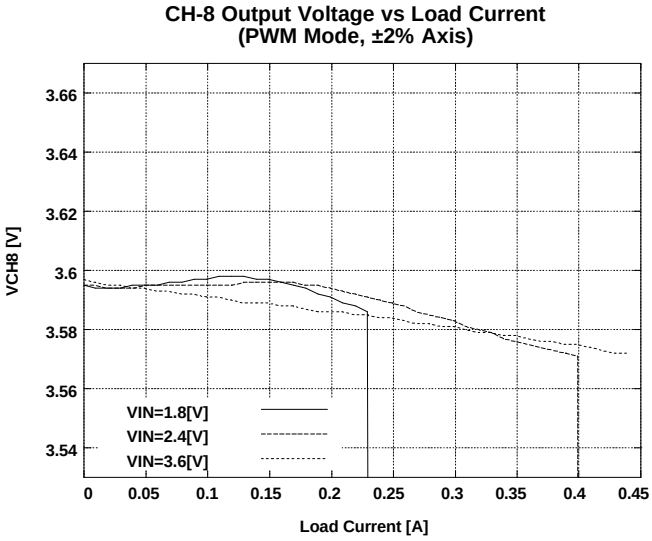


Figure 72.

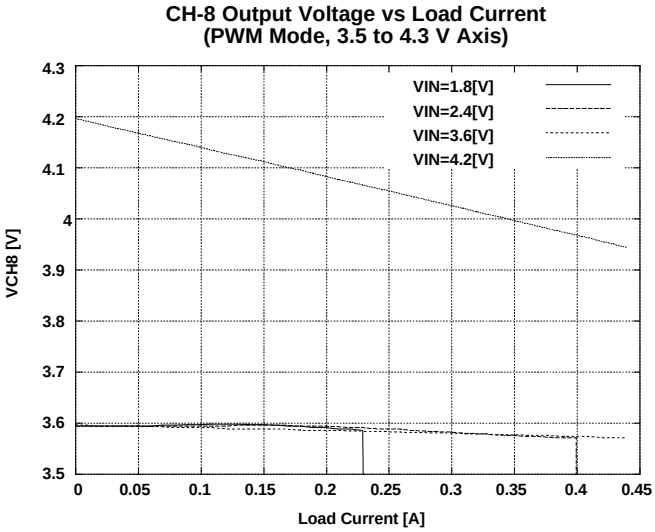


Figure 73.

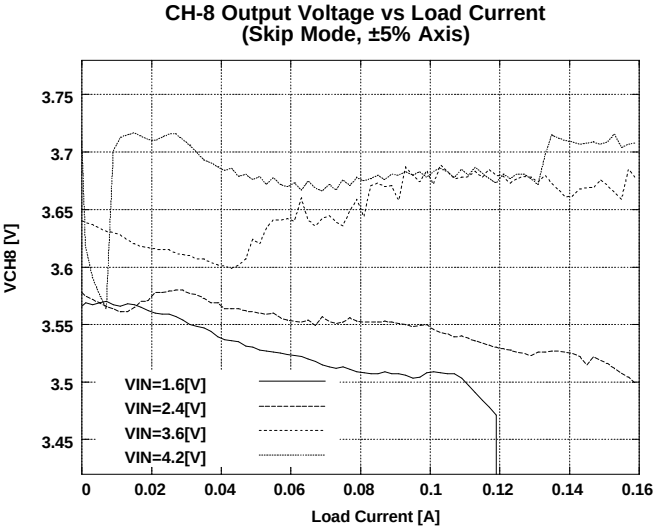


Figure 74.

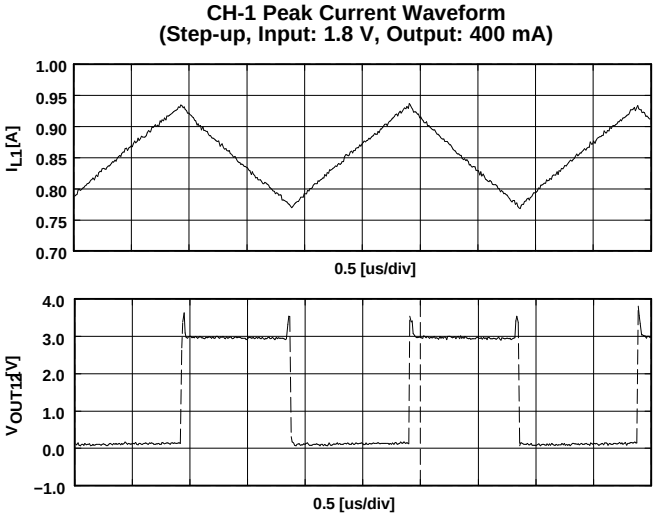


Figure 75.

TYPICAL CHARACTERISTICS (continued)

CH-2 Peak Current Waveform
(Input: 1.8 V, Output: 500 mA)

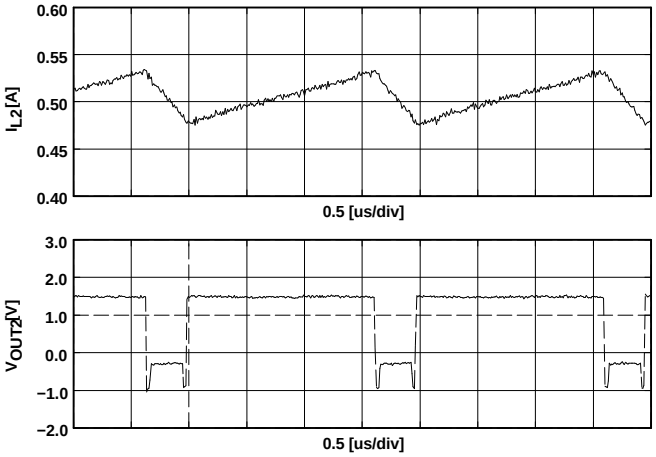


Figure 76.

CH-3 Peak Current Waveform
(Input: 1.8 V, Output: 400 mA)

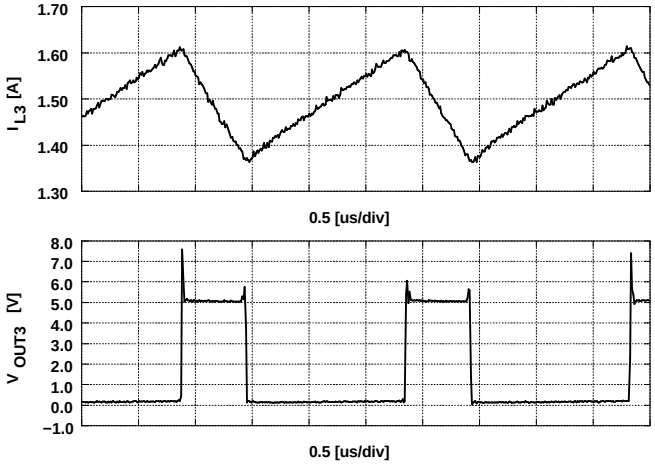


Figure 77.

CH-4 Peak Current Waveform
(Input: 1.8 V, Output: 50 mA)

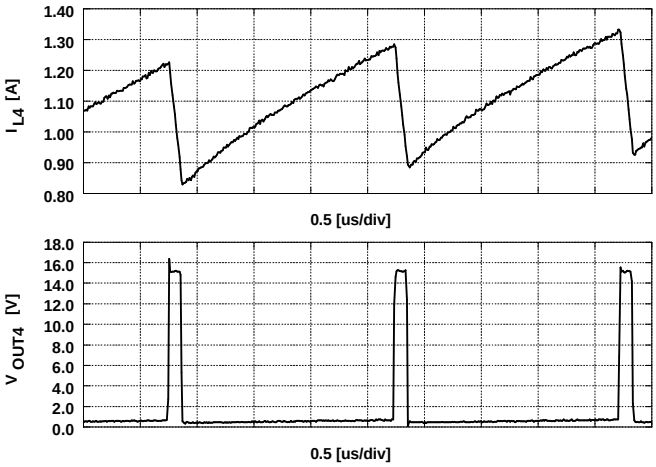


Figure 78.

CH-5 Peak Current Waveform
(Input: VCH3, Output: 50 mA)

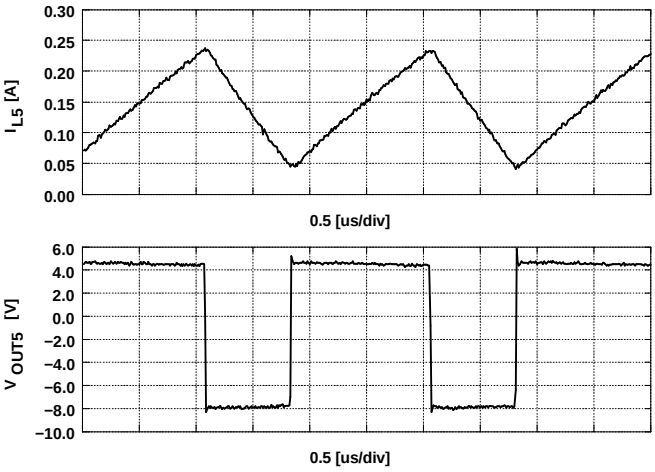


Figure 79.

TYPICAL CHARACTERISTICS (continued)

CH-6 Peak Current Waveform
(Input: 1.8 V, Output: 20 mA)

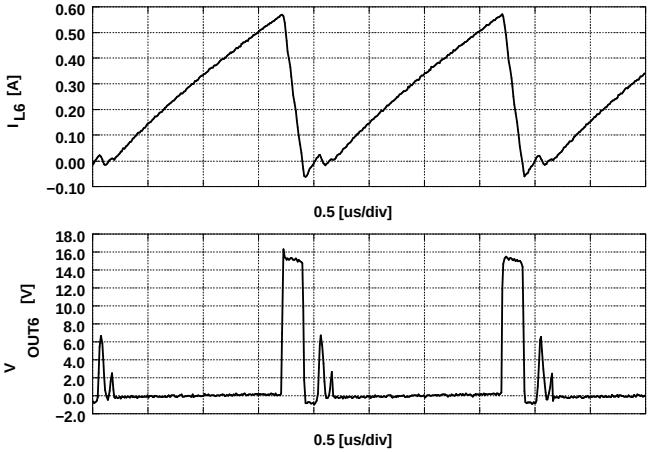


Figure 80.

CH-7 Peak Current Waveform
(MODE7 = H, Input: 1.8 V, Output: 500 mA)

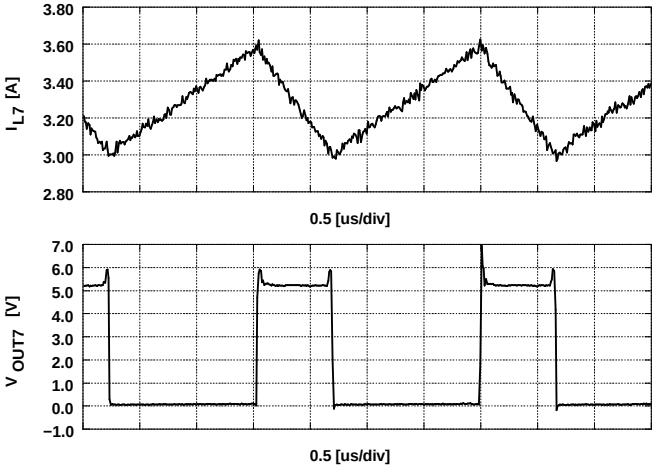


Figure 81.

CH-7 Peak Current Waveform
(MODE7 = L, Input: VCH3, Output: 150 mA)

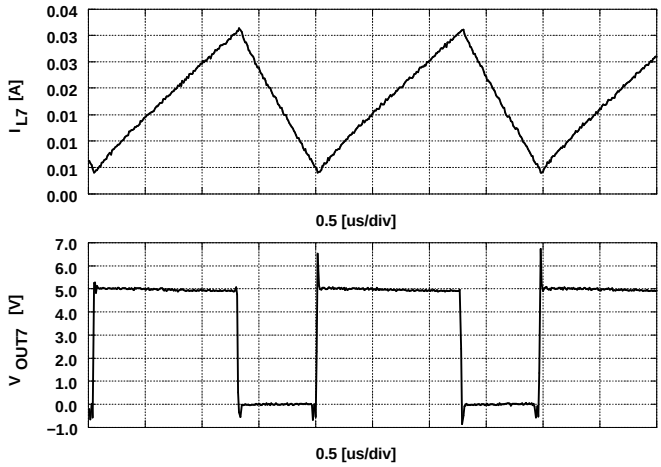


Figure 82.

CH-8 Peak Current Waveform
(Input: 1.8 V, Output: 200 mA)

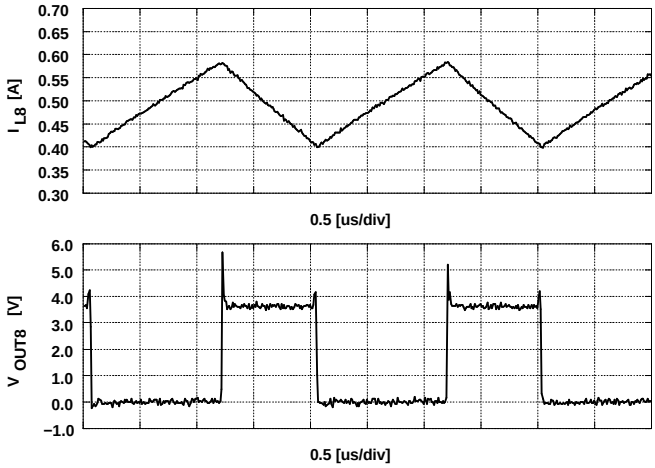


Figure 83.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65520ZVDR	ACTIVE	BGA	ZVD	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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