

INTEGRATED PHOTO FLASH CHARGER AND IGBT DRIVER

FEATURES

- **Highly Integrated Solution to Reduce Components**
- **Integrated 50-V Power Switch, $R_{(ON)} = 200\text{ m}\Omega$ Typical**
- **Integrated IGBT Driver**
- **High Efficiency**
- **Programmable Peak Current, 0.95 A ~ 1.8 A**
- **Input Voltage of 1.8 V to 12 V**
- **Optimized Control Loop for Fast Charge Time**
- **Sensing All Trigger From Primary Side**
- **10-Pin MSOP/16-Pin QFN Package**
- **Protection**
 - MAX On Time
 - Over V_{DS} Shutdown
 - Thermal Monitor

APPLICATIONS

- **Digital Still Cameras (DSC)**
- **Optical Film Cameras**
- **Mobile Phones With Camera**
- **PDA's With Camera**

DESCRIPTION

This device offers a complete solution for charging a photo flash capacitor from battery input, and subsequently discharging the capacitor to the xenon tube. The device has an integrated power switch, IGBT driver, and control logic blocks for charge applications. Compared with discrete solutions, the device significantly reduces the component count, shrinks the solution size, and eases design complexity. Additional advantages are fast charging time and high efficiency due to the optimized PWM control algorithm.

Other provisions of the device includes four options for determining a different target voltage, programmable peak current, thermal disable monitor, input signal for charge enable, flash enable, and an output signal for charge completion status.

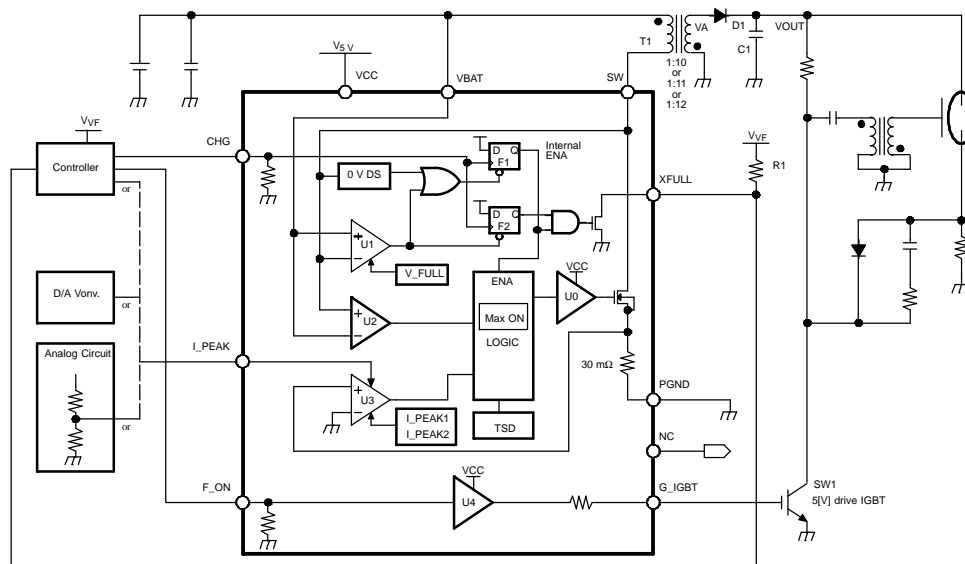


Figure 1. Typical Application Circuit⁽¹⁾

(1) TI assumes no responsibility for the consequences of use of this application circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

TPS65552A

SLVS567–JULY 2005



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	TARGET VOLTAGE at PRIMARY SIDE	PACKAGE MARKING	PACKAGE	PART NUMBER
-35°C to 85°C	29	BKV	16-pin QFN	TPS65552ARGT
-35°C to 85°C	29	BMA	10-pin MSOP	TPS65552ADGQ

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			UNIT
V_{SS}	Supply voltage	VCC	-0.6 V to 6 V
		VBAT	-0.6 V to 13 V
$V_{(SW)}$	Switch terminal voltage		-0.6 V to 50 V
	Switch current between SW and PGND, ISW		3 A
V_I	Input voltage of CHG, I_PEAK, F_ON		-0.3 V to V_{CC}
T_{stg}	Storage temperature		-40°C to 150°C
T_J	Maximum junction temperature		125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, VCC	4.5		5.5	V
	Supply voltage, VBAT	1.8		12	V
$V_{(SW)}$	Switch terminal voltage,	-0.3		45	V
	Switch current between SW and PGND			2	A
	Operating free-air temperature range	-35		85	°C
V_{IH}	High-level digital input voltage at CHG and F_ON	2.4			V
V_{IL}	Low-level digital input voltage at CHG and F_ON			0.6	V

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$ ⁽¹⁾	POWER RATING $T_A < 25^\circ\text{C}$	POWER RATING $T_A = 70^\circ\text{C}$	POWER RATING $T_A = 85^\circ\text{C}$
MSOP	49.08 °C/W	2.04 W	1.12 W	815 mW
QFN	47.40 °C/W	2.11 W	1.16 W	844 mW

(1) The thermal resistance, $R_{\theta JA}$, is based on a soldered PowerPAD™ on a 2S2P JEDEC board using thermal vias.

ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$, $V_{BAT} = 4.2\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{(SW)} = 4.2\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$R_{(ONL)}$	ON resistance of XFULL		1.5	3	$k\Omega$		
$V_{(PKH)}^{(1)}$	Upper threshold voltage of I_PEAK	2.4			V		
$V_{(PKL)}^{(1)}$	Lower threshold voltage of I_PEAK			0.6	V		
I_{CC1}	Supply current from VBAT	CHG = H, $V_{(SW)} = 0\text{ V}$ (free run by t_{MAX})		27	μA		
I_{CC2}	Supply current from VCC	CHG = H, $V_{(SW)} = 0\text{ V}$ (free run by t_{MAX})		2.5	5	mA	
I_{CC3}	Supply current from VCC and VBAT	CHG = L		1	μA		
I_{lk1}	Leakage current of SW terminal			2	μA		
I_{lk2}	Leakage current of XFULL terminal	$V_{(XFULL)} = 5\text{ V}$		1	μA		
$R_{(ONSW)}$	SW ON resistance between SW and PGND	$I_{(SW)} = 1\text{ A}$		0.3	1	Ω	
$R_{(IGBT1)}$	G_IGBT pullup resistance	$V_{(G_IGBT)} = 0\text{ V}$		5	10	15	Ω
$R_{(IGBT2)}$	G_IGBT pulldown resistance	$V_{(G_IGBT)} = 5\text{ V}$		25	51	75	Ω
$I_{(PEAK1)}$	Upper peak of $I_{(SW)}$	$V_{(L_IPEAK)} = 3\text{ V}$		1.58	1.68	1.78	A
$I_{(PEAK2)}$	Lower peak of $I_{(SW)}$	$V_{(L_IPEAK)} = 0\text{ V}$		0.77	0.87	0.97	A
$V_{(FULL)}$	Charge completion detect voltage at $V_{(SW)}$	TPS65552A		28.7	29	29.3	V
$V_{(ZERO)}$	Zero current detection at $V_{(SW)}$	1	20	60	mV		
$T_{(SD)}^{(1)}$	Thermal shutdown temperature	150	160	170	$^\circ\text{C}$		
	Over V_{DS} detection at $V_{(SW)}$	0.95	1.2	1.45	V		
t_{MAX}	MAX ON time	50	80	120	μs		
$R_{(INPD)}$	Pulldown resistance of CHG, F_ON	$V_{CHG} = V_{(F_ON)} = 4.2\text{ V}$		100	$k\Omega$		

(1) Specified by design.

SWITCHING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$, $V_{BAT} = 4.2\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{(SW)} = 4.2\text{ V}$ (unless otherwise noted)

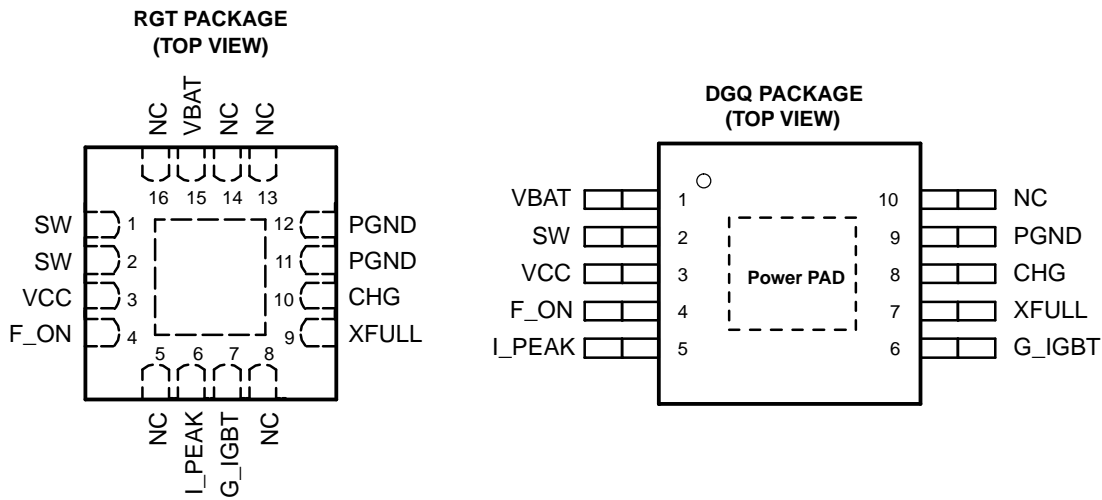
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}^{(1)}$	F_ON \uparrow - G_IGBT \downarrow		50		ns
	SW ON after $V_{(SW)}$ dips from $V_{(ZERO)}$		45		ns
	SW OFF after $I_{(SW)}$ exceeds $I_{(PEAK)}$		270		ns
	XFULL \downarrow after $V_{(SW)}$ exceeds $V_{(FULL)}$		300		ns
	SW ON after CHG \uparrow		20		ns
	SW OFF after CHG \downarrow		20		ns

(1) Specified by design.

TPS65552A

SLVS567–JULY 2005

PIN ASSIGNMENT



NC – No internal connection

TERMINAL FUNCTIONS

PIN NUMBER		SIGNAL	I/O	DESCRIPTION
RGT	DGQ			
1, 2	2	SW	O	Primary side switch
3	3	VCC	I	Power supply voltage
4	4	F_ON	I	G_IGBT control input
5, 8, 13, 16	–	NC		No connection (internally open)
6	5	I_PEAK	I	Peak current control input
7	6	G_IGBT	O	IGBT gate driver output
9	7	XFULL	O	Charge completion output
10	8	CHG	I	Charge control input
11, 12	9	PGND		Power ground
14	10	NC		No connection (used by TI, should be open pin)
15	1	VBAT	I	Battery voltage input

PRODUCT PREVIEW

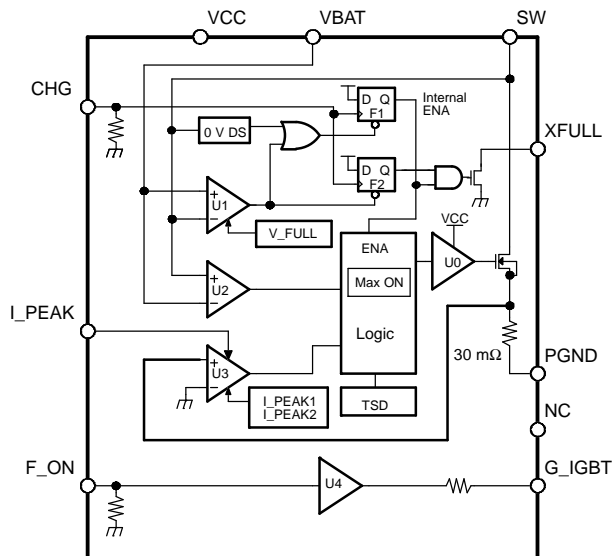


Figure 2. Functional Block Diagram

I/O Equivalent Circuits

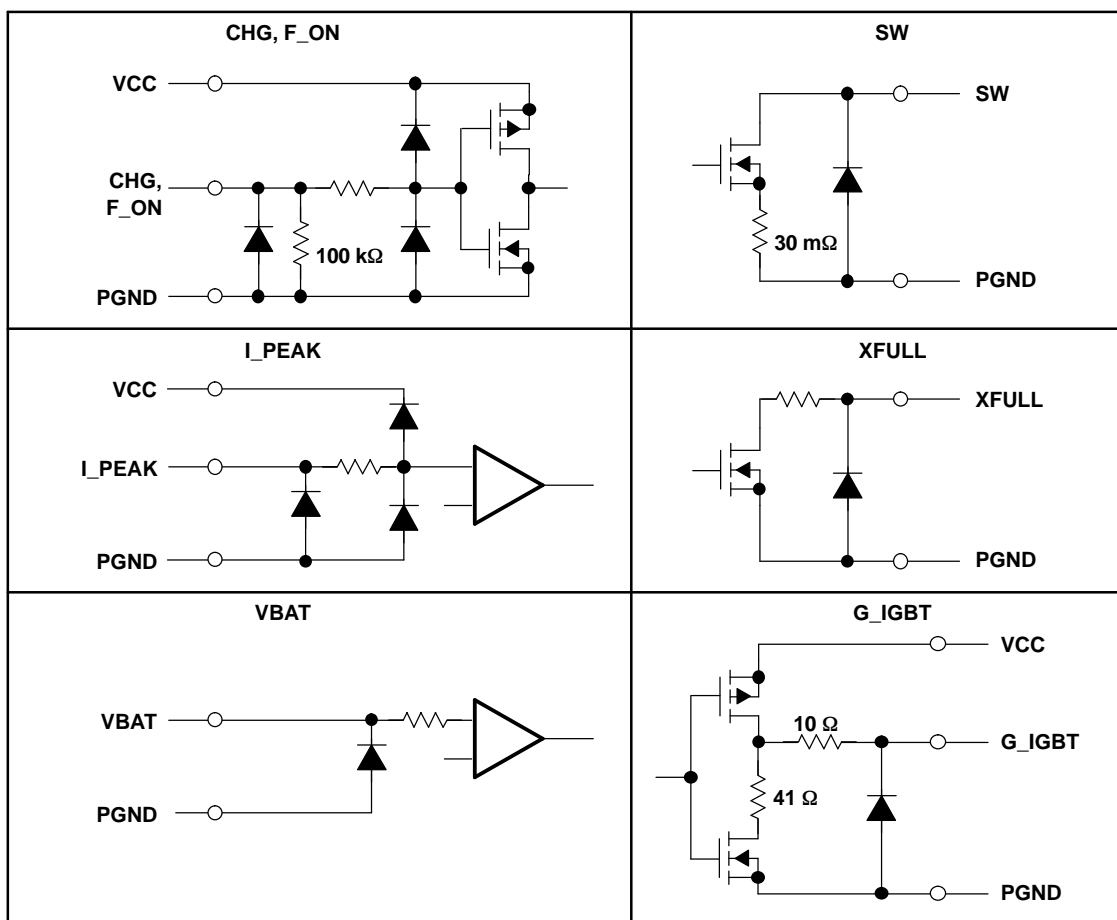
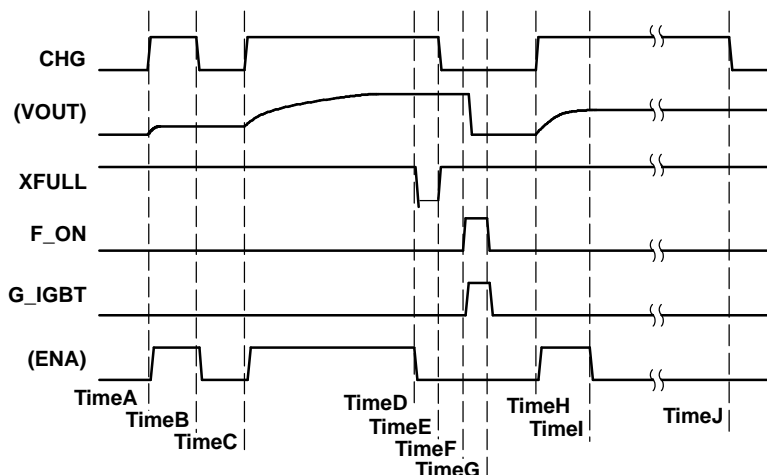


Figure 3. I/O Equivalent Circuits

PRODUCT PREVIEW

TPS65552A

SLVS567–JULY 2005

PRINCIPLES OF OPERATION**Figure 4. Whole Operation Sequence Chart****Start/Stop Charging**

TPS65552A has one internal enable latch, F1, that holds a charge (*ON/OFF* status) of the device. See [Figure 2](#).

The only way to *start* charging is to input $\text{CHG}\uparrow$ (see time A/C/H in [Figure 4](#)). Each time $\text{CHG}\uparrow$ is reached, the TPS65552A starts charging.

There are three trigger events to *stop* charging:

1. Forced *stop* by inputting $\text{CHG} = \text{L}$ from the controller (see timeB in [Figure 4](#)).
2. Automatic *stop* by detecting full charge. VOUT reaches the target value (see TimeD in [Figure 4](#)).
3. Protected *stop* by over V_{DS} detection (see TimeI in [Figure 4](#)).

Indicate Charging Status

When the charging operation is completed, the TPS65552A drives the charge completion indicator pin, XFULL, to GND. XFULL is an open-drain type output. When connecting the indicator LED to XFULL, the LED lights are on when fully charged. The controller detects the status of the device as a logic signal when connecting a pullup resistor, R1 (see [Figure 1](#)).

XFULL enables the controller to detect the over V_{DS} protection status using software time. If over V_{DS} protection occurs, XFULL never goes L during $\text{CHG} = \text{H}$, provided that the timer that starts at $\text{CHG}\uparrow$ stops at $\text{XFULL}\uparrow$, and times out within a designed period of maximum charging times. The controller can detect over V_{DS} at time out.

The device starts charging at *timeH*, and over V_{DS} protection occurs at TimeI (see [Figure 4](#)). At timeI, XFULL stays H, and the controller detects over V_{DS} protection when the timer ends at timeJ. In this event, the controller inputs $\text{CHG} = \text{L}$ to terminate the operation.

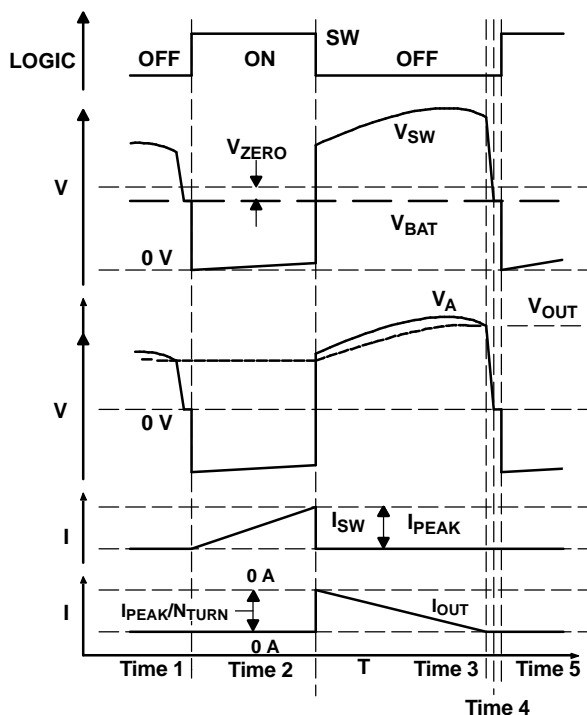


Figure 5. Timing Diagram at One Switching Cycle

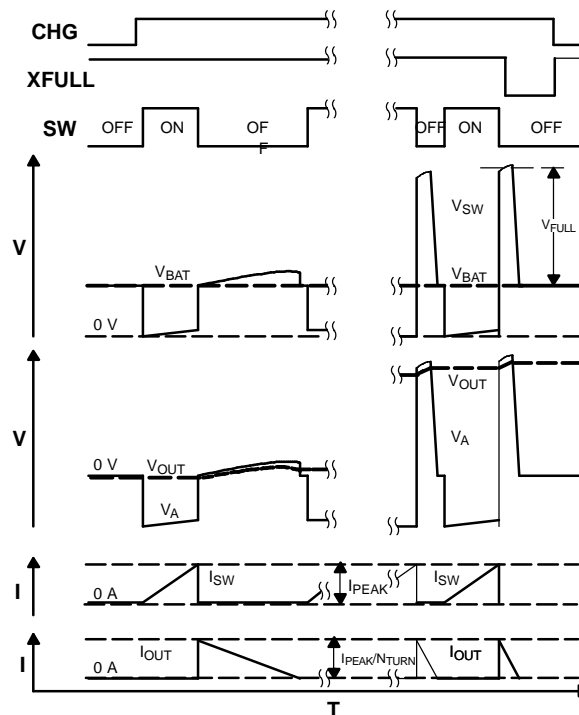


Figure 6. Timing Diagram at Beginning/Ending

Control Charging

The TPS65552A provides three comparators to control charging. Figure 2 shows the block diagram of TPS65552A and Figure 5 shows one timing diagram switching cycle. Note that emphasis is placed on Time1 and Time3 of the waveform in Figure 5.

While SW is ON (Time1 to Time2 in Figure 5), U3 monitors current flow through integrated power-MOSFET from SW to PGND. When $I_{(SW)}$ exceeds $I_{(PEAK)}$, SW turns OFF (Time2 in Figure 5).

When SW turns OFF (Time2 in Figure 5), the magnetic energy in the transformer starts discharging. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of V_{OUT} (Time2 to Time3 in Figure 5). When almost all energy is discharged, the system cannot continue rectification via the diode, and the charging current of I_{OUT} goes to zero (Times3 in Figure 5). After rectification stops, the small amount of energy left in the transformer is released via the parasitic path, and the kickback voltage reaches zero (Time3 to Time4 in Figure 5). During this period, U2 makes SW turn ON when $(V_{(SW)} - V_{BAT})$ dips from $V_{(ZERO)}$ (Time5 in Figure 5). In the actual circuit, the period between Time4 and Time5 in Figure 5 is small or does not appear dependent on the delay time of the U2 detection to SW ON.

U1 also monitors the kickback voltage. When $(V_{(SW)} - V_{BAT})$ exceeds $V_{(FULL)}$, TPS65552A stops charging (see Figure 6).

In Figure 5 and Figure 6, ON time is always the same period in every switching. The ON time is calculated by Equation 1. This equation is not dependent on output voltage.

$$t_{ON} = L \frac{I_{PEAK}}{V_{BAT}} \quad (1)$$

However, OFF time is dependant on output voltage. As the output voltage gets higher, the OFF time gets shorter (see Equation 2).

TPS65552A

SLVS567–JULY 2005

$$t_{\text{OFF}} = N_{\text{TURN}} \times L \frac{I_{\text{PEAK}}}{V_{\text{OUT}}} \quad (2)$$

Reference Voltage

The TPS65552A does not have its own reference voltage circuit inside, and the TPS65552A uses the VCC input voltage as a reference to detect $I_{(\text{PEAK})}$, $V_{(\text{ZERO})}$, and $V_{(\text{FULL})}$. Therefore, voltage input at VCC is approximately 5 V.

VCC differs from 5 V by system limitations. [Table 1](#) shows the dependence of each function of TPS65552A to VCC.

Table 1. VCC Dependence of TPS65552A

PARAMETER		EQUATION	VCC		
			4.5	5	5.5
$I_{(\text{PEAK}1)}$		$0.52 \times VCC - 0.92$	1.42	1.68	1.94
$I_{(\text{PEAK}2)}$		$0.24 \times VCC - 0.33$	0.75	0.87	0.99
$V_{(\text{FULL})}$	TPS65552A	$5.8 \times VCC$	26.1	29.0	31.9
	over V_{DS}	$0.24 \times VCC$	1.08	1.2	1.32

Termination Voltage Setting

To obtain a different termination voltage, transformers of different turn ratio are required. [Table 2](#) shows the matrix of termination voltage and the turn ratio of the transformer. The table only shows a *ONE to integer* ratio while there are no limitations for a turn ratio of the transformer in a real application circuit, example 1:10.5 (= 10:105).

Table 2. Termination Voltage Setting Table

	TPS65552A
	29 [V]
1:10	290
1:11	319
1:12	348

Programming Peak Current

The TPS65552A provides a method to program $I_{(PEAK)}$ through the input voltage of the I_PEAK terminal. Figure 7 shows how to program $I_{(PEAK)}$.

I_PEAK input is treated as a logic input, when its voltage is below $V_{(PKL)}$ (0.6 V) and above $V_{(PKH)}$ (2.4 V). Between $V_{(PKL)}$ and $V_{(PKH)}$, I_PEAK input is treated as an analog input. Using this characteristic, $I_{(PEAK)}$ can be set by the logic signal or by an analog input.

Typical usages of this function are:

1. Charging $I_{(PEAK)}$ depends on the battery voltage. Large $I_{(PEAK)}$ for an adequate battery, small $I_{(PEAK)}$ for a poor battery.
2. Reducing $I_{(PEAK)}$ when zooming lens (motor works); this avoids shutdown of the battery with a large current output.

In Figure 1, three optional connections to I_PEAK are shown.

1. Use the controller to treat I_PEAK as the logic input pin. This option is the easiest.
2. Use a D/A converter to force $I_{(PEAK)}$ to follow analog information, such as battery voltage.
3. Use an analog circuit to achieve the same results as the D/A converter.

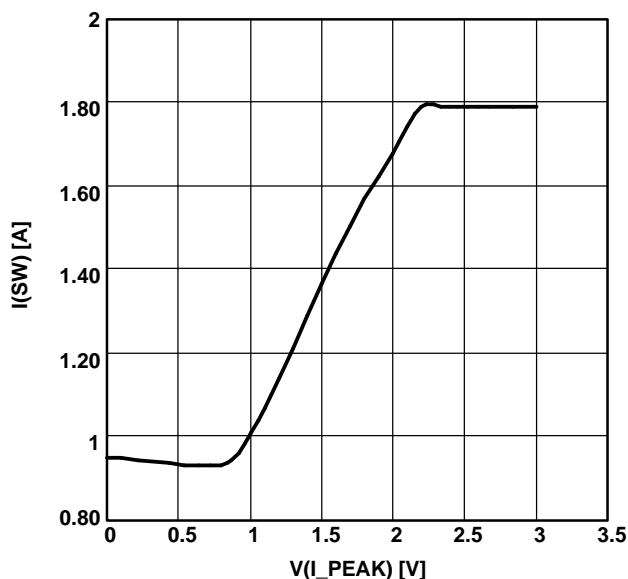


Figure 7. I_PEAK vs $I_{(SW)}$

IGBT Driver Control

The IGBT driver provided by the TPS65552A is a simple buffer in the logical table. Table 3 shows the function (see Figure 4).

Table 3. IGBT Driver Function Table

F_ON	G_IGBT
L	L
H	H

TPS65552A

SLVS567–JULY 2005

Protections

TPS65552A provides three protections: thermal shutdown, max on time, and overvoltage at power SW.

Thermal Shutdown

When TPS65552A overheats, all functions stop. The only way to recover is to wait for the TPS65552A to cool down. This protection is not through *SHUTDOWN*, so the TPS65552A restarts charging if CHG stays H during the whole overheated period.

MAX ON Time

To prevent a condition such as pulling current from a poor power source (i.e., an almost empty battery), the TPS65552A provides a maximum *ON* time protection. If the *ON* time exceeds t_{MAX} , the TPS555x is forced *OFF* regardless of $I_{(PEAK)}$ detection.

Overvoltage at Power SW

To avoid the stress of power dissipation, the TPS65552A provides an overvoltage monitor function at the SW terminal. If this protection occurs, the overvoltage status is latched (see Figure 4 and its descriptions).

This function also protects short-circuit of the secondary side. In the short-circuit state of the secondary side, almost 100% of the battery voltage is supplied to SW, which stresses the device.

PCB Information

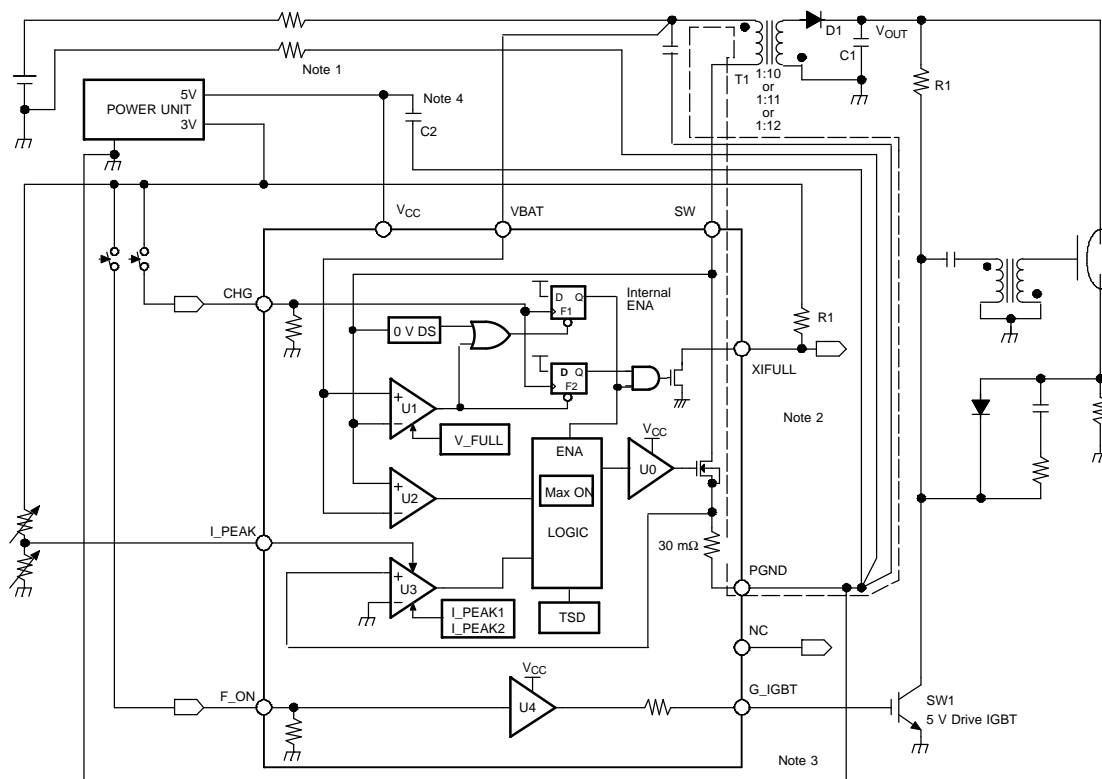


Figure 8. PCB Design Guideline⁽¹⁾

(1) TI assumes no responsibility for the consequences of use of this application circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

PRODUCT PREVIEW

Figure 8 shows key points when designing a PCB.

1. In many DSC designs, parasitic resistance that cannot be ignored, exists on the power line path from the battery to the primary side turn of the transformer. The TPS65552A has one ground point connection inside the IC at the PGND PAD. So, the PCB layout should also keep a one-point ground connection at the PGND terminal of TPS65552A.
2. The loop indicated by dotted-lines is laid out as small as possible to reduce the open area of the loop.
3. The TPS65552A uses the VCC input as a reference voltage. Considering Note 1, the ground of the *power unit* that sources VCC is connected to PGND.
4. Regarding Note 3, the bypass capacitor, C2, is required to avoid grounding noise.

Additional Technical Information

TI provides an application note for this device. For more technical information, please find the application note on the TI Web site or consult your sales contact. Literature number [SLVA197](#).

The application note provides the following information.

1. Recommended external parts
2. PCB layout
3. Detailed operation theory
4. Calculation of the efficiency
5. Key points to design your system

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65552ADGQ	NRND	MSOP- PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-250C-1 YEAR	-35 to 85	BMA	
TPS65552ADGQG4	NRND	MSOP- PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-250C-1 YEAR	-35 to 85	BMA	
TPS65552ADGQR	NRND	MSOP- PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-250C-1 YEAR	-35 to 85	BMA	
TPS65552ADGQRG4	NRND	MSOP- PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-250C-1 YEAR	-35 to 85	BMA	
TPS65552ARGTR	NRND	QFN	RGT	16		Pb-Free (RoHS)	CU SN	Level-2-250C-1 YEAR	-35 to 85	BKV	
TPS65552ARGTRE3	NRND	QFN	RGT	16		Pb-Free (RoHS)	CU SN	Level-2-250C-1 YEAR	-35 to 85	BKV	
TPS65552ARGTT	NRND	QFN	RGT	16		TBD	Call TI	Call TI	-35 to 85	BKV	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

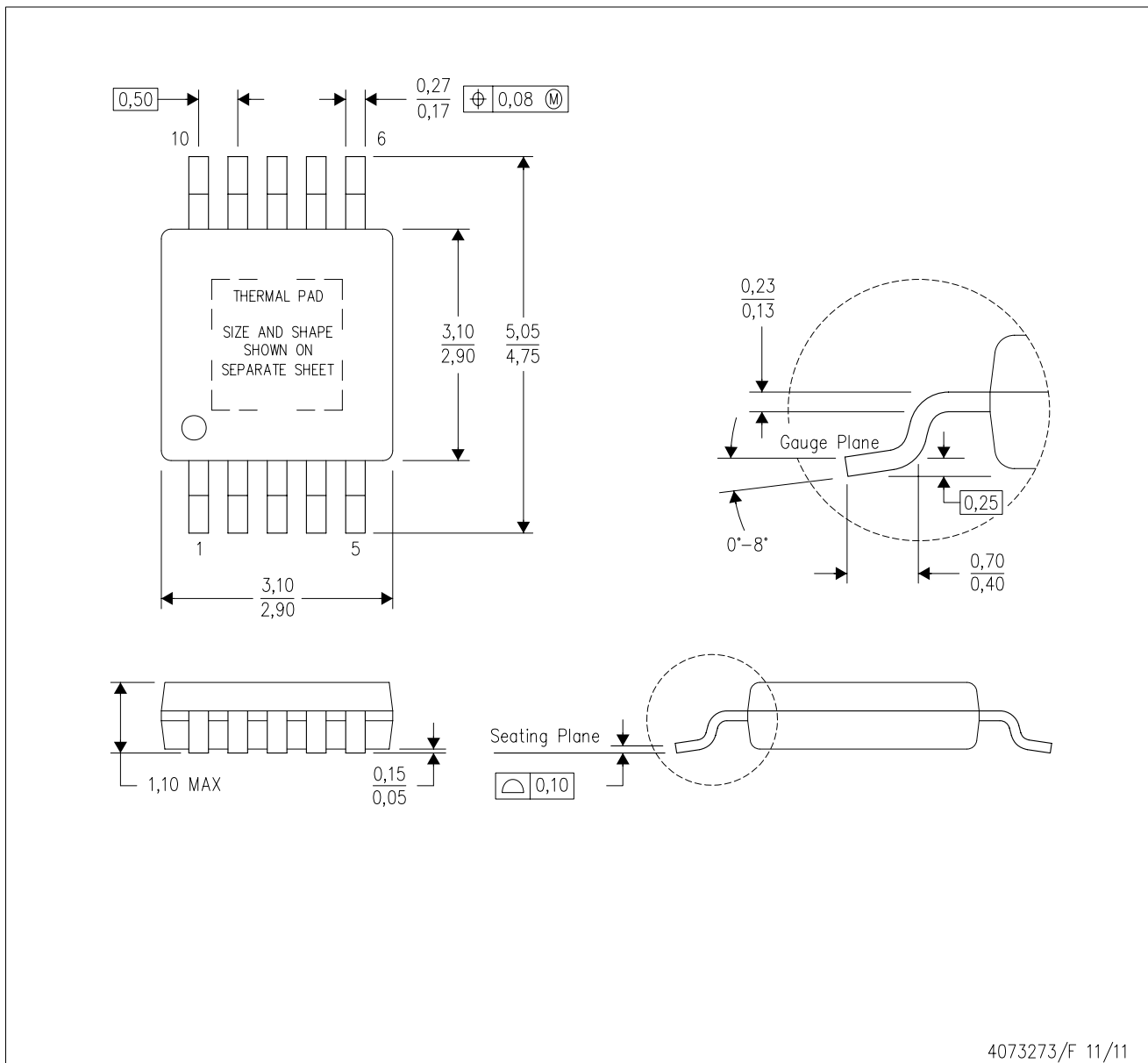
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

DGQ (S-PDSO-G10)

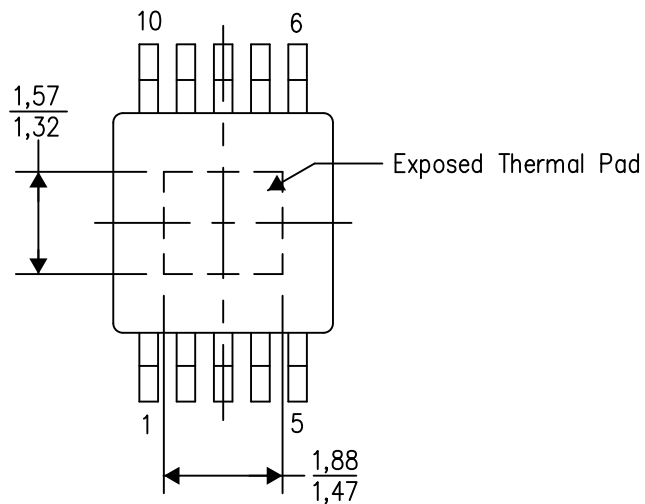
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



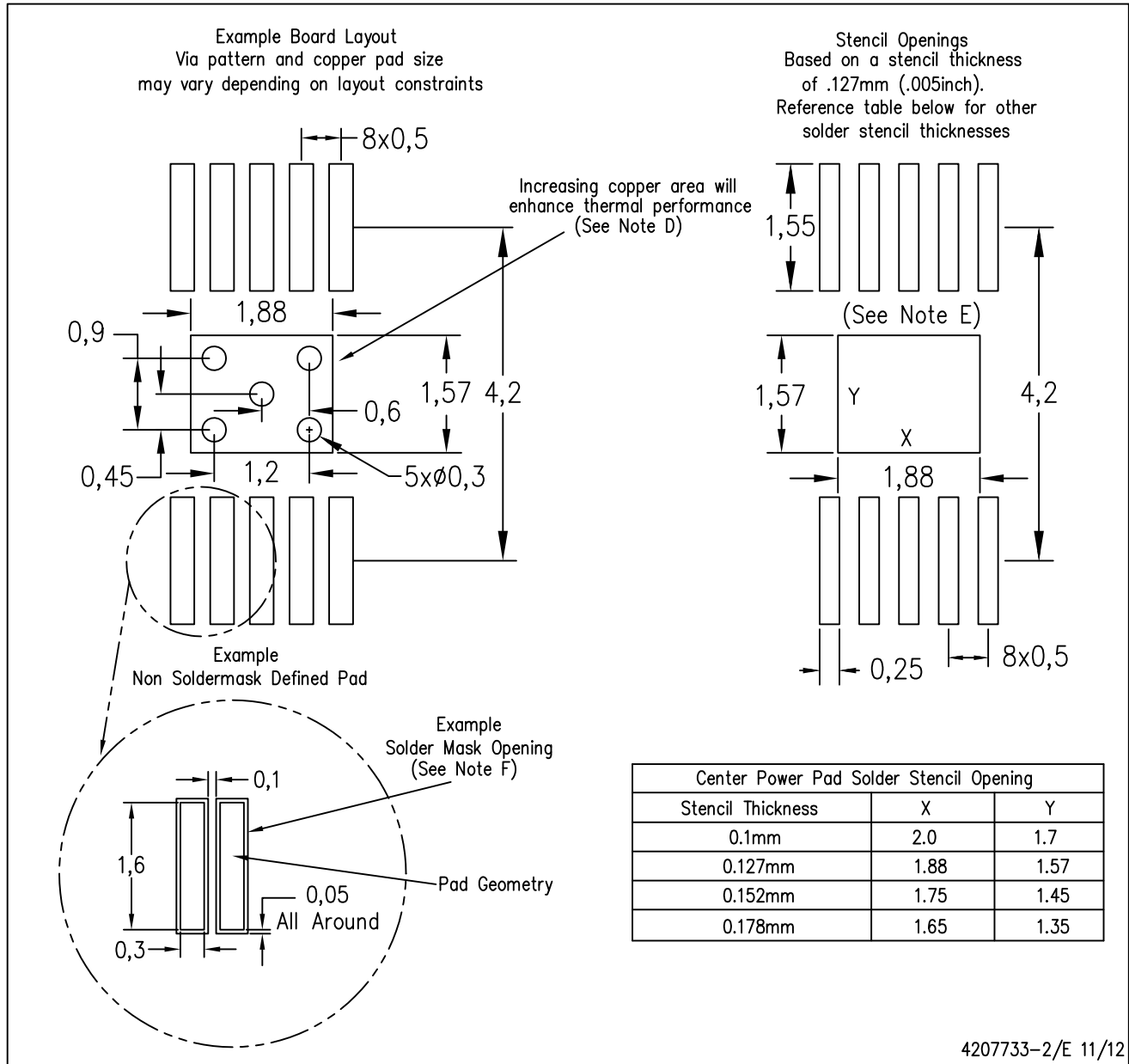
Top View

Exposed Thermal Pad Dimensions

4206324-2/G 05/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

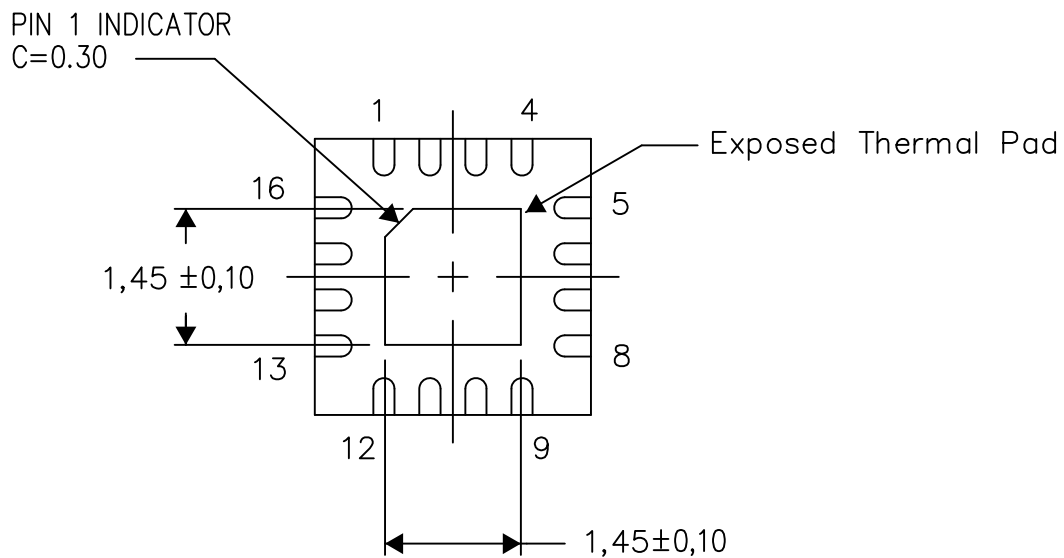
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

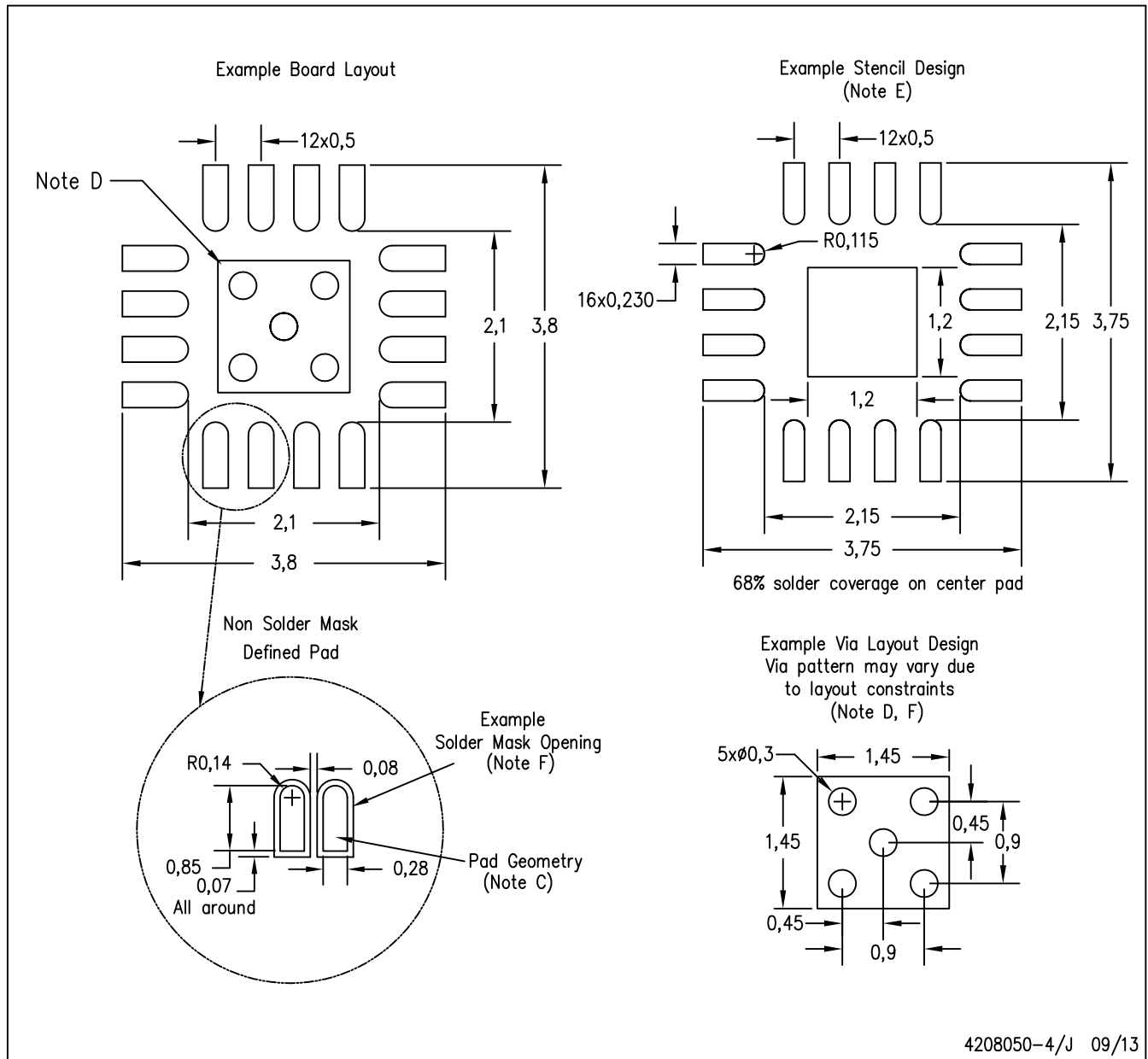
Exposed Thermal Pad Dimensions

4206349-2/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com