75-V High-Side Ideal Diode/OR-ing MOSFET Controller

Features

- Wide Input Voltage Range
  - Normal Operation: 5 V to 75 V
  - Maximum: 100 V Transient
- External N-channel MOSFET Driver
  - Charge Pump with Integrated Capacitor
  - Gate Driver for External N-Channel MOSFET
  - 20-mV V_{SD} for Regulated Conduction Mode
  - −10-mV V_{SD} for Reverse Current Blocking
  - 1.9-A Sink Current to Turn-off NMOS
  - Dedicate OFF Pin for MOSFET Test Function
- Fast Reverse Current Blocking: 25 ns typical
- SOT23-6 Package

Applications

- Industry Control, Factory Automation
- Server, Network, and Enterprise Power Supply
- Active OR-ing for Redundant Power Supplies

Description

The TPS75R01A is an ideal diode controller that operates with an external N-channel MOSFET for reverse protection applications or redundant power supply applications. The forward voltage drop is controlled at as low as 20 mV, which can significantly reduce power loss to replace an ordinary Schottky Diode in power distribution networks.

The TPS75R01A supports a wide operating voltage range from 5 V to 75 V, with an absolute maximum rating of 100 V. The support for a transient 100-V input voltage is particularly suitable to meet the severe requirement in 48-V power supply systems.

The TPS75R01A integrates a charge pump to drive the external N-channel MOSFET. The device provides precise gate control to regulate the voltage drop between the source and drain at 20 mV. When it detects a reverse voltage of −10 mV from IN to OUT, the TPS75R01A turns off the external MOSFET within 25 ns typical to ensure no reverse current flows. The TPS75R01A also features a MOSFET test mode. It allows the MCU controller to test the shorted MOSFET.

The TPS75R01A provides a small SOT23-6 package, and it is qualified to operate within the junction temperature range from −40°C to +125°C.

Typical Application Circuit

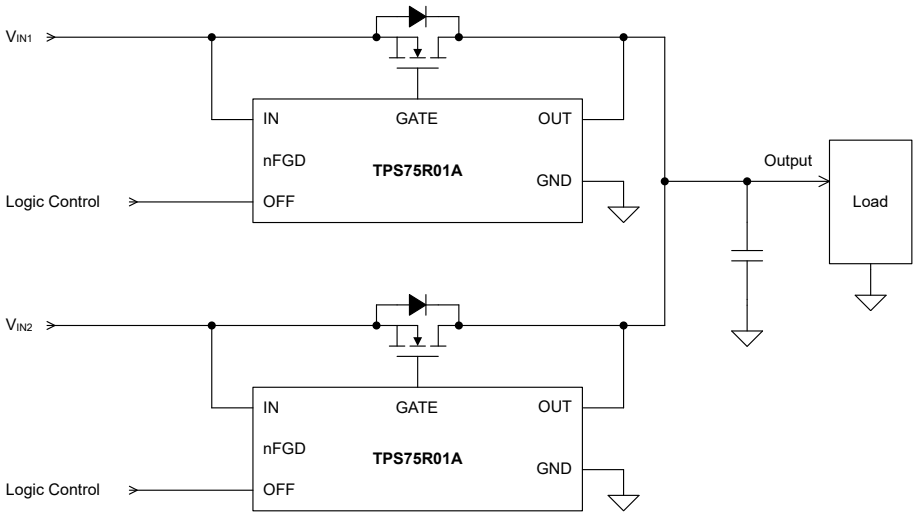


Table of Contents

Product Family Table

Order Number	Voltage Range (V)	Regulated Forward Voltage (mV)	Reverse Protection Threshold (mV)	Package
TPS75R01A-S6TR-S	5 to 75	20	–10	SOT23-6

Revision History

Date	Revision	Notes
2024-06-15	Rev.Pre.0	Preliminary datasheet.
2025-03-11	Rev.Pre.1	Updated the Electrical Characteristics table. Update Layout example.
2025-04-11	Rev.A.0	Initial release.

Pin Configuration and Functions

TPS75R01A
SOT23-6 Package
Top View

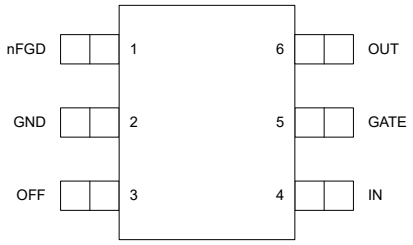


Table 1. Pin Functions: TPS75R01A

Pin No.	Pin Name	I/O	Description
5	GATE	O	Gate drive output pin. Connect this pin to the gate of the external N-channel MOSFET.
2	GND	-	Ground reference pin.
4	IN	I	Input supply voltage sense pin. Connect this pin to the source of the external N-channel MOSFET.
1	nFGD	O	External MOSFET test open-drain output pin. Combined with the OFF pin to achieve the MOSFET test function. When the OFF pin is logic high, an active low output of nFGD indicates the forward voltage from source to drain of the MOSFET is greater than 350 mV, and the MOSFET is not shorted. Left this pin open when the MOSFET test function is not used. Pull up this pin to a voltage below 5.5 V through an external resistor for the MOSFET test function.
3	OFF	I	External MOSFET test control pin. When the OFF pin is logic low or left open, the MOSFET test function is disabled. When the OFF pin is logic high, the GATE pin is pulled down and MOSFET is turned off, and the MOSFET test function is enabled.
6	OUT	I	Output voltage sense pin. Connect this pin to the drain of the external N-channel MOSFET.

Specifications

Absolute Maximum Ratings (1) (2) (3)

Parameter		Min	Max	Unit
IN, OUT		−0.3	100	V
GATE		−0.3	100	V
OFF		−0.3	7	V
nFGD		−0.3	7	V
T_J	Junction Temperature Range	−40	150	°C
T_A	Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	DC Power Supply Voltage	5	75	V
V_{OUT}	Output Voltage	5	75	V
V_{OFF}	OFF Control Voltage	0	5.5	V
V_{nFGD}	MOSFET Status Output	0	5.5	V
T_J	Junction Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,TOP}$	Unit
SOT23-6	155	48	81	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C; typical values at T_J = 25°C, V_{IN} = 12 V, V_{OUT} = 12 V, V_{OFF} = 0 V, C_{GATE}= 47 nF, over operating free-air temperature range, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
IN Pin						
V_{IN}	Supply Input Voltage		5		75	V
I_{IN}	Supply Input Current	V_{IN} = 5 V, V_{OUT} = V_{IN} − 100 mV, GATE = OPEN		287	390	μA
		V_{IN} = 12 V, V_{OUT} = V_{IN} − 100 mV, GATE = OPEN		412	525	μA
		V_{IN} = 75 V, V_{OUT} = V_{IN} − 100 mV, GATE = OPEN		415	525	μA
OUT Pin						
I_{OUT}	OUT Pin Current	V_{IN} = 5 V, V_{OUT} = V_{IN} − 100 mV		78	110	μA
		V_{IN} = 12 V, V_{OUT} = V_{IN} − 100 mV		90	120	μA
		V_{IN} = 75 V, V_{OUT} = V_{IN} − 100 mV		107	180	μA
Gate Pin						
$I_{GATE,ON}$	GATE Pin Source Current	V_{IN} = 5 V to 75 V, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} − 175 mV	20	32	40	μA
$I_{GATE,OFF}$	Gate Pin Sink Current	V_{GATE} = V_{IN} + 3 V, V_{OUT} > V_{IN} + 100 mV, t ≤ 10 ms		1.9		A
V_{GS} (1)	V_{GATE} − V_{IN} in Forward Operation	V_{IN} = 5 V, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} − 175 mV	4	7.9	9	V
		V_{IN} = 12 V, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} − 175 mV	9	10.5	14	V
		V_{IN} = 75 V, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} − 175 mV	9	10.5	14	V
$V_{SD,REG}$	Regulated Forward V_{SD} Threshold, V_{IN} > V_{OUT}	V_{IN} − V_{OUT}	13	23	33	mV
$V_{SD,REV}$	Reverse V_{SD} Threshold, V_{IN} < V_{OUT}	V_{IN} − V_{OUT}	−17	−9.2	−2	mV
$\Delta V_{SD,REV}$	Reverse V_{SD} Hysteresis			9.5		mV
$t_{GATE,REV}$ (2)	Gate Capacitance Discharge Time at Forward to Reverse Transition	C_{GATE} = 0		25	100	ns
		C_{GATE} = 10 nF		80		ns
		C_{GATE} = 47 nF		260	425	ns
$t_{GATE,OFF}$ (2)	Gate Capacitance Discharge Time at OFF Pin Low to High Transition	C_{GATE} = 47 nF		450		ns
OFF Pin						

Parameter		Conditions	Min	Typ	Max	Unit
$V_{OFF,IH}$	OFF Input High-Level Voltage	V_{OUT} = V_{IN} − 500 mV, V_{OFF} Rising		1.55	1.75	V
$V_{OFF,IL}$	OFF Input Low-Level Voltage	V_{OUT} = V_{IN}− 500 mV, V_{OFF} Falling	1.1	1.4		V
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF,IH}$ − $V_{OFF,IL}$		160		mV
I_{OFF}	OFF Pin Internal Pulldown Current	V_{OFF} = 5 V		5	8	µA
nFGD Pin						
$V_{SD,TEST}$	FET Source-to-Drain Test Threshold Voltage, V_{IN} < V_{OUT}	V_{OFF} = 5 V, V_{OUT} = 12 V, V_{IN} Falling from 12 V		332	450	mV
$\Delta V_{SD,TEST}$	FET Source-to-Drain Test Threshold Voltage Hysteresis			85		mV
$V_{OL,nFGD}$	nFGD Output Low Voltage, nFGD Output = On	V_{OFF} = 5 V, I_{nFGD} = 1 mA Sinking		5	400	mV
$I_{OL,nFGD}$	nFGD Output Leakage Current, nFGD Output = Off	V_{OFF} = 0 V, V_{nFGD} = 5.5 V		0.001	1	µA

(1) Measurement of V_{GS} voltage (i.e., V_{GATE}− V_{IN}) includes 1 MΩ in parallel with C_{GATE}.
(2) Not subject to production test, specified by design.

Typical Performance Characteristics

All test conditions: T_A = 25°C, V_{IN} = 12 V, V_{OFF} = 0 V, over operating free-air temperature range (unless otherwise noted).

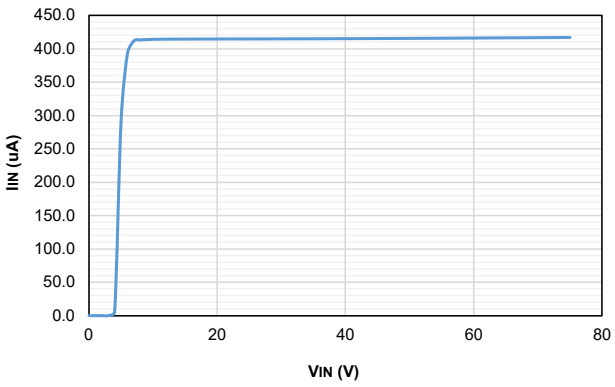


Figure 1. I_{IN} vs. V_{IN}

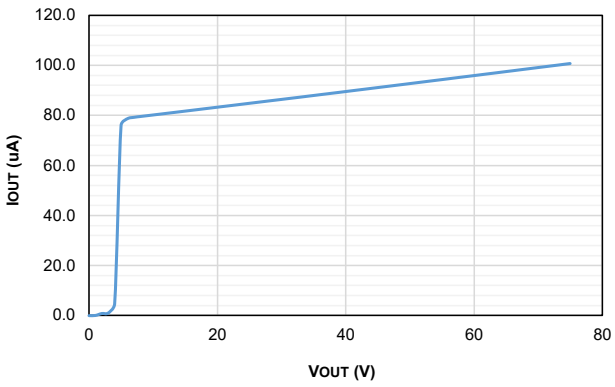


Figure 2. I_{OUT} vs. V_{OUT}

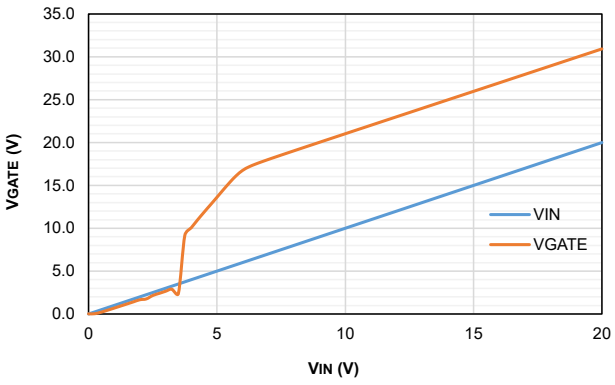


Figure 3. V_{GATE} vs. V_{IN}

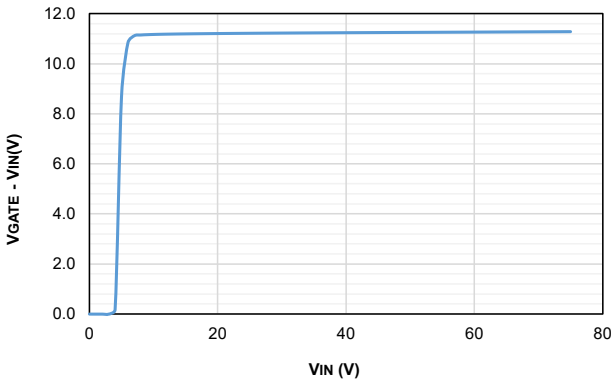


Figure 4. V_{GS} vs. V_{IN}

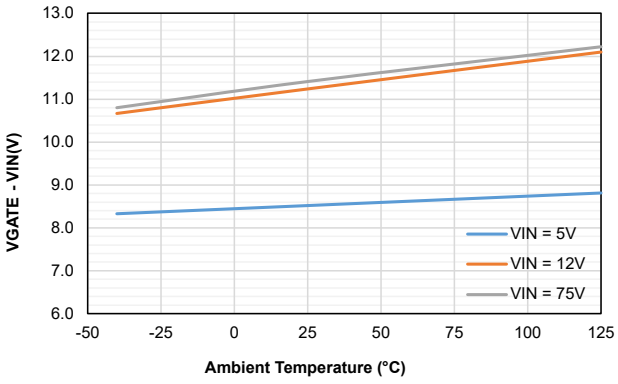
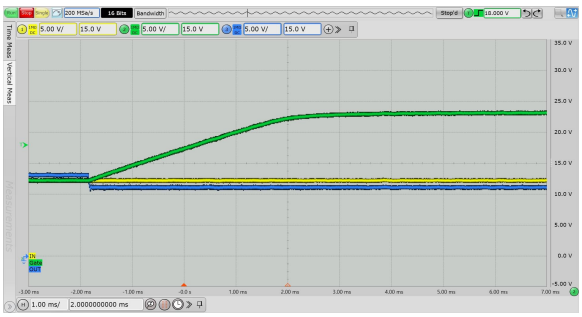
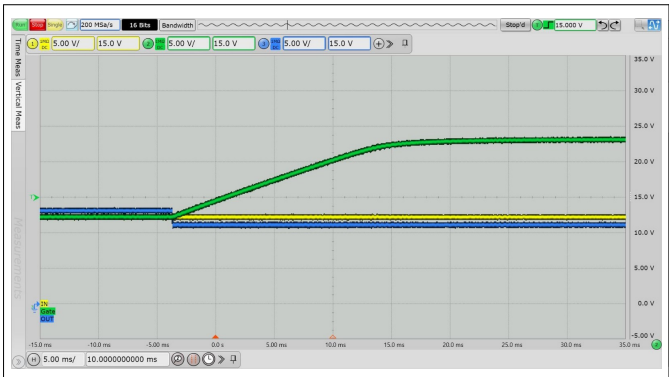


Figure 5. V_{GS} vs. Temperature



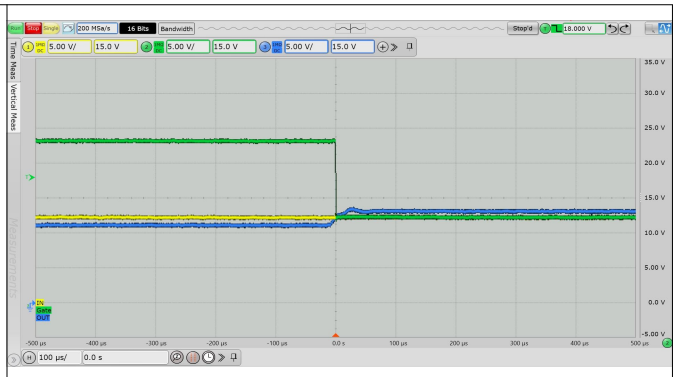
CH1: IN; CH2: GATE; CH3: OUT

Figure 6. Forward Gate Charge Time, C_{GATE} = 10 nF



CH1: IN; CH2: GATE; CH3: OUT

Figure 7. Forward Gate Charge Time, C_{GATE} = 47 nF



CH1: IN; CH2: GATE; CH3: OUT

Figure 8. Reverse Gate Charge Time, C_{GATE} = 10 nF

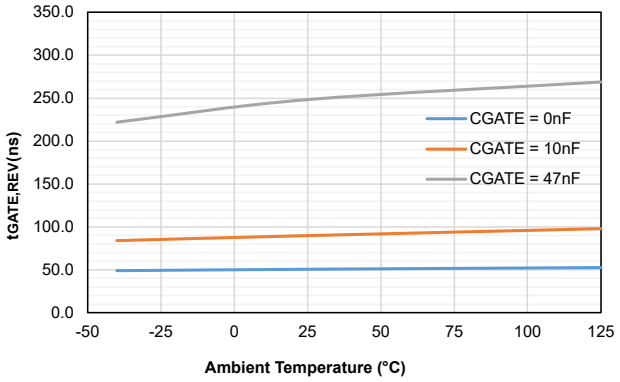


Figure 9. t_{GATE} vs. Temperature

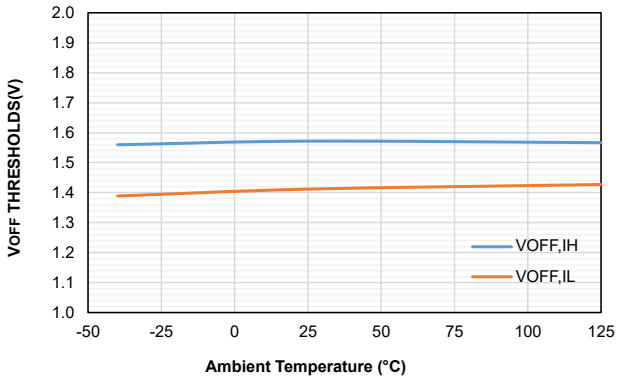


Figure 10. OFF Pin Thresholds vs. Temperature

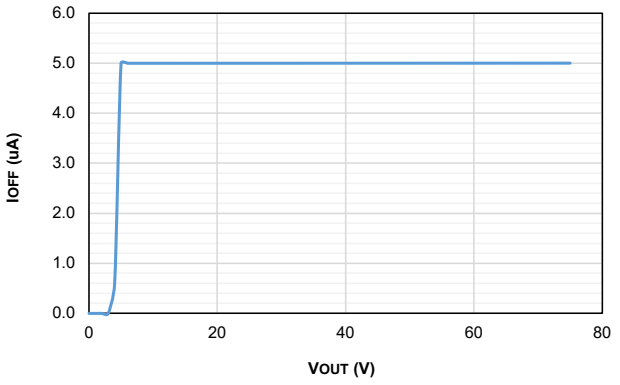
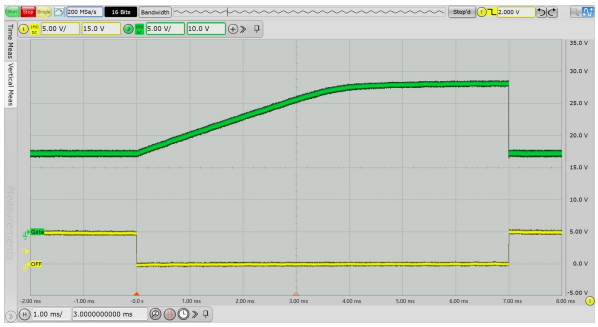
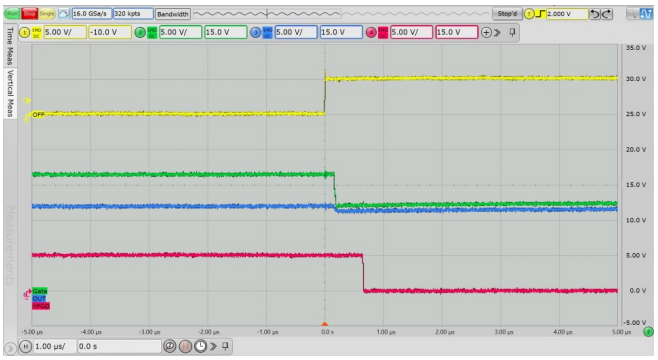


Figure 11. OFF Pin Pull-Down vs. V_{OUT}



CH1: OFF; CH2: GATE

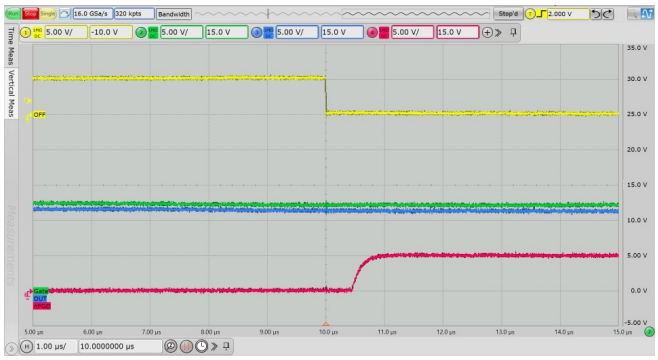
Figure 12. CGATE Charge and Discharge, C_{GATE} = 10 nF



CH1: OFF; CH2: GATE; CH3: OUT; CH4: nFGD

V_{IN} = 12 V, I_{LOAD} = 4 A, C_{OUT} = 0

Figure 13. OFF Pin, On to Off Transition



CH1: OFF; CH2: GATE; CH3: OUT; CH4: nFGD

V_{IN} = 12 V, I_{LOAD} = 4 A, C_{OUT} = 0

Figure 14. OFF Pin, Off to On Transition

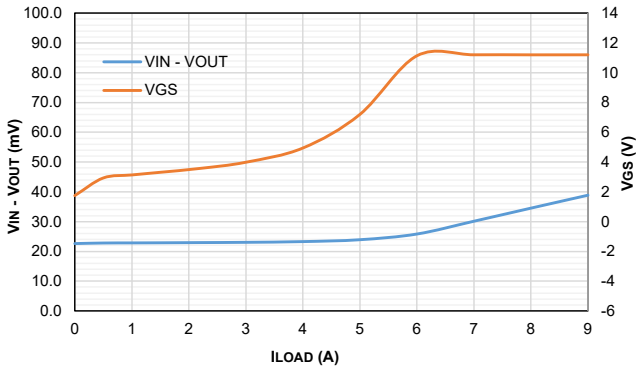


Figure 15. GATE Pin vs. Ron * I_{DS}

Detailed Description

Overview

The TPS75R01A is an ideal diode controller that operates with an external N-channel MOSFET for reverse protection applications or redundant power supply applications. The forward voltage drop is controlled at as low as 20 mV, which can significantly reduce power loss to replace an ordinary Schottky Diode in power distribution networks.

The TPS75R01A supports a wide operating voltage range from 5 V to 75 V, with an absolute maximum rating of 100 V. The support for a transient 100-V input voltage is particularly suitable to meet the severe requirement in 48-V power supply systems.

The TPS75R01A integrates a charge pump to drive the external N-channel MOSFET. The device provides precise gate control to regulate the voltage drop between the source and drain at 20 mV. When it detects a reverse voltage of −10 mV from IN to OUT, the TPS75R01A will turn off the external MOSFET within 450 ns maximum to ensure no reverse current flows. The TPS75R01A also features a MOSFET test mode. It allows the MCU controller to test the shorted MOSFET.

Functional Block Diagram

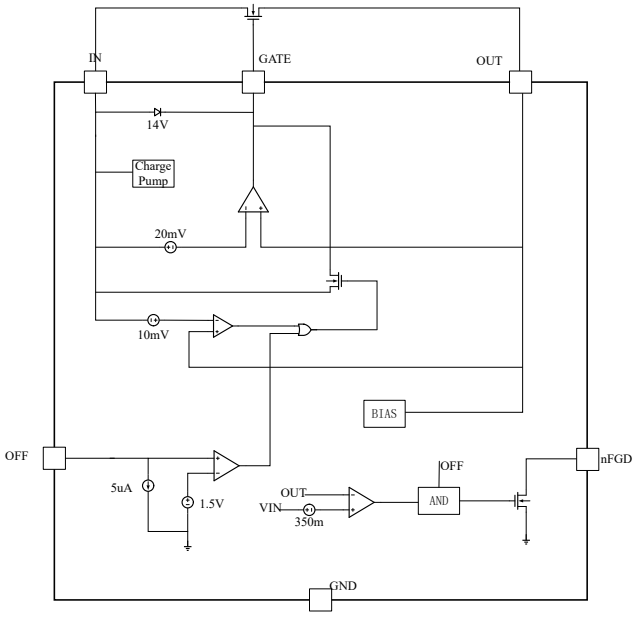


Figure 16. Functional Block Diagram

Feature Description

Input Power Supply Voltage (IN)

The TPS75R01A uses the IN pin to power up the internal circuitry with a supply voltage ranging from 5 V to 75 V. The maximum voltage range from IN to GND is 100 V.

In, Gate, and Out Pins

When power is first applied, the load current flows from source to drain through the MOSFET's body diode. The voltage across this diode is detected by the TPS75R01A's IN and OUT pins, and then the TPS75R01A starts charging the MOSFET gate via a 30 μA (typical) charge pump current source. In normal operation, the MOSFET gate is charged until it's typically 10.5V above the IN pin. When the IN pin voltage is less than about 10V, the gate is charged to typically twice the IN pin voltage.

The TPS75R01A is designed to regulate the MOSFET gate-to-source voltage if the voltage across the MOSFET source and drain pins drops below the typical 20 mV $V_{SD(REG)}$ voltage.

When the MOSFET current drops to the extent that the voltage across the MOSFET is below the typical 20 mV $V_{SD(REG)}$ voltage regulation point, the GATE pin voltage is reduced until the voltage across the MOSFET is regulated at 20 mV. In case the drain-to-source voltage is higher than the VSD(REG) voltage, the gate-to-source voltage rises and eventually reaches the 10.5-V zener clamp level between the GATE and IN pins.

If the MOSFET current reverses, perhaps due to a failure of the input supply, and the voltage across the TPS75R01A IN and OUT pins becomes more negative than the typical -10 mV $V_{SD(REV)}$ voltage, the TPS75R01A promptly dischargse the MOSFET gate by means of a powerful GATE to IN pin discharge transistor.

When the input supply fails suddenly, like when it's directly shorted to the ground, a reverse current flows through the MOSFET temporarily until the gate is fully discharged. This reverse current comes from the output load capacitance and the parallel-connected supplies. The TPS75R01A typically responds to a voltage reversal condition within 25 ns. The actual time needed to turn off the MOSFET depends on the charge held by the gate capacitance of the MOSFET in use. For a MOSFET with an effective gate capacitance of 47 nF, it can typically be turned off in 260 ns. This fast turn-off time minimizes voltage disturbances at the output and reduces current transients from the redundant supplies.

Off Pin and nFGD Pin

The OFF pin serves as a logic level input pin, which is utilized for controlling the gate drive of the external MOSFET when in the FET Test Mode. Its maximum operating voltage is capped at 5.5V. The nFGD pin, on the other hand, is an open-drain output pin that can support a logic level voltage, and its maximum operating voltage is also 5.5 V.

When the OFF pin is at a high level, the MOSFET gets turned off regardless of the sensed IN and OUT voltages, and simultaneously, the FET Test Mode gets activated. In this mode, the load current flows through the body diode of the MOSFET. If the MOSFET is functioning normally via the body diode, the voltage difference between the IN pin and the OUT pin is around 700 mV. The FET test comparator of the TPS75R01A keeps an eye on the voltage difference between the IN and OUT pins, with a typical $V_{SD(TST)}$ threshold of 332 mV. If the voltage difference between the IN pin and the OUT pin is larger than this threshold, the nFGD pin shifts to a low impedance state and its voltage becomes a logic low.

In the event that the MOSFET is shorted, the voltage difference between the IN pin and the OUT pin is less than the $V_{SD(TST)}$ threshold. Then, the nFGD pin stays in a high impedance state, and its pin voltage can be pulled high by an external pull-up resistor.

During normal operation, the OFF pin has to be pulled low or can be left open. In this situation, the GATE pin voltage relys on the forward or reverse voltage across the MOSFET from source to drain, as has been described before.

Typically, the OFF pin has an internal pull-down current of 5 μA. If the OFF function isn't needed, this pin can either be left open or connected to the ground.

When the OFF pin is at a low level, the nFGD pin always remains in a high impedance open state.

There are several factors that can make the nFGD pin unable to show that the external MOSFET is operating normally. For example, when the TPS75R01A is employed to connect parallel and redundant power supplies, one of the connected supplies might keep the OUT pin voltage close enough to the IN pin voltage of the TPS75R01A so that the $V_{SD(TST)}$ threshold isn't exceeded. Moreover, when operating with a high output capacitance value and a low load current, it might take a considerable amount of time before the output capacitance is discharged to the point where the $V_{SD(TST)}$ threshold is surpassed and the nFGD pin switches to a low state.

Short Circuit Failure of an Input Supply

When there is an abrupt zero-ohm short circuit across the input supply, the highest possible reverse current flows as the internal control circuitry of the TPS75R01A discharges the gate of the MOSFET. During this period, the reverse current is restricted only by the on-resistance $R_{DS(ON)}$ of the MOSFET along with the parasitic resistances and inductances of the wiring. The worst-case instantaneous reverse current is limited in accordance with the following formula:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator responds and initiates the process of discharging the Gate when the reverse current reaches the level determined by this formula:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

Once the MOSFET is finally turned off, the energy stored in the parasitic wiring inductances is transferred to the rest of the circuit. Consequently, the TPS75R01A IN pin experiences a negative voltage spike while the OUT pin has a positive voltage spike. To protect the IN pin, it can be diode-clamped to the ground in the negative direction. For the OUT pin, it can be safeguarded by using a transient voltage suppression (TVS) protection diode, a local bypass capacitor, or both. In low-voltage applications, the drain-to-source breakdown voltage rating of the MOSFET might be sufficient to protect the OUT pin. However, since most MOSFET datasheets don't specify the maximum breakdown rating clearly, this method should be employed with caution.

Table 2. FET Test Status Table

OFF Pin	Mode	FET Gate Drive	VIN - VOUT	FET Status	nFGD Pin Status	nFGD Pin Voltage
Low or Open	Normal Operation	Active	-	-	High Z	High
High	FET Test	Off	> $V_{SD(TST)}$	OK	Low Z	Low
			< $V_{SD(TST)}$	Not OK	High Z	High

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPS75R01A is an ideal diode controller operating with an external N-channel MOSFET for reverse protection and redundant power supplies applications. The following Typical Application section shows a typical usage of the TPS75R01A.

Typical Application

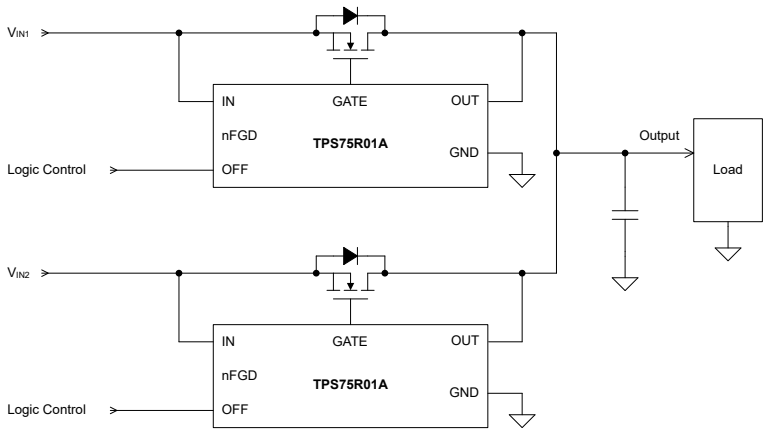


Figure 17. Typical Application

Layout

Layout Guideline

- Connect the IN, GATE, and OUT pins of TPS75R01A close to the source, gate, and drain pins of the external N-channel MOSFET.
- Connect the GATE pin of TPS75R01A to the gate pin of the external N-channel MOSFET with short and wide traces to avoid turn-off delay due to the trace resistance.
- For the high current path through the external N-channel MOSFET, it is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Layout Example

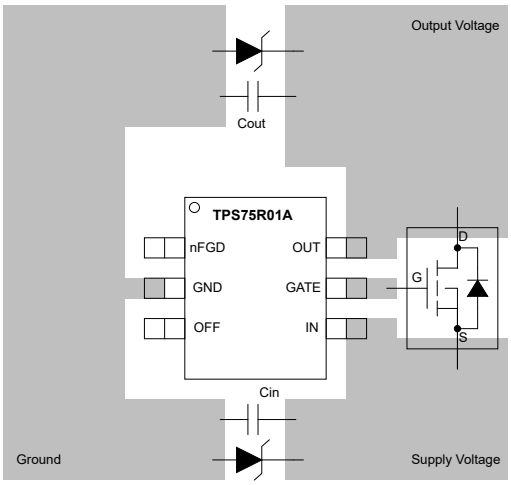
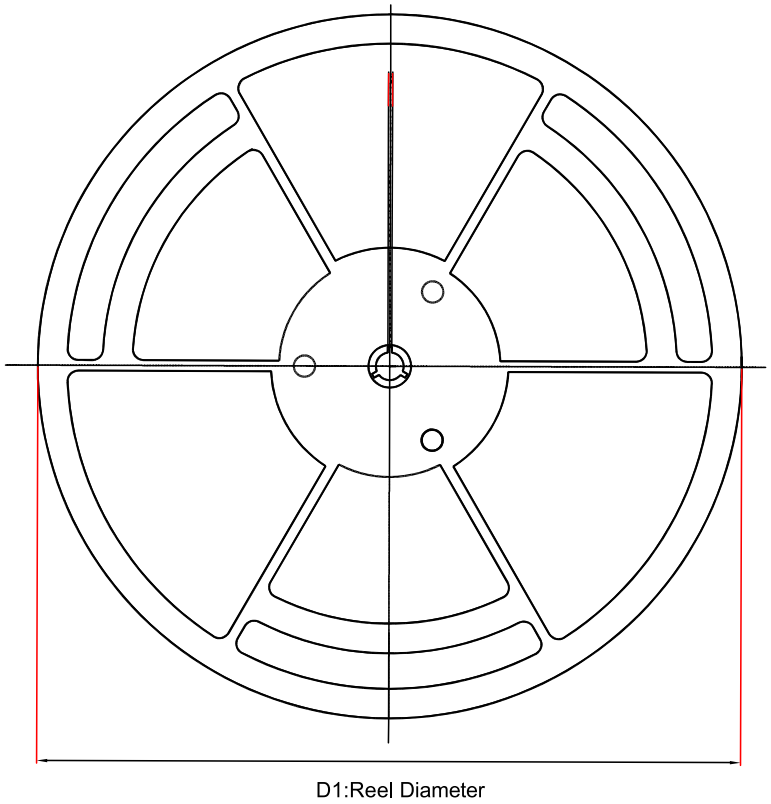
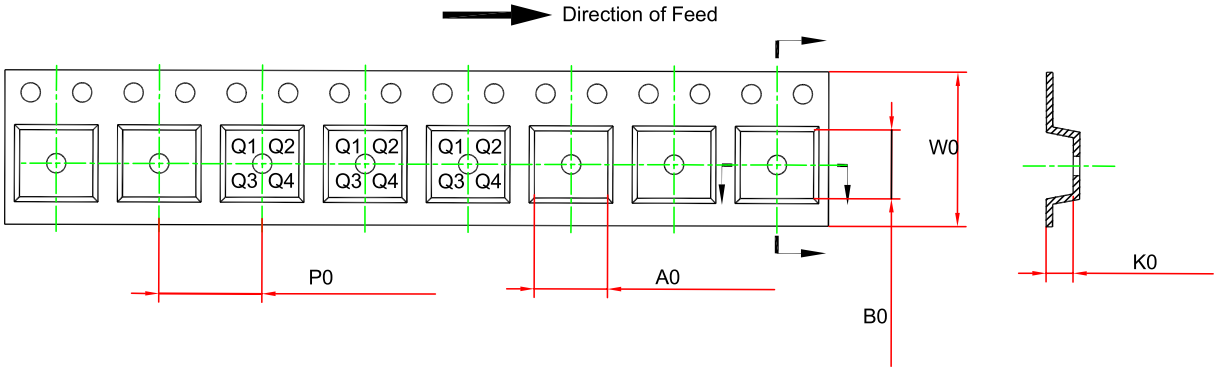


Figure 18. Layout Example

Tape and Reel Information



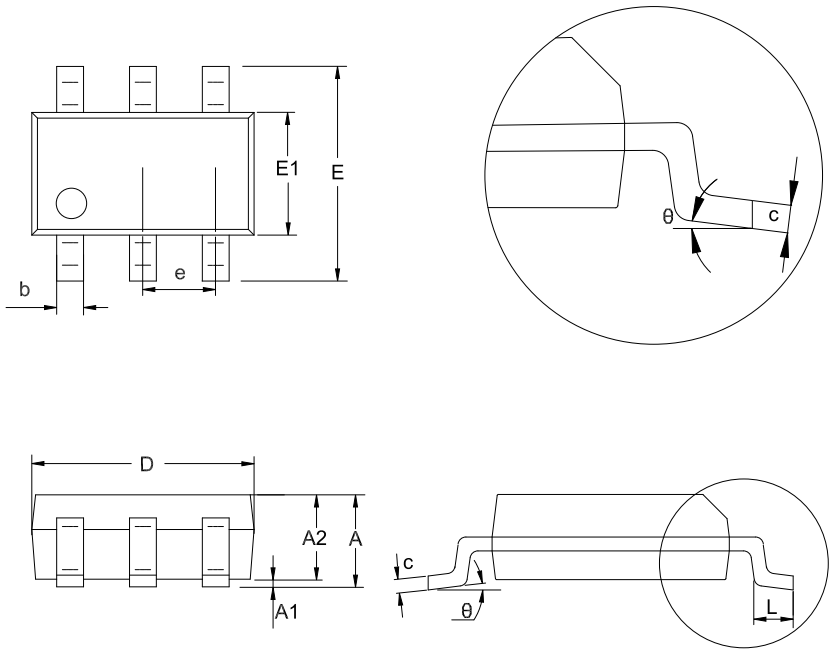


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS75R01A-S6TR-S	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS75R01A-S6TR-S	−40 to 150°C	SOT23-6	S7A	MSL2	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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