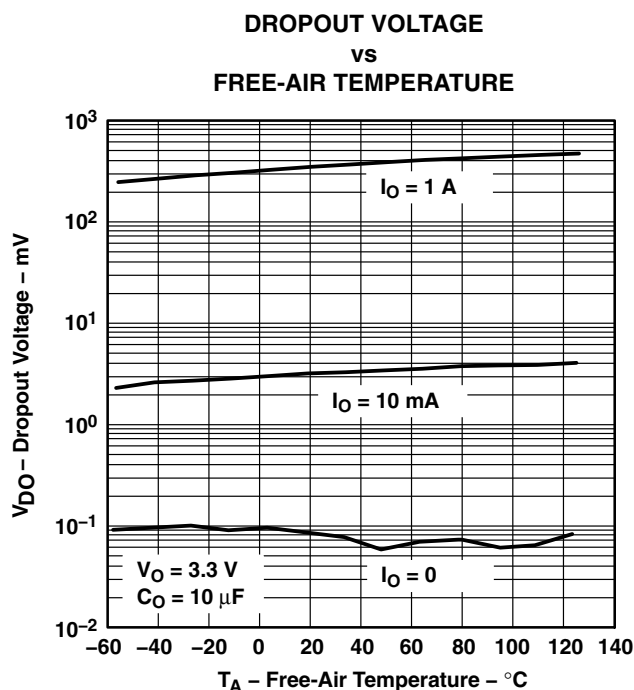
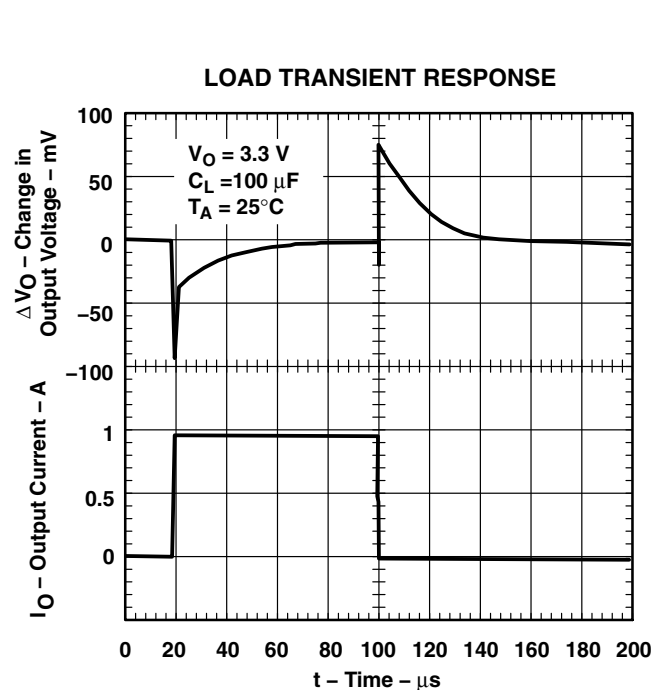


TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 350 mV at an output current of 1 A for the TPS767D325) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μA at $T_J = 25^\circ\text{C}$.

The $\overline{\text{RESET}}$ output of the TPS767D3xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767D3xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767D3xx is offered in 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767D3xx family is available in 28 pin PWP TSSOP package. They operate over a junction temperature range of -40°C to 125°C .

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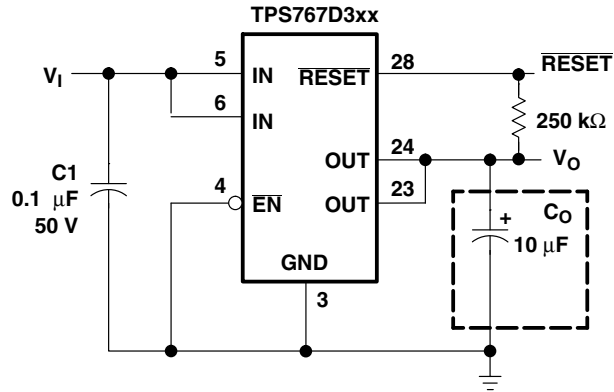
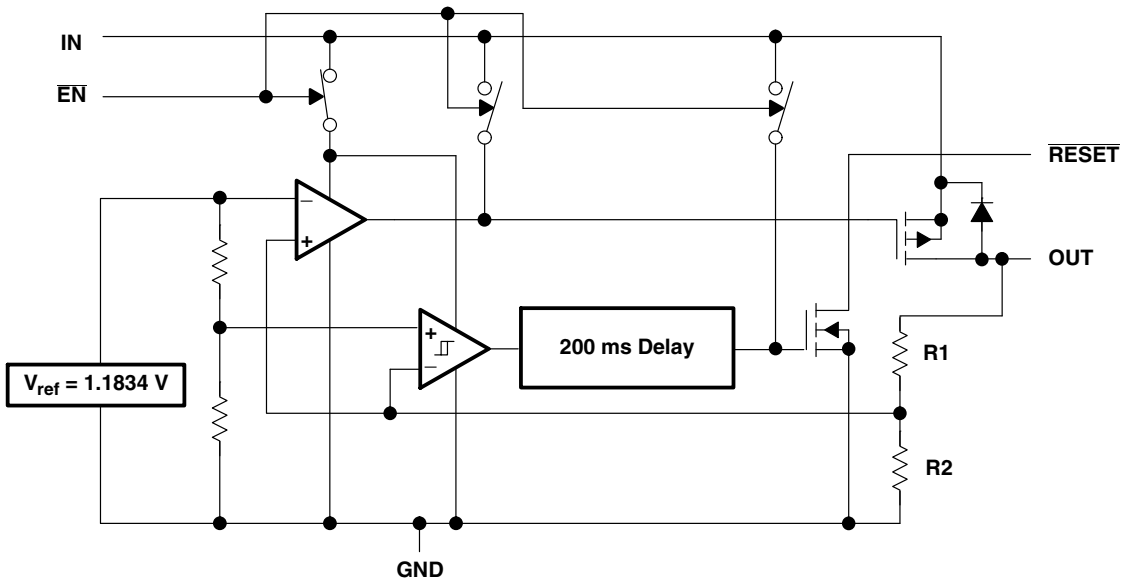


Figure 1. Typical Application Circuit (Fixed Versions) for Single Channel

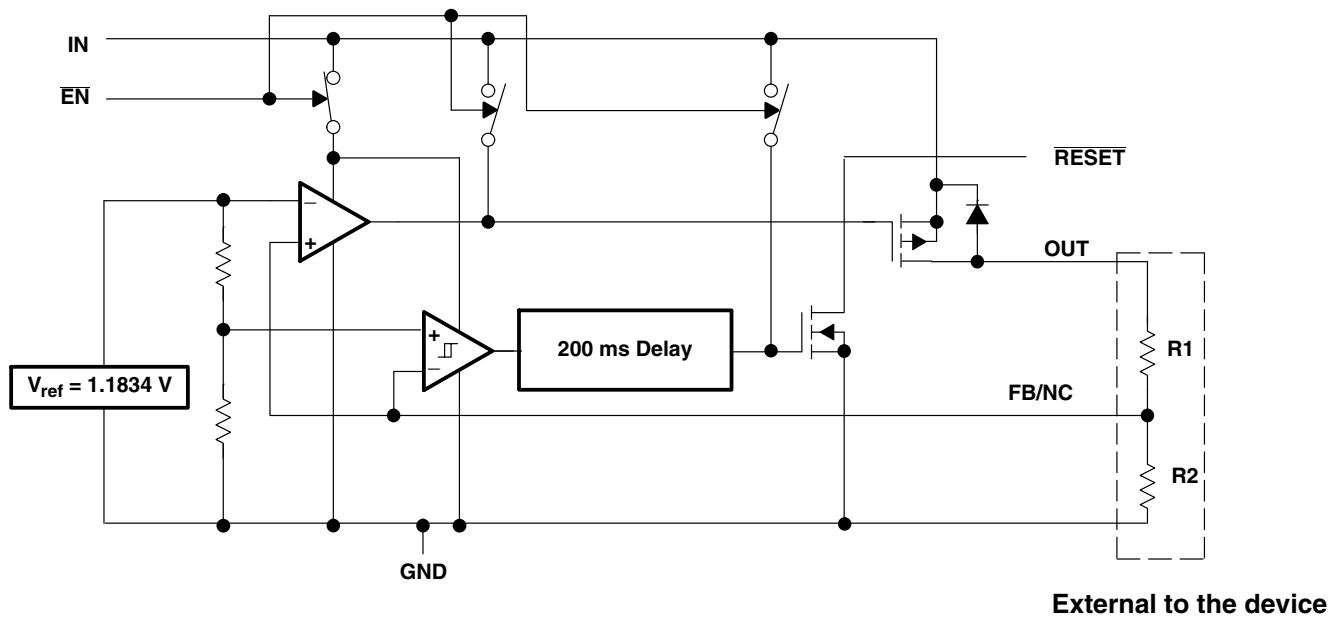
TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram—adjustable version (for each LDO)



functional block diagram—fixed-voltage version (for each LDO)



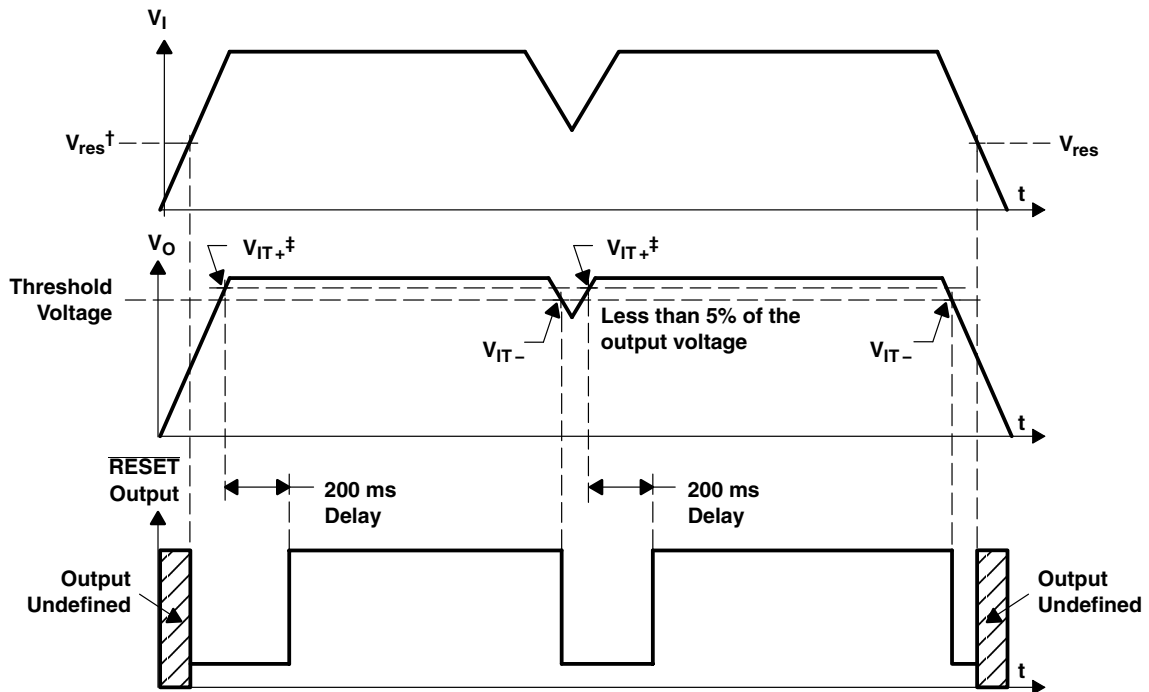
TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
1GND	3		Regulator #1 ground
$\overline{1EN}$	4	I	Regulator #1 enable
1IN	5, 6	I	Regulator #1 input supply voltage
2GND	9		Regulator #2 ground
$\overline{2EN}$	10	I	Regulator #2 enable
2IN	11, 12	I	Regulator #2 input supply voltage
2OUT	17, 18	O	Regulator #2 output voltage
$\overline{2RESET}$	22	O	Regulator #2 reset signal
1OUT	23, 24	O	Regulator #1 output voltage
1FB/NC	25	I	Regulator #1 output voltage feedback for adjustable and no connect for fixed output
$\overline{1RESET}$	28	O	Regulator #1 reset signal
NC	1, 2, 7, 8, 13–16, 19, 20, 21, 26, 27		No connection

timing diagram



† V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT-} Trip voltage is typically 5% lower than the output voltage ($95\%V_O$)

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Input voltage range [‡] , V_I	-0.3 V to 13.5 V
Input voltage range, V_I (1IN, 2IN, \overline{EN})	-0.3 V to $V_I + 0.3$ V
Output voltage, V_O (1OUT, 2OUT)	7 V
Output voltage, V_O (RESET)	16.5 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP [§]	0	3.58 W	35.8 mW/°C	1.97 W	1.43 W
	250	5.07 W	50.7 mW/°C	2.79 W	2.03 W

This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on 4-in x 4-in ground layer. For more information, refer to TI technical brief literature number SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I [¶] (1IN, 2IN)	2.7	10	V
Output current for each LDO, I_O (Note 1)	0	1.0	A
Output voltage range, V_O (1OUT, 2OUT)	1.5	5.5	V
Operating virtual junction temperature, T_J	-40	125	°C

[¶] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



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electrical characteristics, $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (V_O) (see Note 2)	Adjustable	$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	V_O			V
			$T_J = -40^\circ\text{C}$ to 125°C	$0.98V_O$	$1.02V_O$		
	1.8 V Output	$2.8\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	1.8			
			$T_J = -40^\circ\text{C}$ to 125°C	1.764	1.836		
	2.5 V Output	$3.5\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	2.5			
			$T_J = -40^\circ\text{C}$ to 125°C	2.45	2.55		
	3.3 V Output	$4.3\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	3.3			
			$T_J = -40^\circ\text{C}$ to 125°C	3.234	3.366		
Quiescent current (GND current) for each LDO (see Note 2)		$10\text{ }\mu\text{A} < I_O < 1\text{ A}$, $T_J = 25^\circ\text{C}$	85			μA	
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C	125				
Output voltage line regulation for each LDO ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$		0.01		%/V	
Output noise voltage		BW = 200 Hz to 100 kHz, $V_O = 1.8\text{ V}$, $I_C = 1\text{ A}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$		55		μV_{rms}	
Output current limit for each LDO		$V_O = 0\text{ V}$		1.7	2	A	
Thermal shutdown junction temperature				150		$^\circ\text{C}$	
Standby current for each LDO		$2.7 < V_I < 10\text{ V}$, $T_J = 25^\circ\text{C}$,	$\overline{EN} = V_I$		1	μA	
			$\overline{EN} = V_I$			10	
FB input current	Adjustable	FB = 1.5 V		2		nA	
High level enable input voltage				2.0		V	
Low level enable input voltage				0.8		V	
Power supply ripple rejection (see Note 2)		$f = 1\text{ KHz}$, $T_J = 25^\circ\text{C}$, $C_O = 10\text{ }\mu\text{F}$		60		dB	
Reset	Minimum input voltage for valid RESET		$I_{O(\text{RESET})} = 300\text{ }\mu\text{A}$		1.1		V
	Trip threshold voltage		V_O decreasing		92	98	% V_O
	Hysteresis voltage		Measured at V_O		0.5		% V_O
	Output low voltage		$V_I = 2.7\text{ V}$, $I_{O(\text{RESET})} = 1\text{ mA}$		0.15	0.4	V
	Leakage current		$V_{(\text{RESET})} = 7\text{ V}$		1		μA
	RESET time-out delay				200		mA

NOTES: 2. Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1\text{ V}$, whichever is greater. maximum IN voltage 10V.
3. If $V_O \leq 1.8\text{ V}$, $V_{\text{Imin}} = 2.7\text{ V}$, and $V_{\text{Imax}} = 10\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - 2.7\text{ V})}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$, $V_{\text{Imin}} = V_O + 1\text{ V}$, and $V_{\text{Imax}} = 10\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - (V_O + 1\text{ V}))}{100} \times 1000$$

TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics, $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)
(continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current (\overline{EN})	$\overline{EN} = 0\text{ V}$	-1	0	1	μA
	$\overline{EN} = V_I$	-1		1	
Load regulation			3		mV
Dropout voltage (see Note 4)	$V_O = 3.3\text{ V}$, $I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	350		mV
		$T_J = -40^\circ\text{C}$ to 125°C		575	

NOTE 4: I_N voltage equals $V_O(\text{Typ}) - 100\text{mV}$; Adjustable output voltage set to 3.3V nominal with external resistor divider. 1.8V, and 2.5V dropout voltage is limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	vs Output current	2, 3, 4
	vs Free-air temperature	5, 6, 7
Ground current	vs Free-air temperature	8, 9
Power supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
Dropout voltage	vs Free-air temperature	13
Line transient response		14, 16
Load transient response		15, 17
Output voltage	vs Time	18
Dropout voltage	vs Input voltage	19
Equivalent series resistance (ESR)	vs Output current, $T_A = 25^\circ\text{C}$	21
	vs Output current, $T_J = 125^\circ\text{C}$	22
	vs Output Current, $T_A = 25^\circ\text{C}$	23
	vs Output current, $T_J = 125^\circ\text{C}$	24



TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

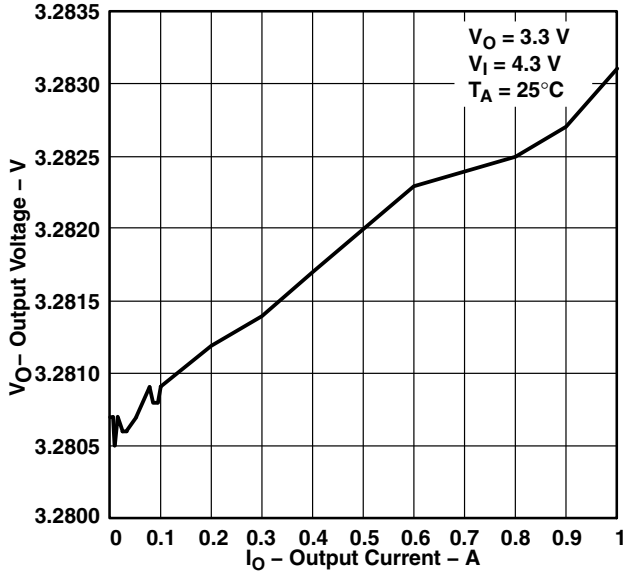


Figure 2

**OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

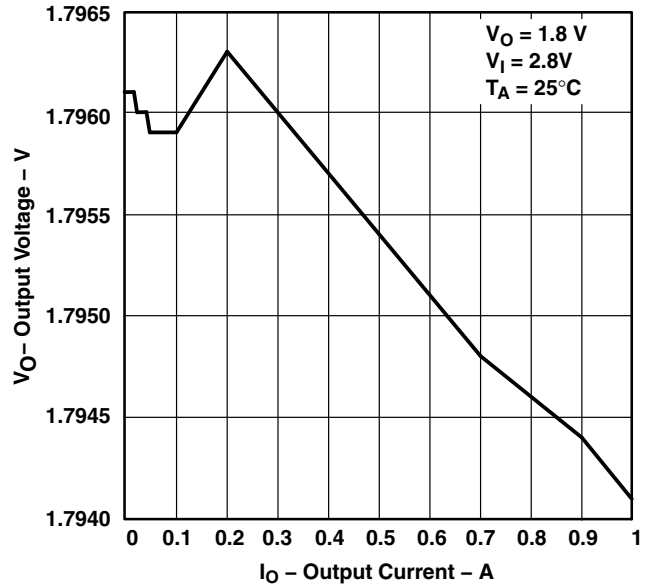


Figure 3

**OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

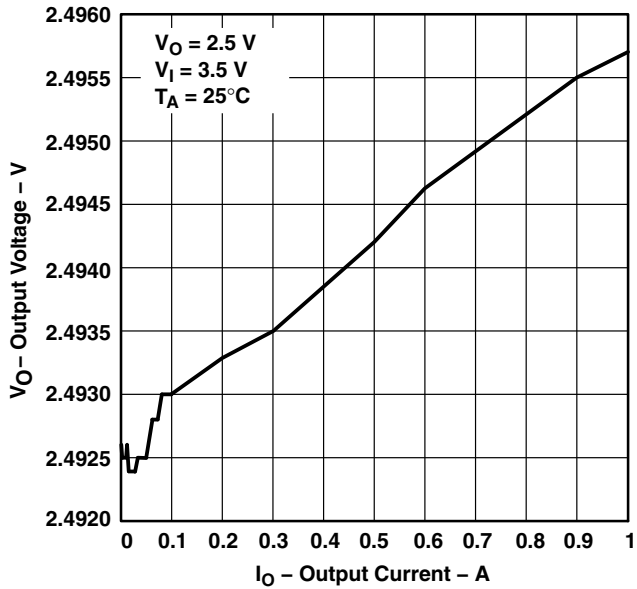


Figure 4

**OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

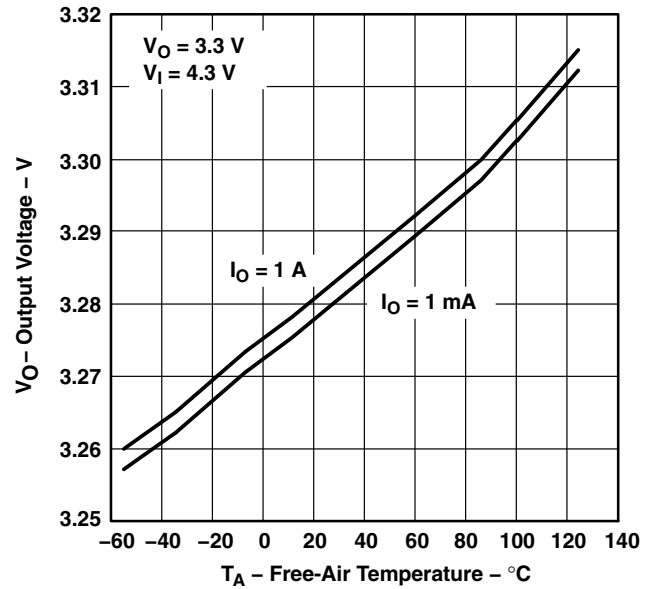


Figure 5



TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

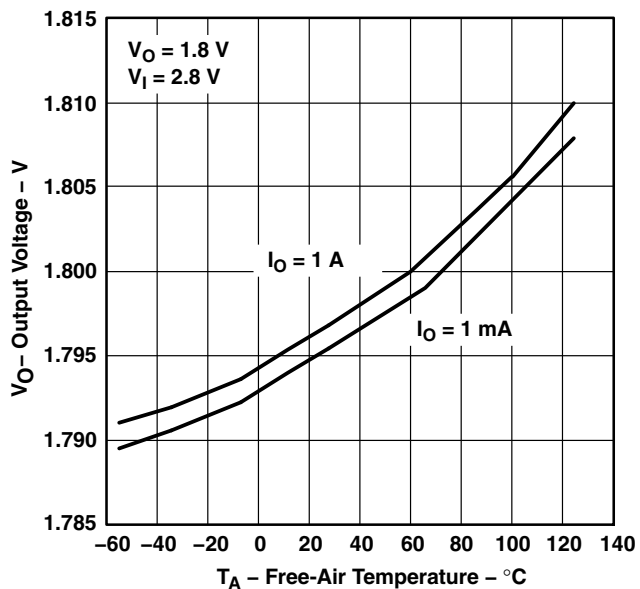


Figure 6

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

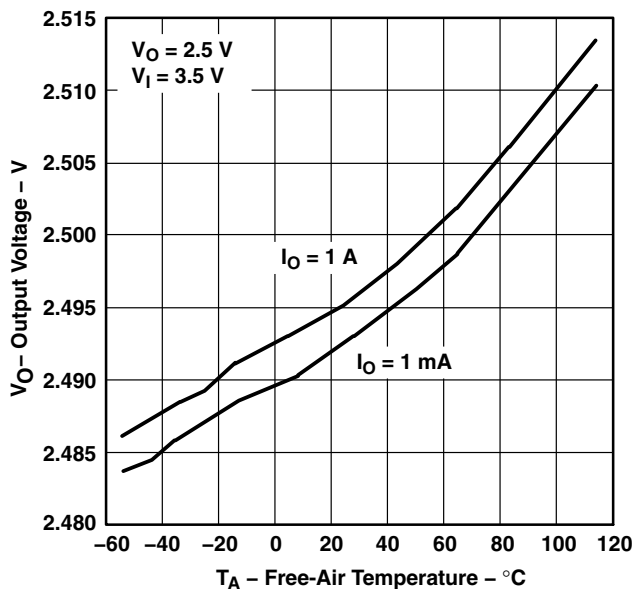


Figure 7

GROUND CURRENT
vs
FREE-AIR TEMPERATURE

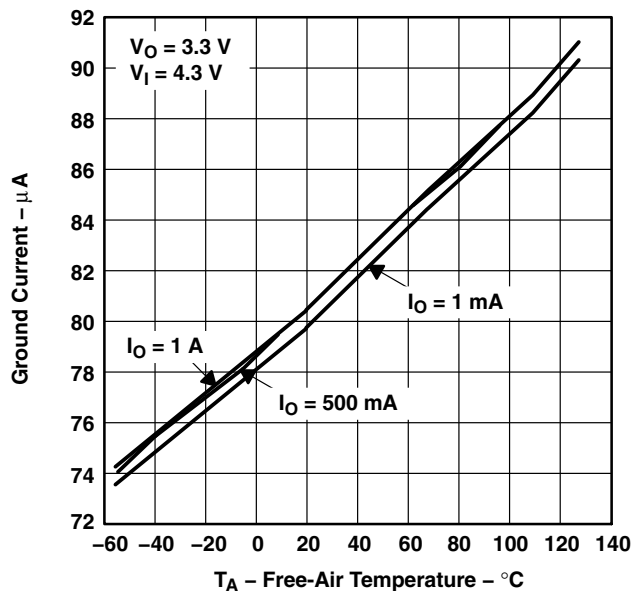


Figure 8

GROUND CURRENT
vs
FREE-AIR TEMPERATURE

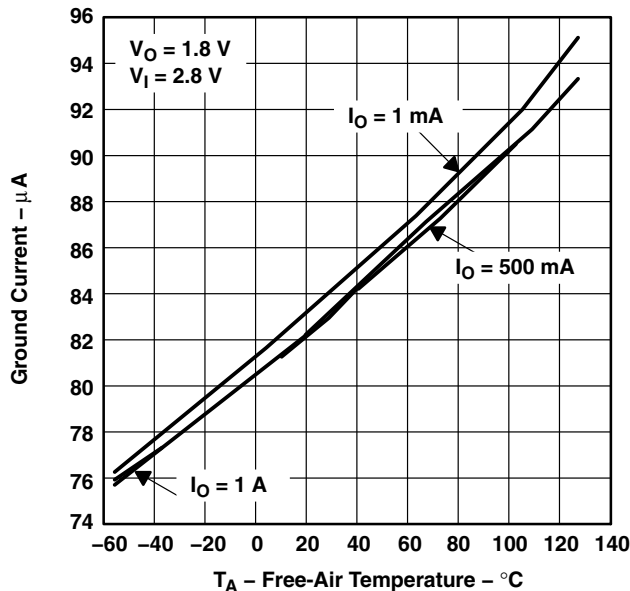


Figure 9



TYPICAL CHARACTERISTICS

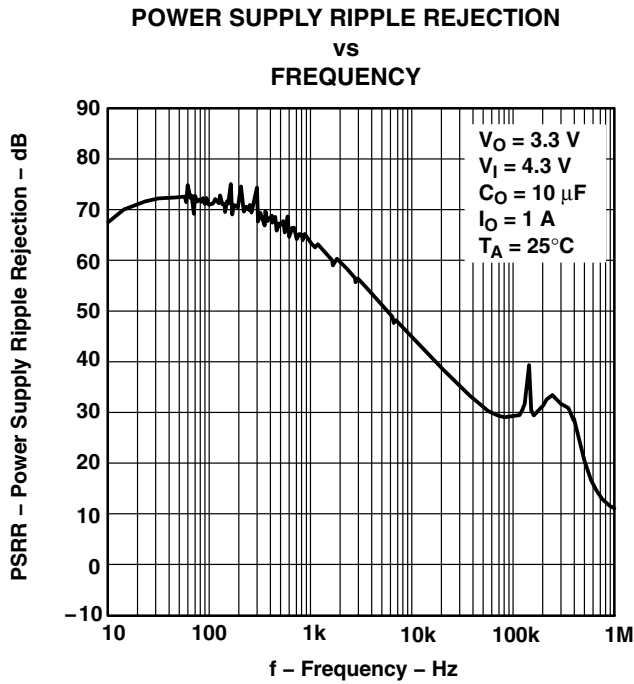


Figure 10

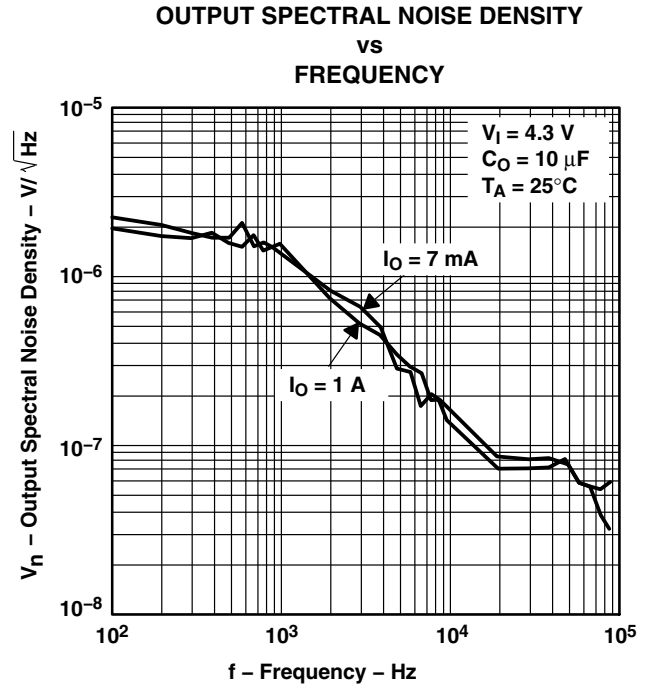


Figure 11

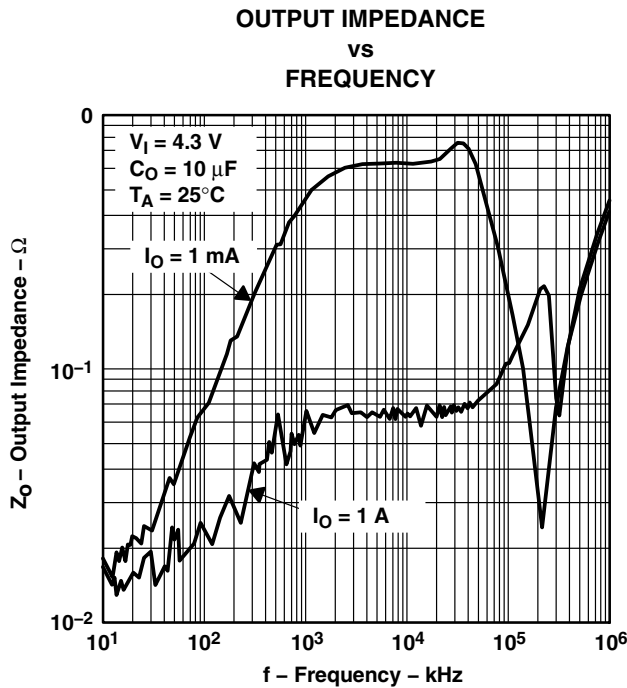


Figure 12

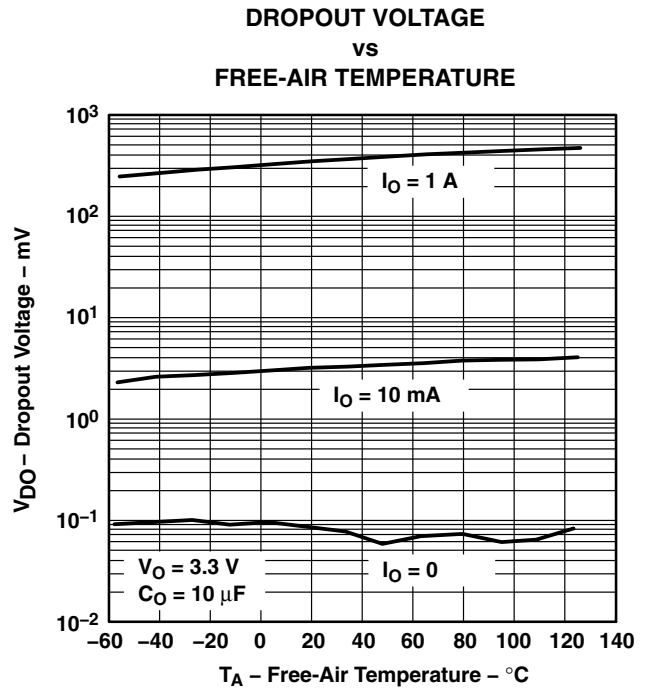


Figure 13

TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

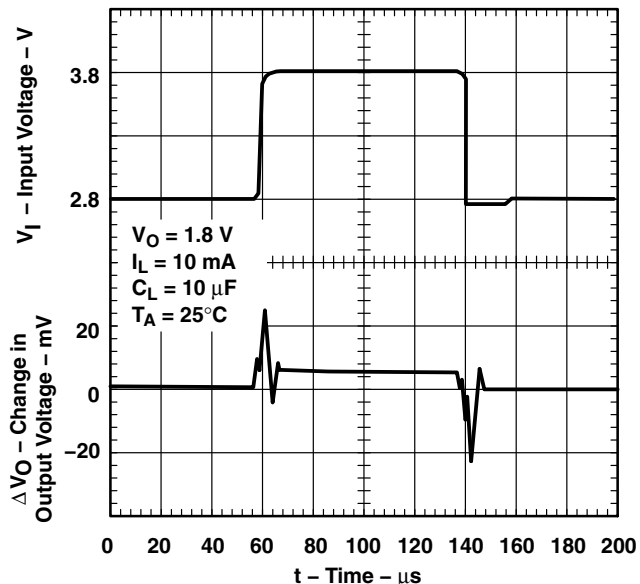


Figure 14

LOAD TRANSIENT RESPONSE

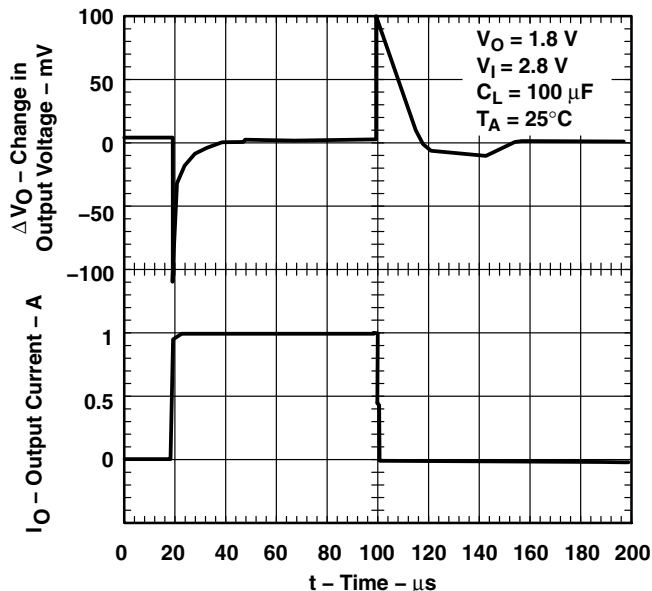


Figure 15

LINE TRANSIENT RESPONSE

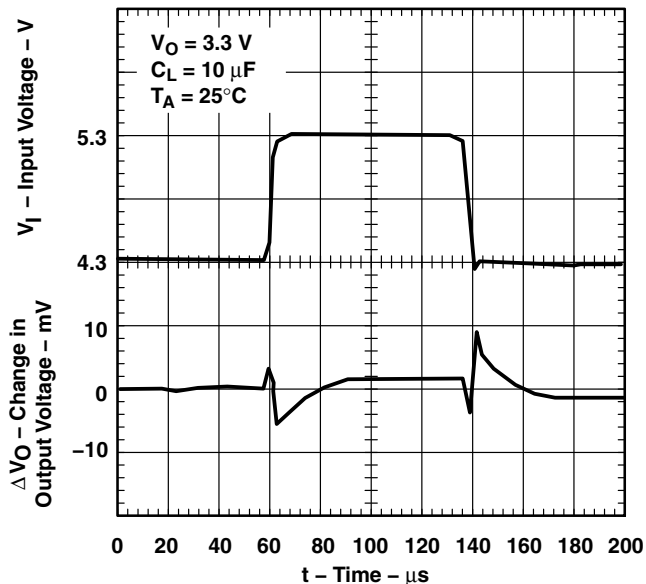


Figure 16

LOAD TRANSIENT RESPONSE

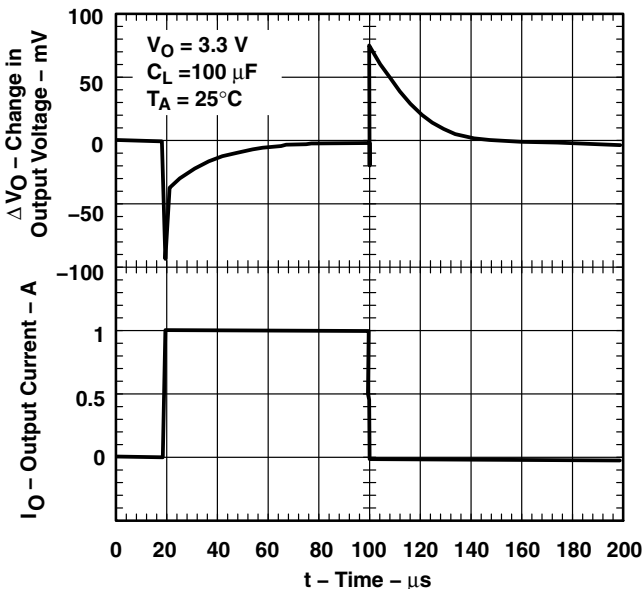


Figure 17

TYPICAL CHARACTERISTICS

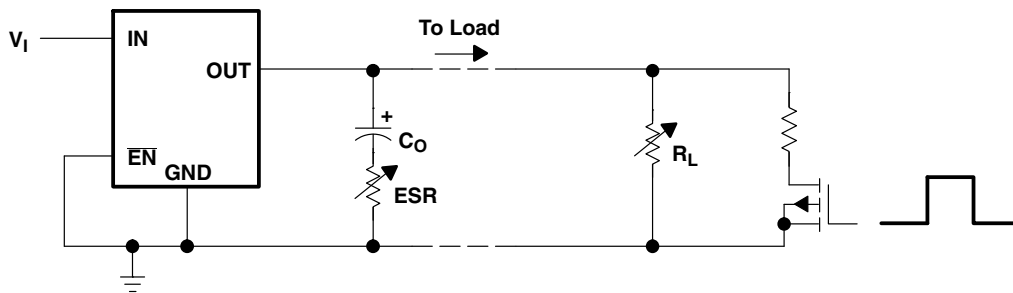
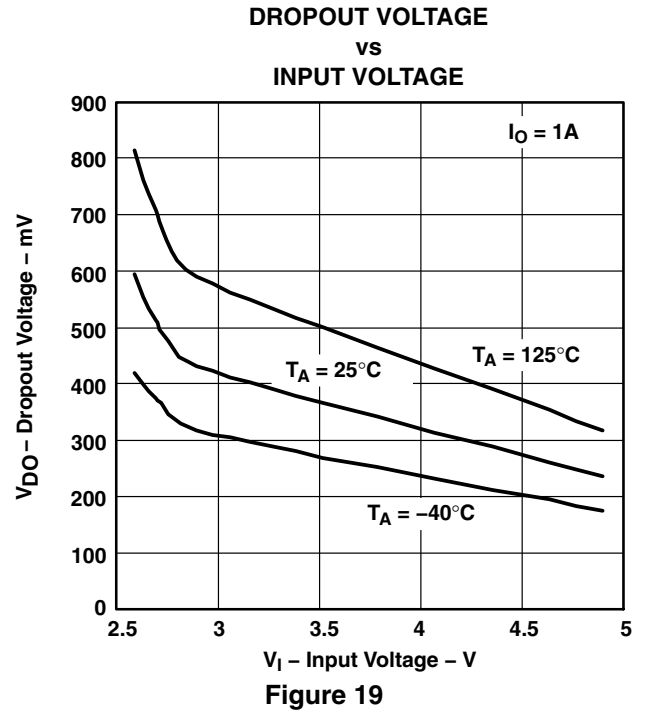
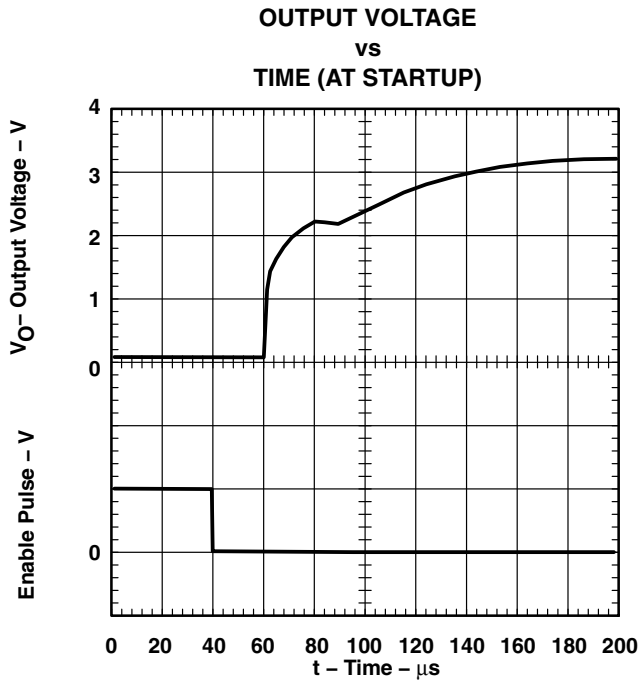


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (fixed output options)

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TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

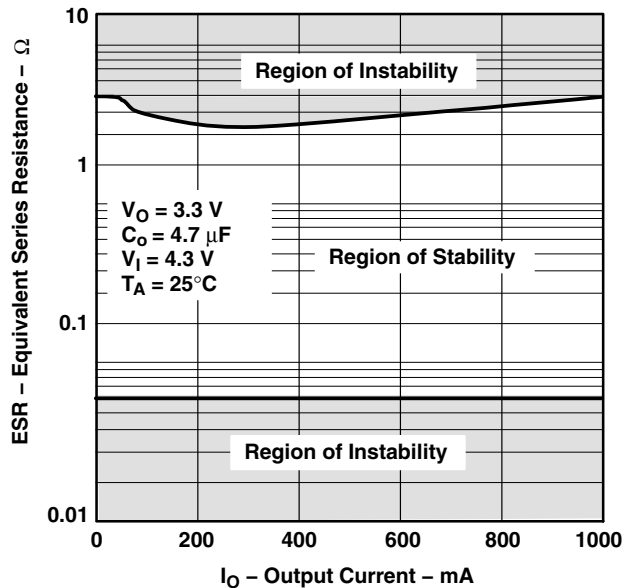


Figure 21

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

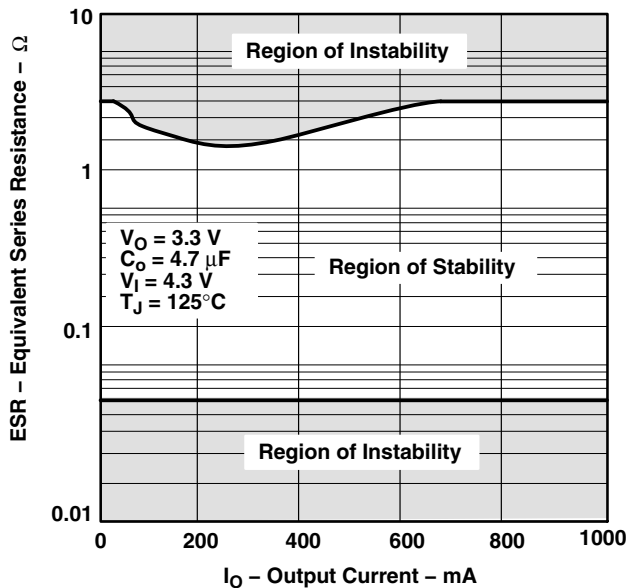


Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

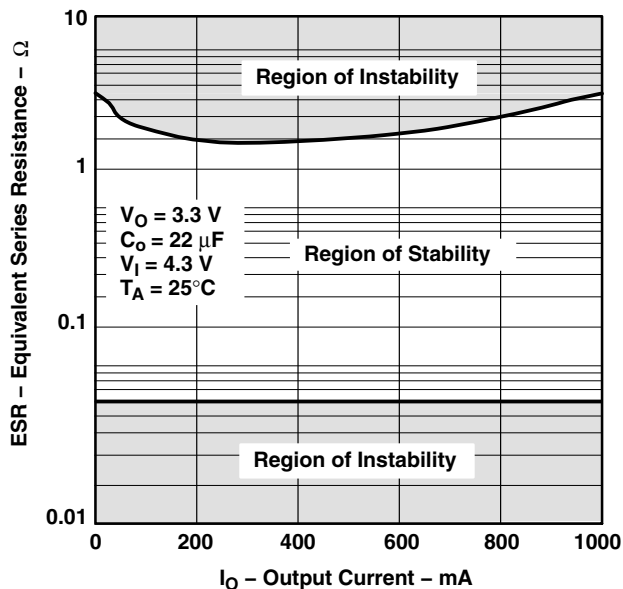


Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

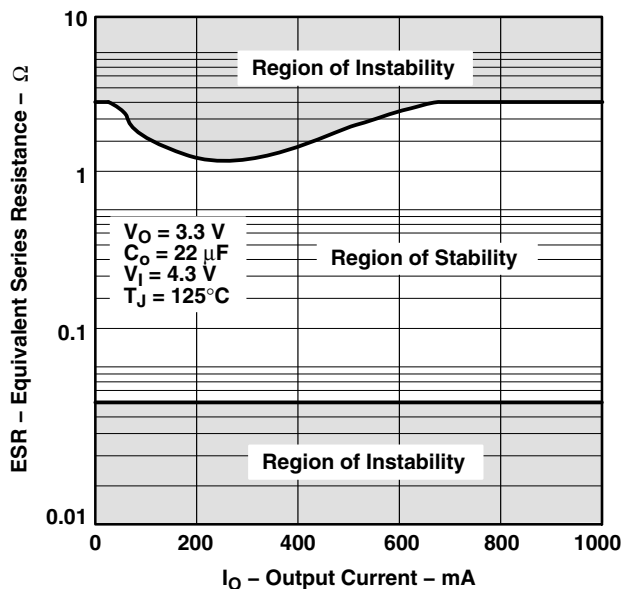


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

The features of the TPS767D3xx family (low-dropout voltage, ultra low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package have enabled the integration of the dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 25 shows a typical dual-voltage DSP application.

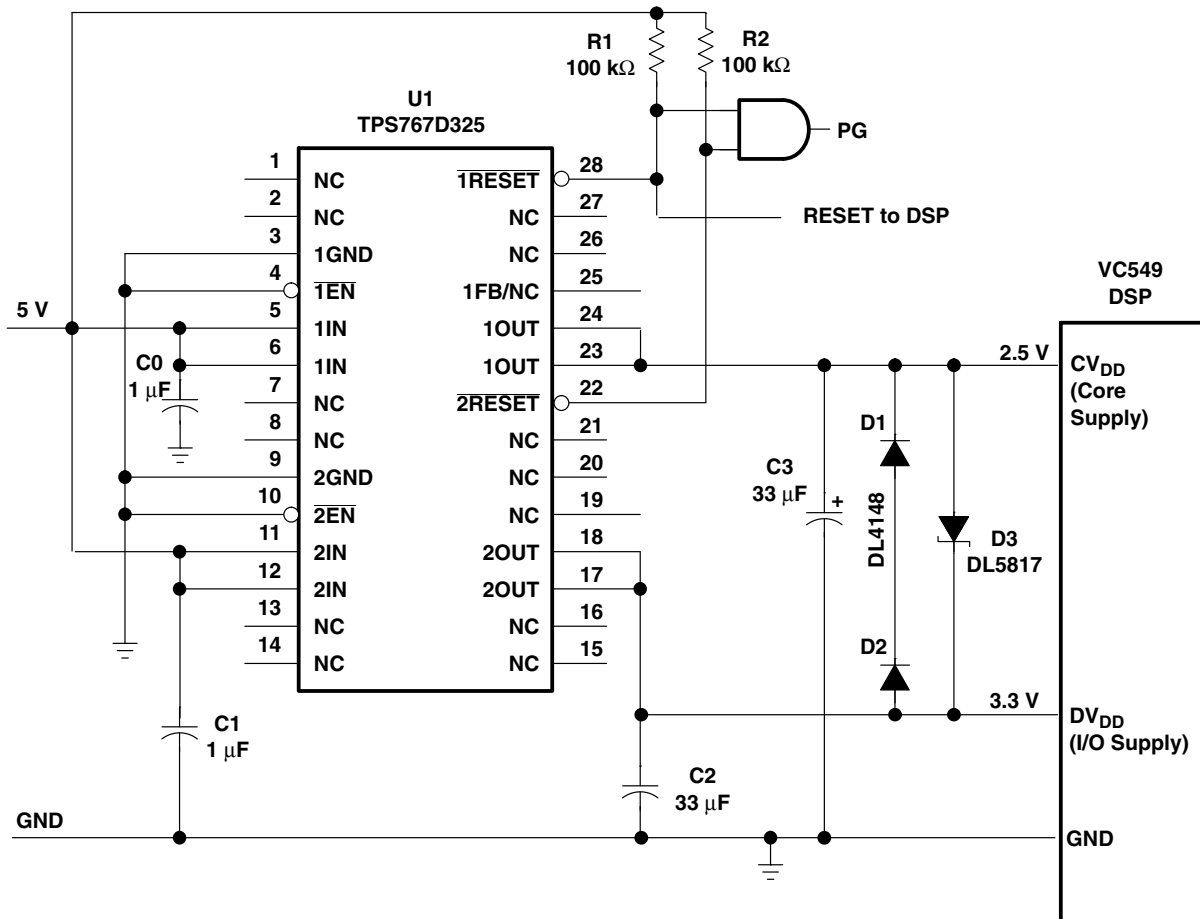


Figure 25. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents.

device operation

The TPS767D3xx features very low quiescent current, which remain virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that these devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS767D3xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range. The TPS767D3xx specifications reflect actual performance under load condition.

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device operation (continued)

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767D3xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767D3xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA . If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μs .

minimum load requirements

The TPS767D3xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network as is shown in Figure 27 to close the loop. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential. In fixed output options this pin is a no connect.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 μF to 0.1 μF) improves load transient response and noise rejection when the TPS767D3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767D3xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 60 $\text{m}\Omega$ and 1.5 Ω . Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

external capacitor requirements (continued)

When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

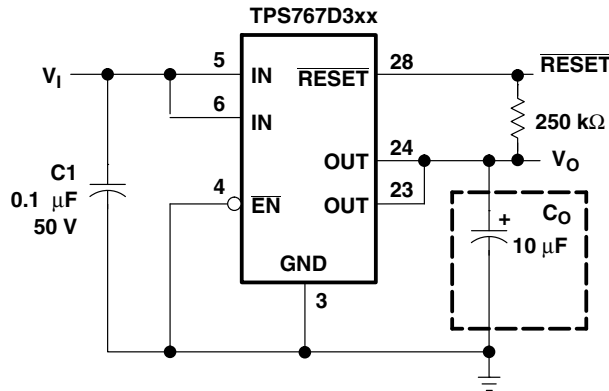


Figure 26. Typical Application Circuit (Fixed Versions) for Single Channel

programming the TPS767D301 adjustable LDO regulator

The output voltage of the TPS767D301 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2} \right) \quad (1)$$

where:

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \times R2 \quad (2)$$

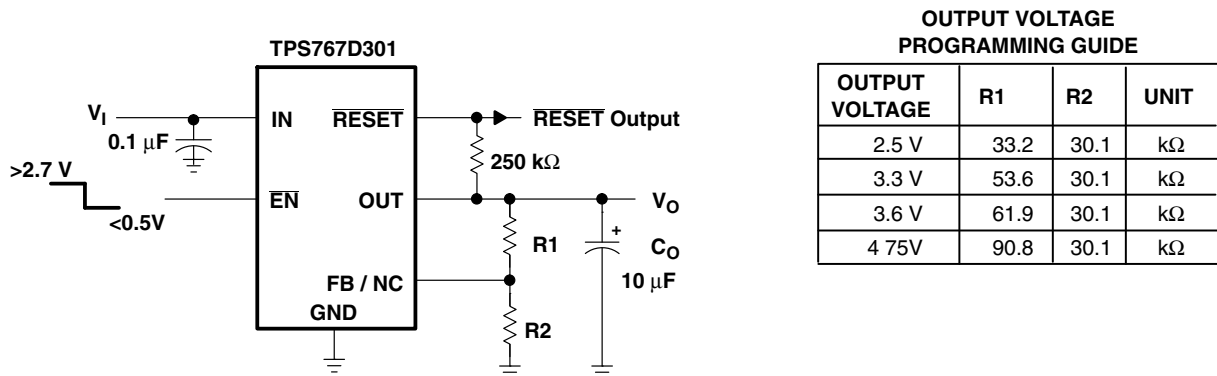


Figure 27. TPS767D301 Adjustable LDO Regulator Programming

TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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Reset indicator

The TPS767D3xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to 95% (typical) of its regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator.

regulator protection

The TPS767D3xx PMOS-pass transistor has a built-in back-gate diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767D3xx also features internal current limiting and thermal protection. During normal operation, the TPS767D3xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\max)} = \frac{T_{J\max} - T_A}{R_{\theta JA}}$$

where:

$T_{J\max}$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 27.9°C/W for the 28-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS767D301QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	767D301Q1	Samples
TPS767D318QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	767D318Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS767D301-Q1, TPS767D318-Q1, TPS767D325-Q1 :

● Catalog: [TPS767D301](#), [TPS767D318](#), [TPS767D325](#)

● Enhanced Product: [TPS767D301-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS767D301QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS767D318QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS767D301QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS767D318QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

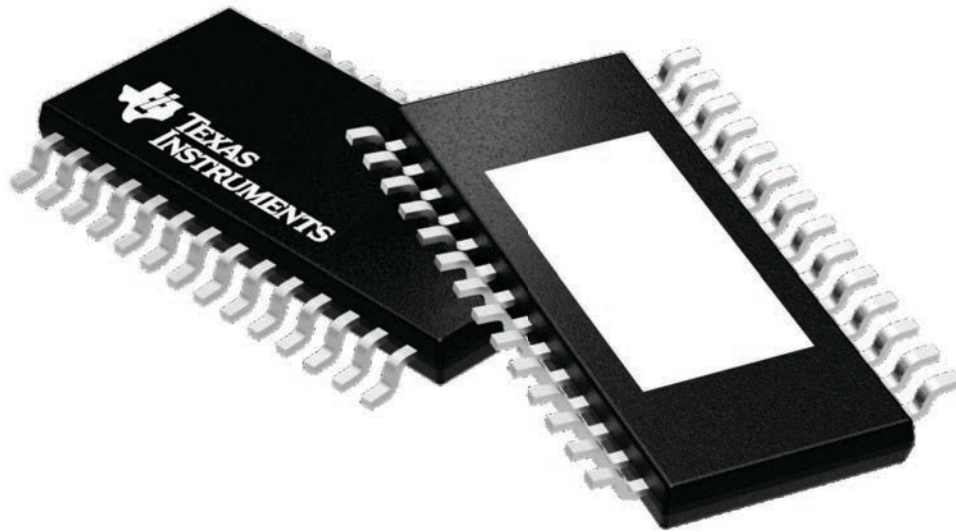
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE



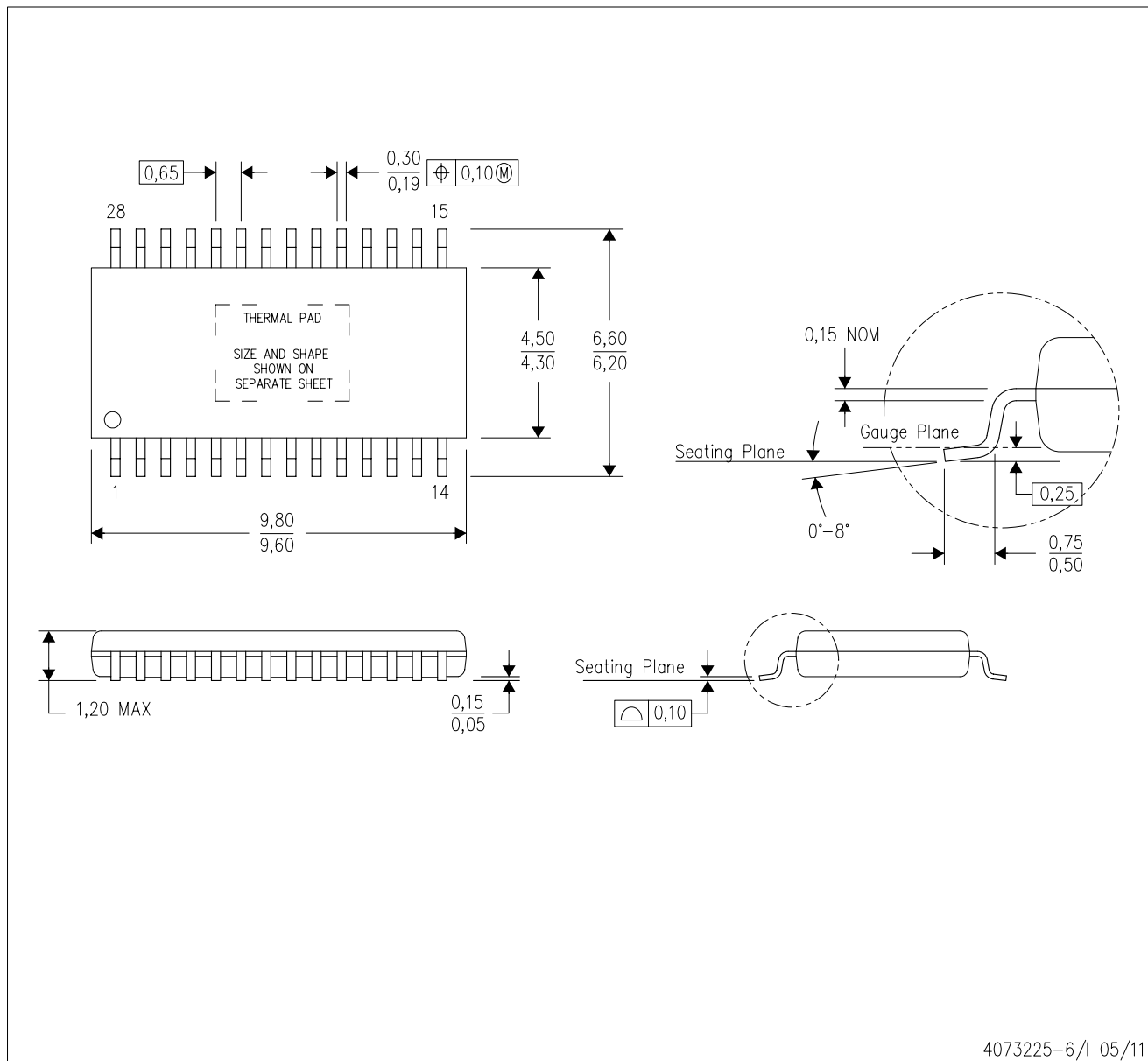
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/1 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

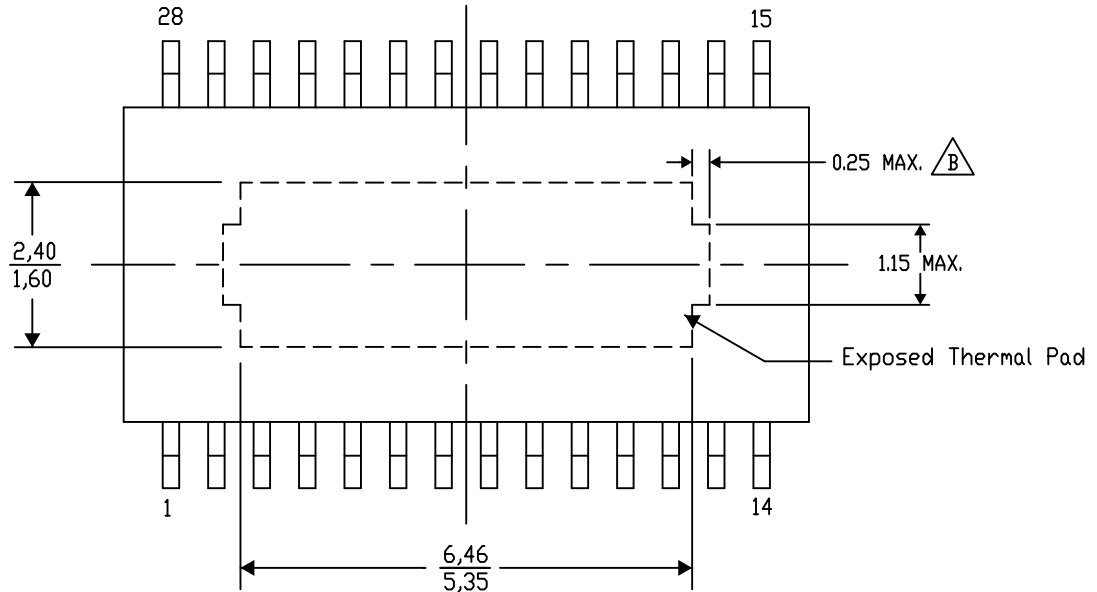
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

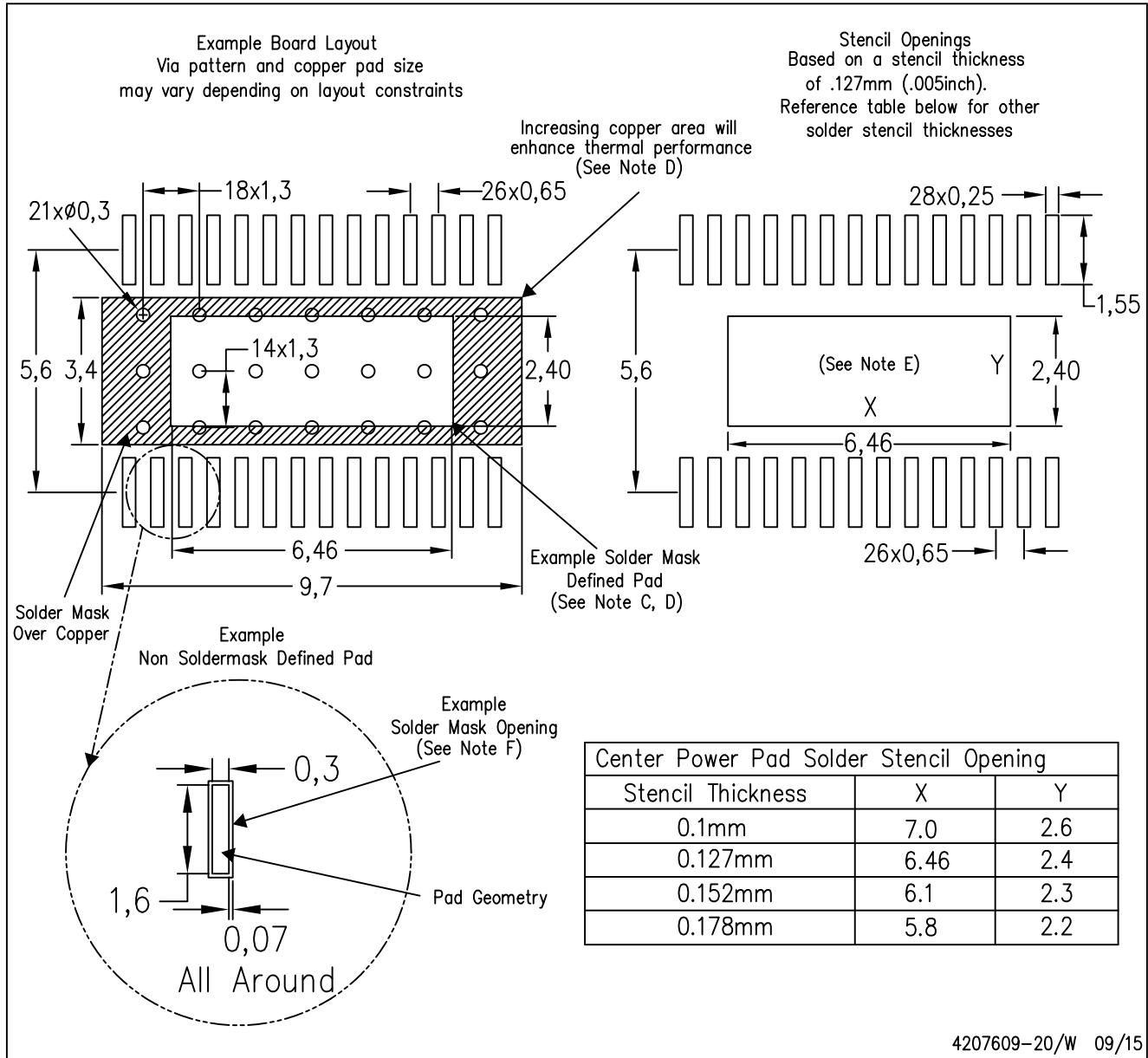
4206332-34/AO 01/16

NOTE: A. All linear dimensions are in millimeters
 $\triangle B$. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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