300-mA 40-V LOW-DROPOUT REGULATOR WITH ULTRA-LOW Iq

Check for Samples: TPS7A6301-Q1, TPS7A6333-Q1, TPS7A6350-Q1, TPS7A6401-Q1

FEATURES

- **Low Dropout Voltage**
  - **300mV at I_{OUT} = 150mA**
- **4-V to 40-V Wide Input Voltage Range With up to 45-V Transients**
- **300-mA Maximum Output Current**
- **Ultra Low Quiescent Current**
  - **$I_{QUIESCENT}$ = 35 µA (Typ) at Light Loads**
  - **I_{SLEEP} < 2µA when EN = Low**
- **Fixed (3.3V and 5V) and Adjustable (2.5V to 7V) Output Voltages**
- **Integrated Watchdog with Fault/Flag**
- **Stable with Low-ESR Ceramic Output Capacitor**
- **Integrated Power-On Reset**
  - **Programmable Delay**
  - **Open-Drain Reset Output**
- **Integrated Fault Protection**
  - **Short-Circuit/Over-Current Protection**
  - **Thermal Shutdown**
- **Low Input Voltage Tracking**
- **Thermally Enhanced 14-pin TSSOP - PWP Package and 10-pin VSON - DRK Package**

APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment Systems with Sleep Mode**
- **Body Control Modules**
- **Always ON Battery Applications**
  - **Gateway Applications**
  - **Remote Keyless Entry Systems**
  - **Immobilizers**

DESCRIPTION

The TPS7A63xx/TPS7A6401 is a series of low dropout linear voltage regulators designed for low power consumption and quiescent current less than 35 µA in light load applications. These devices feature an integrated programmable window watchdog, over-current protection and are designed to achieve stable operation even with a low-ESR ceramic output capacitor. The output voltage can be programmed using external resistors. Low voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. The Power-On Reset delay is fixed (250 µs typical), and can also be programmed by an external capacitor. Because of such features, these devices are well suited in power supplies for various automotive applications.

TYPICAL APPLICATION SCHEMATIC

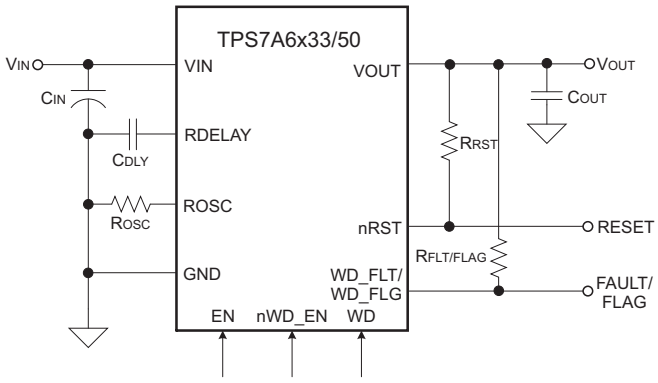


Figure 1. Fixed Output Voltage Option

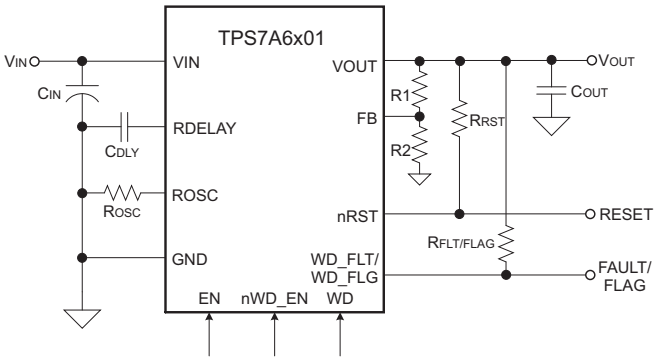


Figure 2. Adjustable Output Voltage Option

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

NO.	DESCRIPTION		VALUE	UNIT
1.1	V_{IN}, V_{EN}	Unregulated inputs(2)(3)	45	V
1.2	V_{OUT}	Regulated output	7	V
1.3	FB	Sense voltage for error amplifier(2)	7	V
1.4	ROSC	Constant voltage reference(2)	7	V
1.5	nWD_EN, WD, WD_FLAG, WD_FLT	Watchdog inputs and outputs(2)	7	V
1.6	nRST	Open drain reset output(2)	7	V
1.7	RDELAY	Reset delay timer output(2)	7	V
1.8	θ_{JP}	Thermal impedance junction to exposed pad TSSOP-PWP package	4.1	°C/W
		Thermal impedance junction to exposed pad VSON-DRK package	5.2	°C/W
1.9	θ_{JA}	Thermal impedance junction to ambient TSSOP-PWP package(4)	51	°C/W
		Thermal impedance junction to ambient VSON-DRK package(4)	51.7	°C/W
2.0	ESD	Electrostatic discharge(5)	2	kV
2.1	T_{OP}	Operating ambient temperature	125	°C
2.2	T_S	Storage temperature range	-65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3V.
(3) Absolute maximum voltage for duration less than 480ms.
(4) The thermal data is based on JEDEC standard high K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(5) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
2.1	JEDEC Standard PCB High K, JESD 51-5	14 pin TSSOP-PWP	2.45	51	1.27
2.2	JEDEC Standard PCB High K, JESD 51-5	10 pin VSON-DRK	2.41	51.7	1.25

RECOMMENDED OPERATING CONDITIONS

NO.	DESCRIPTION		MIN	MAX	UNIT
3.1	V_{IN}, V_{EN}	Unregulated input voltage	4	40	V
3.2	nRST, RDELAY, nWD_EN, WD_FLT(1), WD_FLAG(2), WD, FB(3)	Low voltage input/output	0	5.25	V
3.3	T_J	Operating junction temperature range	-40	150	°C

(1) Applicable for TPS7A63xx only
(2) Applicable for TPS746401 only
(3) Applicable for TPS7A63/401 only

ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	V_{IN}	Input voltage	V_{OUT} = 2.5V to 7V, I_{OUT} = 1mA	V_{OUT} + 0.3V		40	V
4.2	$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2V to 18V, V_{EN} = 5V, I_{OUT} = 0.01mA to 0.75mA		35		µA
4.3	I_{SLEEP}	Sleep/shutdown current	V_{IN} = 8.2V to 18V, V_{EN} < 0.8V, I_{OUT} = 0mA (no load), T_A = 125°C			3	µA
4.4	$V_{IN-UVLO}$	Under voltage lock out voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
4.5	$V_{IN(POWERUP)}$	Power up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
5. Device Enable Input (EN pin)							
5.1	V_{IL}	Logic input low level		0		0.8	V
5.2	V_{IH}	Logic input high level		2.5		40	V
6. Regulated Output Voltage (VOUT pin)							
6.1	V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3V, 5V or a programmed value), I_{OUT} = 10mA to 200mA, V_{IN} = V_{OUT} + 1V to 16V	-2		2	%
6.2	$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 5V			15	mV
			V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 3.3V			20	mV
6.3	$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10mA to 200mA, V_{IN}= 14V, V_{OUT} = 5V			25	mV
			I_{OUT} = 10mA to 200mA,V_{IN} = 14V, V_{OUT} = 3.3V			35	mV
6.4	$V_{DROPOUT}$	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 200mA			500	mV
			I_{OUT} = 150mA			300	mV
6.5	R_{SW}(1)	Switch resistance	VIN to VOUT resistance			2	Ω
6.6	I_{OUT}	Output current	V_{OUT} in regulation	0		200	mA
			[V_{OUT} in regulation, V_{OUT} = 3.3V, V_{IN} = 6V](2)	0		300	mA
6.7	I_{CL}	Output current limit	V_{OUT} = 0V (VOUT pin is shorted to ground)	350		1000	mA

(1) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} drops by 100mV from the programmed value (of V_{OUT}) at specified loads.
(2) Design Information - not tested; specified by characterization.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.8	PSRR(3)	Power supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200mA, frequency = 100 Hz, V_{OUT} = 5V and V_{OUT} = 3.3V		60		dB
			$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 200mA, frequency = 150 kHz, V_{OUT} = 5V and V_{OUT} = 3.3V		30		
7. Reset (nRST pin)							
7.1	V_{OL}	Reset pulled low	I_{OL} = 5mA			0.4	V
7.2	I_{OH}	Leakage current	Reset pulled to VOUT through 5kΩ resistor			1	µA
7.3	$V_{TH(POR)}$	Power-On Reset threshold	V_{OUT} power up above internally set tolerance, V_{OUT} = 5V	4.5	4.65	4.77	V
			V_{OUT} power up above internally set tolerance, V_{OUT} = 3.3V		3.07		
7.4	UV_{THRES}	Reset threshold	V_{OUT} falling below internally set tolerance, V_{OUT} = 5V	4.5	4.65	4.77	V
			V_{OUT} falling below internally set tolerance, V_{OUT} = 3.3V		3.07		
7.5	t_{POR}(2)	Power-On Reset delay	C_{DLY} = 100pF		300		µs
			C_{DLY} = 100nF		300		ms
7.6	$t_{POR-PRESET}$	Internally preset Power-On Reset delay	C_{DLY} not connected, V_{OUT} = 5V and V_{OUT} = 3.3V		250		µs
7.7	$t_{DEGLITCH}$	Reset deglitch time			5.5		µs
8. Reset Delay (RDELAY pin)							
8.1	$V_{TH(RDELAY)}$	Threshold to release nRST high	Voltage at RDELAY pin is ramped up		3	3.3	V
8.2	I_{DLY}	Delay capacitor charging current		0.75	1	1.25	µA
8.3	I_{OL}	Delay capacitor discharging current	Voltage at RDELAY pin = 1V	5			mA
9. Current Voltage Reference (ROSC pin)							
9.1	V_{ROSC}	Voltage Reference		0.95	1	1.05	V
10. Watchdog Fault/ Flag Output (WD_FLT/ WD_FLAG pin)							
10.1	V_{OL}	Logic output low level	I_{OL}= 5 mA			0.4	V
10.2	I_{OH}	Leakage current	WD_FLT/WD_FLG pulled to V_{OUT} through 5 kΩ resistor			1	µA
11. Watchdog Enable Input (nWD_EN pin)							
11.1	V_{IL}	Logic input low level				0.8	V
11.2	V_{IH}	Logic input high level	5.25 V < V_{DD} < 3 V	2.5			
12. Watchdog Input Pulse (WD pin)							
12.1	V_{IL}	Logic input low level				0.8	V
12.2	V_{IH}	Logic input high level	5.25 V < V_{DD} < 3 V	2.5			
12.3	t_{WD}	Wactchdog window width	R_{OSC}=10kΩ ± 1%		10		mS
			R_{OSC}=20kΩ ± 1%		20		
12.4	t_{WD-tol}	Tolerance of watchdog period using external resistor	Excludes tolerance of R_{OSC} (external resistor connected to ROSC pin)	-10		10	%
12.5	$t_{WD-DEFAULT}$	Default watchdog period	External resistor not connected, ROSC pin is floating/ open	108	164	254	ms
12.6	$t_{WD-HOLD}$	Minimum pulse width for resetting watch dog timer			1.65		µs

(3) Specified by design - not tested

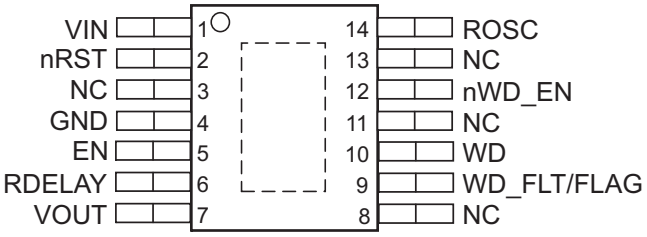
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

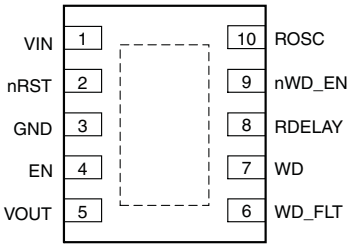
NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
13. Operating Temperature Range							
13.1	T_J	Operating junction temperature		-40		150	ºC
13.2	$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
13.3	T_{HYST}	Thermal shutdown hysteresis			10		ºC

DEVICE INFORMATION

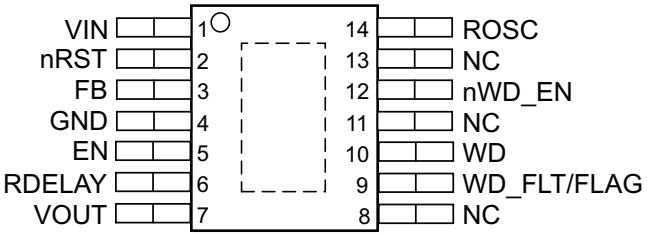
TSSOP PWP PACKAGE (TOP VIEW)
Fixed Output Voltage Option



VSON DRK PACKAGE (TOP VIEW)
Fixed Output Voltage Option



TSSOP PWP PACKAGE (TOP VIEW)
Adjustable Output Voltage Option



PIN FUNCTIONS

PIN NO.		PIN NAME	TYPE	DESCRIPTION
PWP	DRK			
1	1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	2	nRST	O	Reset pin: This is an open drain reset output pin with an external pullup resistor connected to VOUT pin.
3	-	FB	I	Feedback pin (only applicable for TPS7A6x01): Sense voltage for error amplifier.
		NC	-	Not connected (only applicable for TPS7A6x33/50)
4	3	GND	I/O	Ground pin: This is signal ground pin of the IC.
5	4	EN	I	Chip enable pin: This is a high voltage tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. This input can be connected to VIN terminal for self bias applications. If this pin is not connected, the device will stay disabled.
6	8	RDELAY	O	Reset delay timer pin: This pin is used to program the reset delay timer using an external capacitor (C_{DLY}) to ground.
7	5	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3 V or 5 V or a programmed value) pin with a limitation on maximum output current. For devices with adjustable output voltage (TPS7A6x01), an external resistor network is connected to program the output voltage. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and GND pin.
8	-	NC	-	Not connected
9	6	WD_FLT	O	Watchdog Fault pin (for TPS7A63xx only): This is an active low fault output pin with an external pullup resistor connected to VOUT pin.
		WD_FLAG	O	Watchdog Flag pin (for TPS746401 only): This is an active high latched fault (i.e flag) output pin with an external pullup resistor connected to VOUT pin.
10	7	WD	I	Watchdog Service pin: This is an input pin to provide service signal to the watchdog.
11	-	NC	-	Not connected
12	9	nWD_EN	I	Watchdog Enable pin: A high input to this pin disables the watchdog and vice versa. This is an active low input pin with an internal pulldown. If this pin is not connected and left floating, the watchdog will stay enabled. An external microcontroller can pull this pin high momentarily to disable and reinitialize the watchdog.
13	-	NC	-	Not connected
14	10	ROSC	O	ROscillator pin: This pin is used to program the internal oscillator frequency (and hence the width of watchdog window) by connecting an external resistor to ground.

FUNCTIONAL BLOCK DIAGRAMS

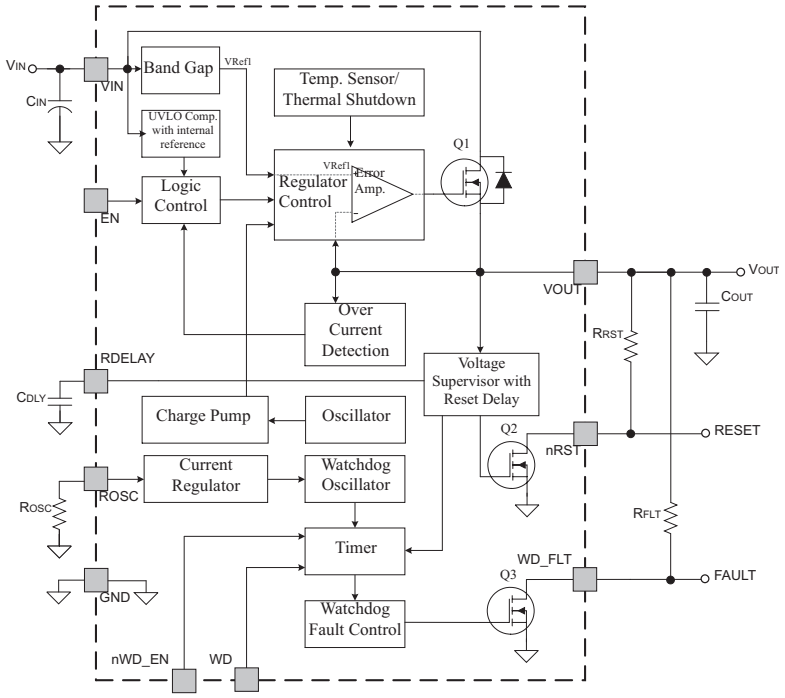


Figure 3. TPS7A6333/50 (Fixed Output Voltage with FAULT Output)

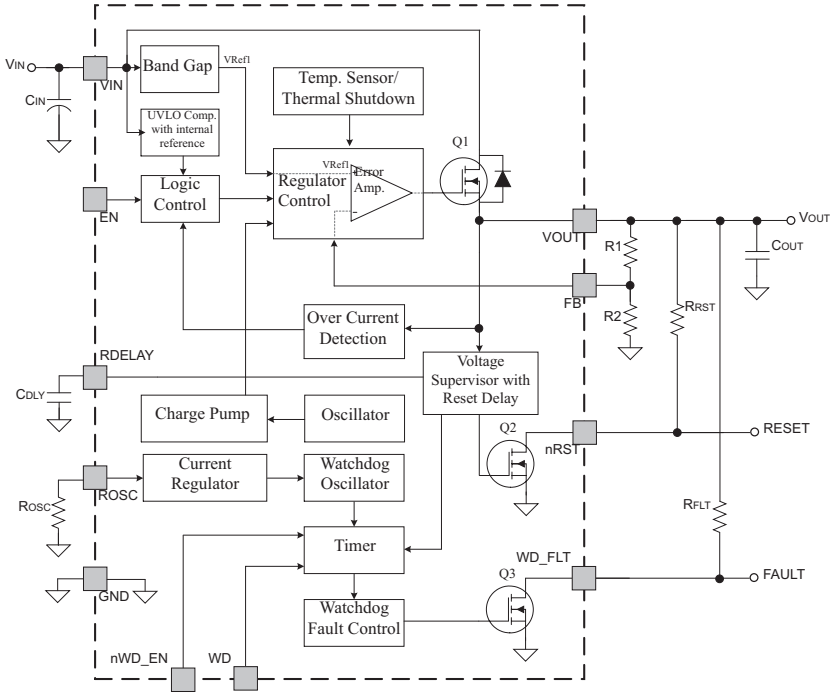


Figure 4. TPS7A6301 (Adjustable Output Voltage with FAULT Output)

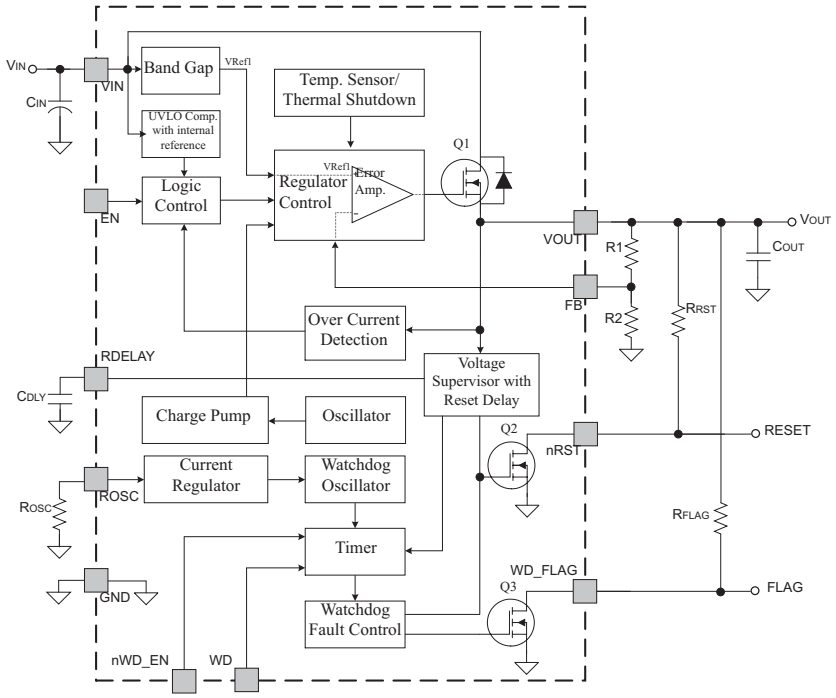


Figure 5. TPS7A6401 (Adjustable Output Voltage with FLAG Output)

TYPICAL CHARACTERISTICS

Graphs shown in 'Typical Characteristics' section for unreleased devices are for preview only.

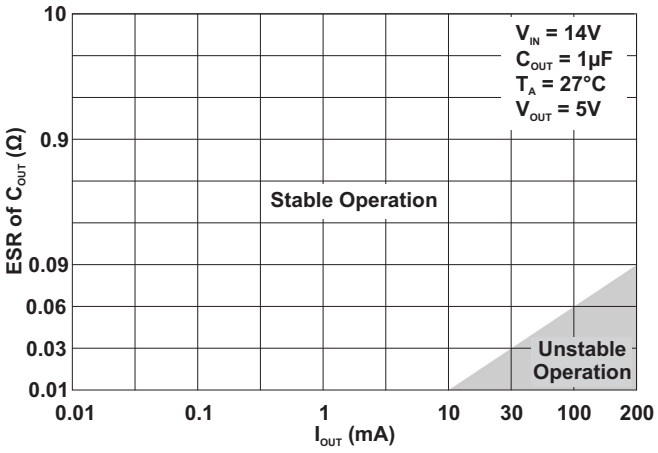


Figure 6. ESR vs Load Current

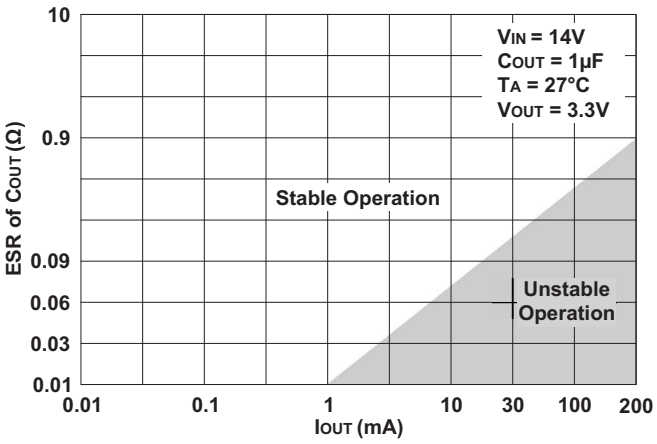


Figure 7. ESR vs Load Current

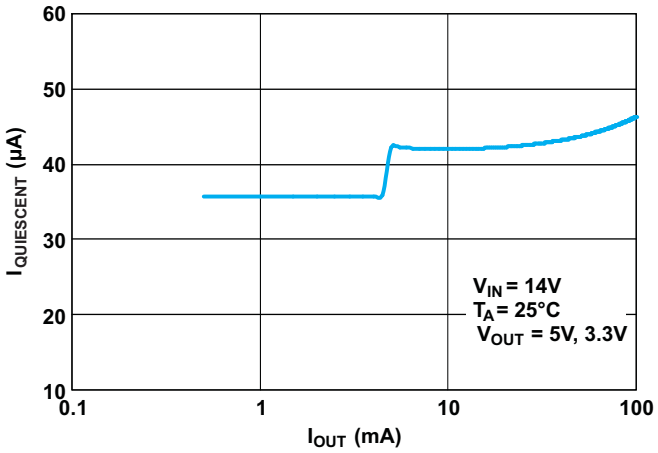


Figure 8. Quiescent Current vs Load Current

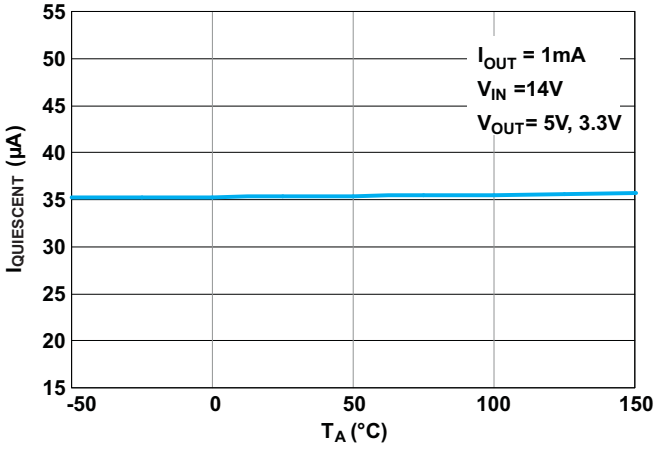


Figure 9. Quiescent Current vs Ambient Air Temperature

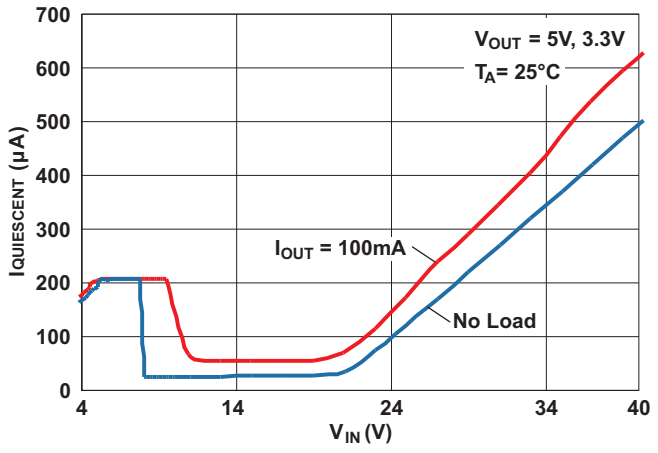


Figure 10. Quiescent Current vs Input Voltage

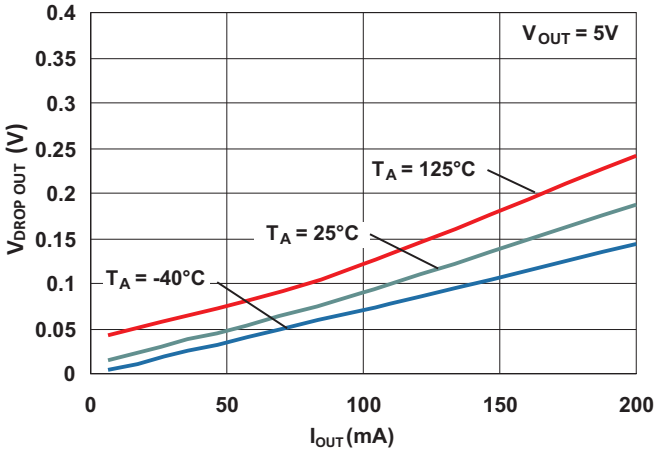


Figure 11. Drop Out Voltage vs Load Current(1)

(1) Drop out voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, if output voltage is programmed to be 5V, the drop out voltage is measured when the output voltage drops down to 4.9V from 5V.)

TYPICAL CHARACTERISTICS (continued)

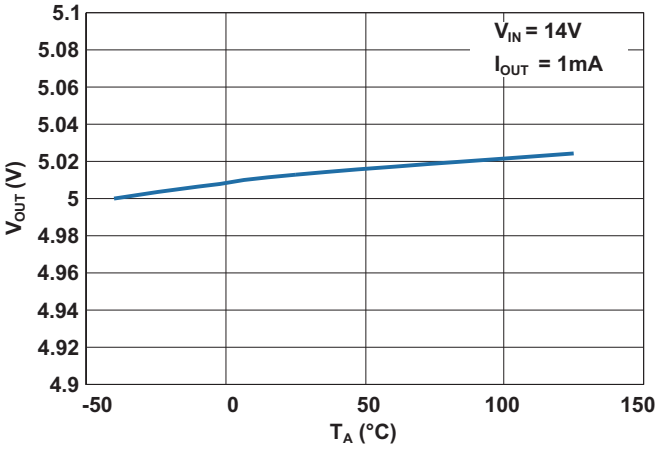


Figure 12. Output Voltage vs Ambient Air Temperature (V_{OUT} Set to 5 V)

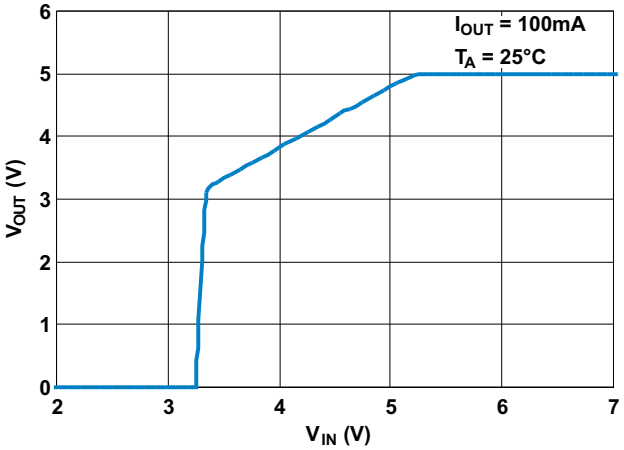


Figure 13. Output Voltage vs Input Voltage (V_{OUT} Set to 5 V)

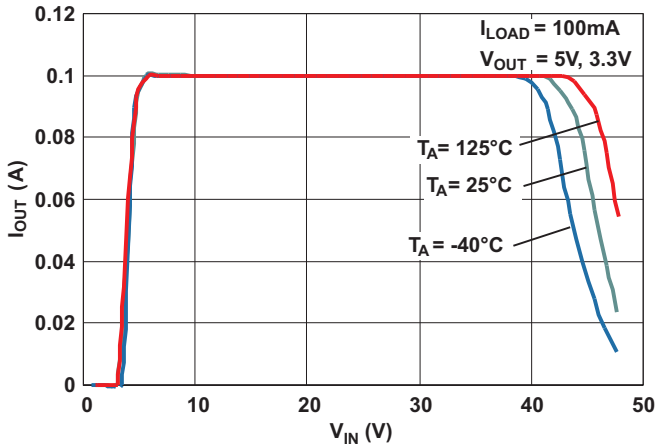


Figure 14. Output Voltage vs Input Voltage

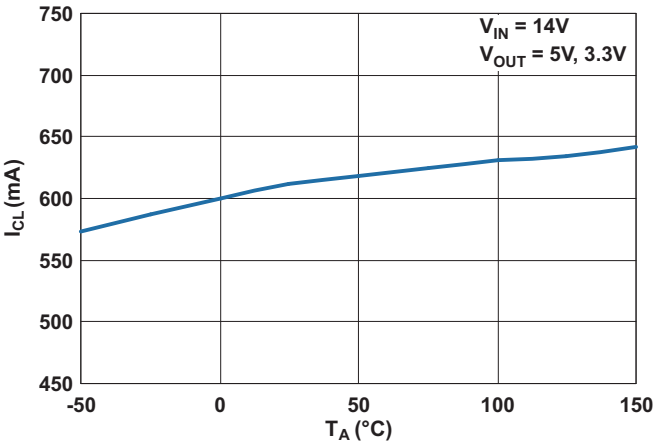


Figure 15. Output Current Limit vs Ambient Air Temperature

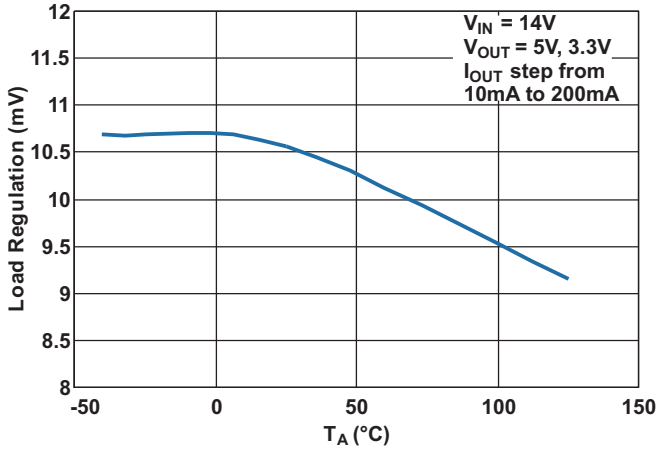


Figure 16. Load Regulation vs Ambient Air Temperature

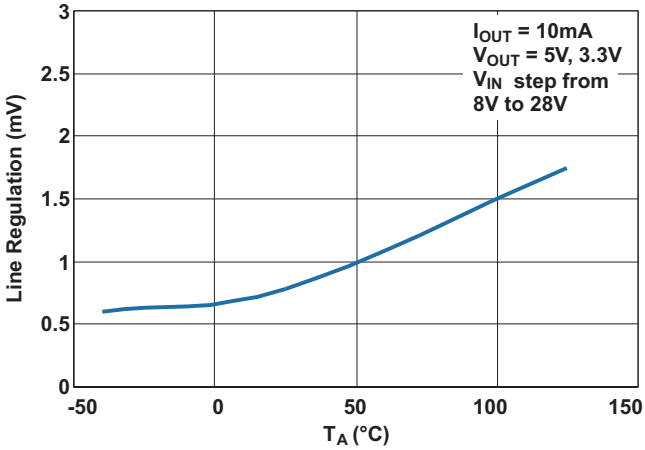


Figure 17. Line Regulation vs Ambient Air Temperature

TYPICAL CHARACTERISTICS (continued)

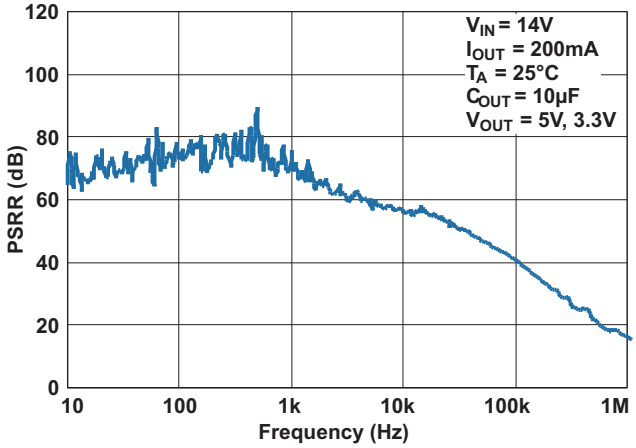


Figure 18. PSRR at Heavy Load Current

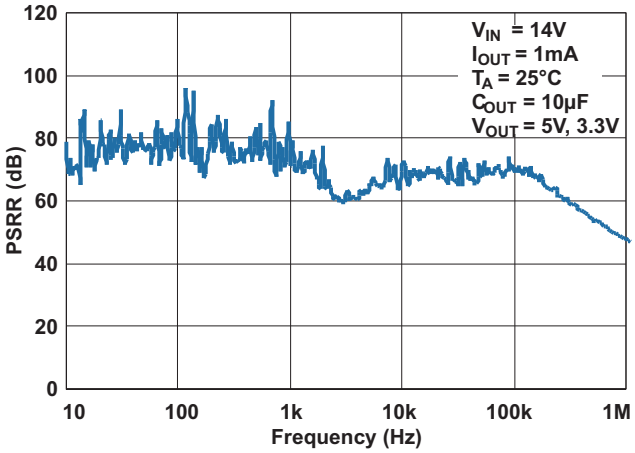


Figure 19. PSRR at Light Load Current

DETAILED DESCRIPTION

TPS7A63/401 is a series of monolithic low dropout linear voltage regulators with integrated watchdog and reset functionality. These voltage regulators are designed for low power consumption and quiescent current less than 25µA in light load applications. Because of an programmable reset delay (also called Power-On Reset delay), these devices are well suited in power supplies for microprocessors/ microcontrollers.

These devices are available in two fixed and adjustable output voltage versions as follows:

- Fault (WD_FLT) output version: TPS7A63xx
- Flag (WD_FLAG) output version: TPS7A6401

The following section describes the features of TPS7A63/401 voltage regulators in detail.

Power Up, Reset Delay and Reset Output

During power up, the regulator incorporates a protection scheme to limit the current through pass element and output capacitor. When the input voltage exceeds a certain threshold ($VIN_{(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 20.

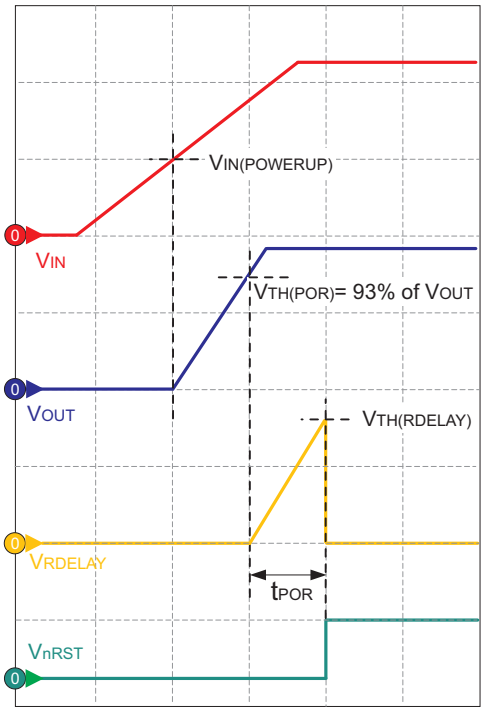


Figure 20. Power Up and Conditions for activation of Reset

Reset delay is implemented when the device starts up to indicate that output voltage is stable and in regulation, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration.

When the output voltage reaches power on reset threshold ($V_{TH(POR)}$) level i.e. 93% of regulated output voltage (3.3V or 5V, or a programmed value), a constant output current charges an external capacitor (C_{DLY}) to an internal threshold ($V_{TH(RDELAY)}$) voltage level. Then, nRST is asserted high and C_{DLY} is discharged through an internal load. This allows C_{DLY} to charge from approximately 0V during the next power cycle.

The reset delay time can be programmed by connecting an external capacitor (C_{DLY} ,100 pF to 100 nF) to RDELAY pin. The delay time is given by Equation 1:

$$t_{POR} = \frac{CDLY \times 3}{1 \times 10^{-6}} \quad (1)$$

Where,

t_{POR} = reset delay time in seconds
C_{DLY} = reset delay capacitor value in farads

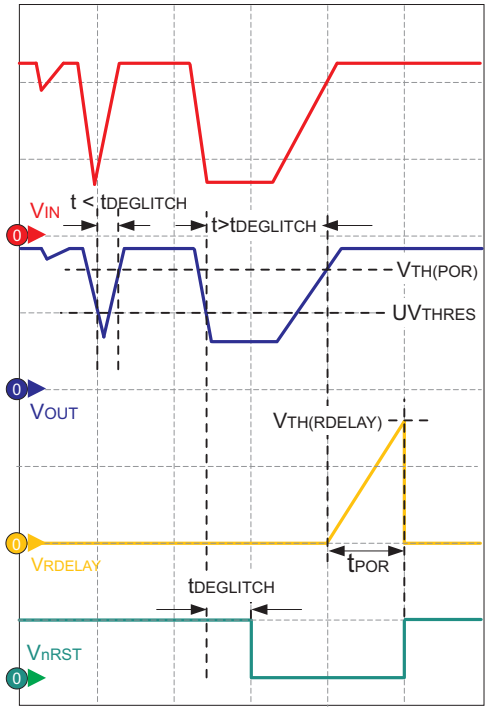


Figure 21. Reset Delay and Deglitch Filter

As shown in Figure 21, if the regulated output voltage falls below 93% of the set level, nRST is asserted low after a short de-glitch time of approximately 5.5µs (typical). In case of negative transients in the input voltage (V_{IN}), the reset signal will be asserted low only if the output (V_{OUT}) drops and stays below the reset threshold level ($V_{TH(POR)}$) for more than deglitch time ($t_{DEGLITCH}$). This is shown in Figure 21 and Figure 24. While nRST is low, if the input voltage resumes to the nominal operating voltage, normal power up sequence will be followed. nRST will be asserted high, only if the output voltage exceeds the reset threshold voltage ($V_{TH(POR)}$) and the reset delay time (t_{POR}) has elapsed.

Adjustable Output Voltage

The regulated output voltage (V_{OUT}) can be programmed by connecting external resistors to FB pin. The feedback resistor values can be calculated using Equation 2.

$$V_{OUT} = V_{REF}\left[1 + \frac{R1}{R2}\right] \quad (2)$$

Where,

V_{OUT}= desired output voltage

V_{REF} = reference voltage (V_{REF}= 1.23 V typically)

R1, R2 = feedback resistors (see Figure 5)

The overall tolerance of the regulated output voltage is given by Equation 3.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[\frac{R1}{R1 + R2}\right]\left[tol_{R1} + tol_{R2}\right] \quad (3)$$

Where,

tol_{VOUT} = tolerance of output voltage

tol_{VREF} = tolerance of internal reference voltage (tol_{VREF} = ± 1.5% typically)

tol_{R1},tol_{R2} = tolerance of feedback resistors R1, R2

For a tighter tolerance on V_{OUT}, lower-value feedback resistors can be selected. It is recommended to select feedback resistors such that the sum of R1 and R2 is between 20kΩ and 200kΩ.

Chip Enable

These devices have a high voltage tolerant EN pin that can be used to enable and disable them from an external microcontroller or a digital control circuit. A high input to this pin activates the device and turns the regulator on. This input can also be connected to VIN terminal for self bias applications. An internal pulldown resistor is connected to this pin, and therefore if this pin is left unconnected, the device will stay disabled.

Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry shall not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 22 and Figure 23 shows typical switching thresholds for the charge pump at light (I_{OUT} < ~2mA) and heavy (I_{OUT} > ~2mA) loads respectively.

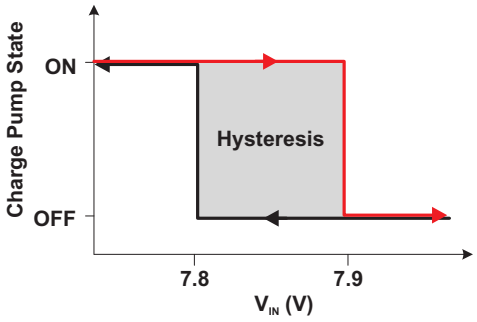


Figure 22. Charge Pump Operation at Light Loads

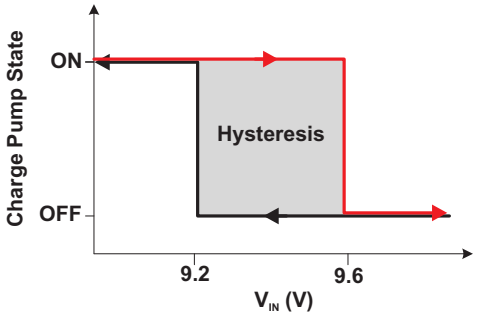


Figure 23. Charge Pump Operation at Heavy Loads

Low Power Mode

At light loads and high input voltages (V_{IN}>~8V such that charge pump is off) the device operates in Low Power Mode and the quiescent current consumption is reduced to 25µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < ~2mA (Light load)	250 µA	35 µA (Low Power Mode)
I_{OUT} > ~2mA (Heavy load)	280 µA	70 µA

Under Voltage Shutdown

These devices have an integrated under voltage lock out (UVLO) circuit to shutdown the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$). This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds $V_{IN(POWERUP)}$ level. This is shown in Figure 24.

Low Voltage Tracking

At low input voltages the regulator drops out of regulation, the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}). This is shown in Figure 24. This feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions. This is shown in Figure 24.

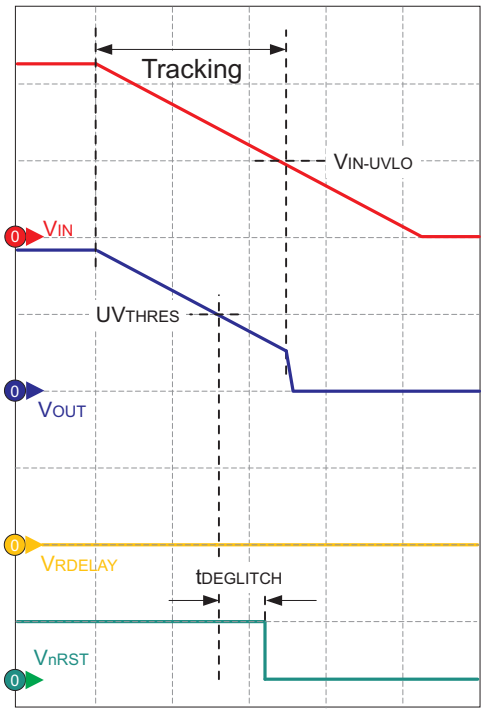


Figure 24. Low Voltage Tracking and Under Voltage Lock Out

Integrated Fault Protection

These devices feature an integrated fault protection to make them ideal for use in automotive applications. In order to keep them in safe area of operation during certain fault conditions, internal current limit protection and current limit fold back are used to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short circuit condition on the output; current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed TSD trip point. If the junction temperature exceeds TSD trip point, the output is turned off. When the junction temperature falls below TSD trip point, the output is turned on again. This is shown in Figure 25.

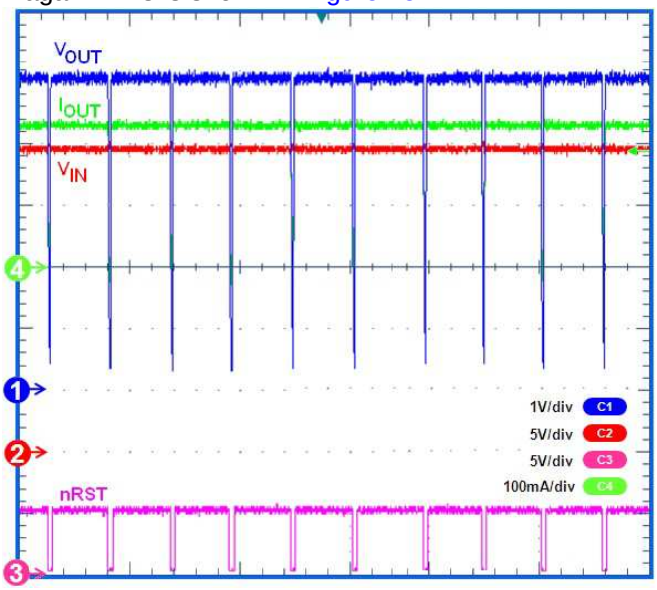


Figure 25. Thermal Cycling Waveform for TPS7A6x50 (V_{IN}= 24V, I_{OUT}= 200mA, V_{OUT}= 5V)

INTEGRATED WINDOW WATCHDOG

These devices have an integrated watchdog with fault (WD_FLT) and flag (WD_FLAG) output options. Both device options are available in fixed and adjustable output versions. The watchdog operation, service fault conditions and difference between fault (TPS7A63xx) and flag (TPS746401) output versions are described below.

Programmable Window Watchdog

The width of the watchdog window can be programmed by connecting an external resistor (R_{OSC}) to ground at ROSC pin. The current through the resistor sets the clock frequency of the internal oscillator. The user can adjust the width of watchdog

window (i.e watchdog timer period) by changing the resistor value. The width of watchdog window and duration of fault output are multiples of internal oscillator frequency and are given by following equations:

$$t_{WD} = 10^{-6} \times R_{OSC} = 5000 \times 1/f_{OSC} \quad (4)$$

$$t_{WD\_OUT} = 1/f_{OSC} \quad (5)$$

$$t_{CW} = t_{OW} = 1/2\ t_{WD} \quad (6)$$

Where,

t_{WD} = width of watchdog window
R_{OSC} = resistor connected at ROSC pin
t_{WD_OUT} = width of fault output
f_{OSC} = frequency of internal oscillator
t_{CW} = width of close window
t_{OW} = width of open window

As shown in Figure 26, each watchdog window consists of an open window and a close window, and their width is approximately 50% of the watchdog window. However, there is an exception to this; the first open window after watchdog initialization is eight times the width of watchdog window. All open windows except the one after watchdog initialization are one-half the width of watchdog window. Upon initialization, the watchdog must be serviced (by software/ external microcontroller etc.) only during an open window. If the watchdog is serviced during a close window, or not serviced during a open window, a watchdog fault condition is created.

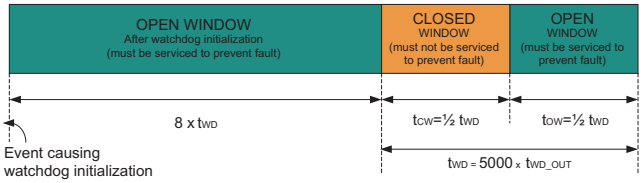


Figure 26. Watchdog Window Duration

Watchdog Enable

The watchdog can be enabled and disabled by an external microcontroller or a digital circuit by applying appropriate signal to nWD_EN pin. A low input to this pin turns the watchdog on. An internal pulldown resistor is connected to this pin, and therefore if this pin is left unconnected, watchdog will stay enabled.

Watchdog Service Signal

In order for watchdog service signal (WD) to correctly service an open window, the service signal must stay high for least t_{WD_HOLD} duration. The recommended value of t_{WD_HOLD} is given by Equation 7:

$$t_{WD\_HOLD} = 3x\ t_{WD\_OUT} \quad (7)$$

Watchdog Fault Outputs

WD_FLT pin and WD_FLAG pin are fault output terminals for TPS7A63xx and TPS7A6401 devices respectively. These fault outputs are typically pulled high to regulated output supply. In case of a watchdog fault condition, for TPS7A63xx, WD_FLT is momentarily pulled low for t_{WD_OUT} duration. Whereas in case of TPS746401, WD_FLAG is latched high and nRST is momentarily pulled low for t_{WD_OUT} duration.

Watchdog Initialization

Upon power up and during normal operation, the watchdog is initialized under the following conditions shown in Table 2. The normal operation of watchdog for WD_FLT and WD_FLAG output device options are shown in Figure 27 and Figure 28 respectively.

Table 2. Conditions for Watchdog Initialization

Edge	What causes watchdog to initialize?	TPS7A63xx (FAULT Option)	TPS746401 (FLAG Option)
	Rising edge of nRST (when V_{OUT} exceeds $V_{TH(POR)}$) while the watchdog is already enabled. For example, during soft power up.	✓	✓
	Falling edge of nWD_EN while the nRST is already high. For example, when microprocessor enables the watchdog after the device is powered up.	✓	✓
	Rising edge of WD_FLT while the nRST is already high and watchdog is enabled. For example, right after when a closed window is serviced.	✓	X

Watchdog Operation

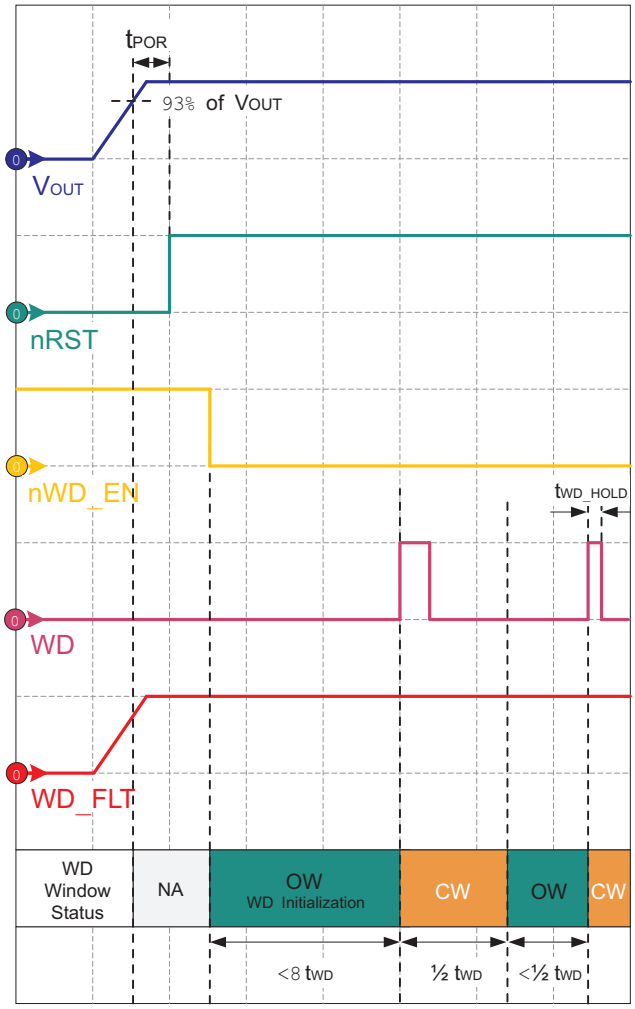


Figure 27. Power Up, Initialization, and Normal Operation for TPS7A63xx

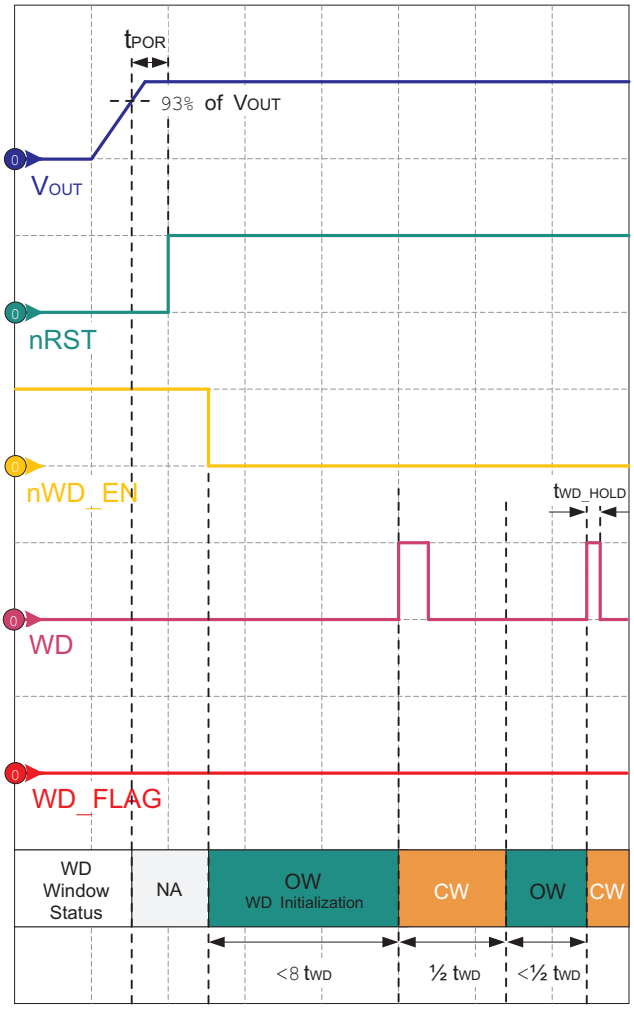


Figure 28. Power Up, Initialization, and Normal Operation for TPS7A6401

Figure 27 shows watchdog initialization and operation for TPS7A63xx. After output voltage is in regulation and reset is asserted high (clearly chip enable pin is high), the watchdog is enabled when nWD_EN (watchdog enable pin) is externally pulled low. This causes watchdog initialize and wait for a service signal during first open window for 8 x t_{WD} duration. When the service signal is applied to WD pin during the first open window, watchdog counter resets and a close window starts. To prevent the fault condition from occuring, the watchdog must not be serviced during the close window. The watchdog must be serviced during the following open window to prevent fault condition from occurring. The fault output (WD_FLT) is externally pulled up to VOUT (typically) and stays high as long as the watchdog is properly serviced and there is no fault condition.

Figure 28 shows watchdog initialization and operation for FLAG output version (TPS7A6401). The fault output (WD_FLAG) is externally pulled up to VOUT (typically) and stays low as long as the watchdog is properly serviced and there is no fault condition.

Likewise, when the watchdog is enabled before the device is powered on (i.e. nWD_EN pin is pulled low before power up), the watchdog will initialize as soon as output voltage is in regulation and reset is asserted high (see Table 2 for Conditions for Watchdog Initialization).

Watchdog Fault Conditions

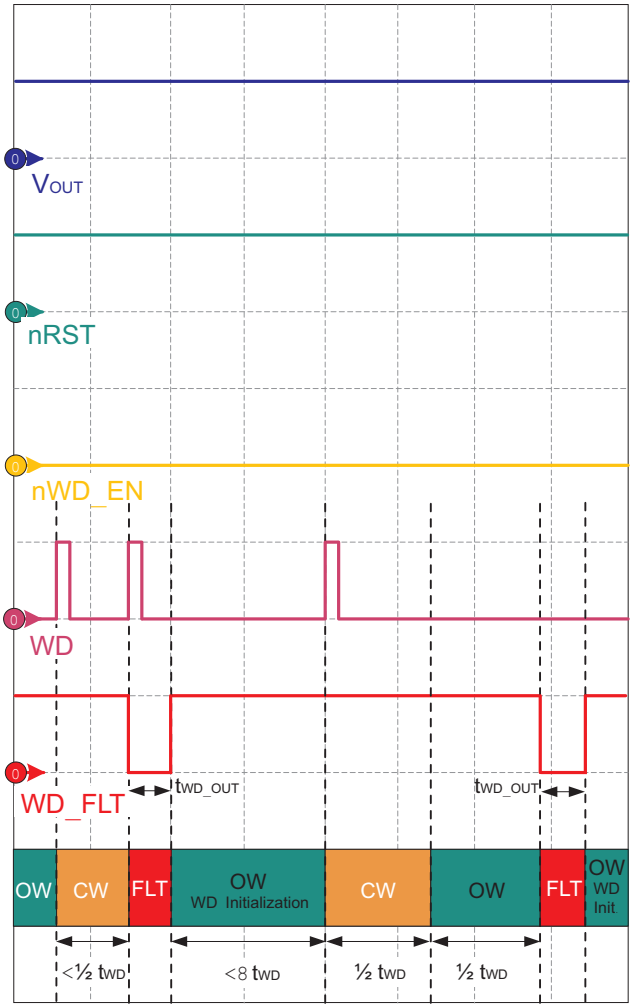


Figure 29. Watchdog Service Fault Conditions for TPS7A63xx

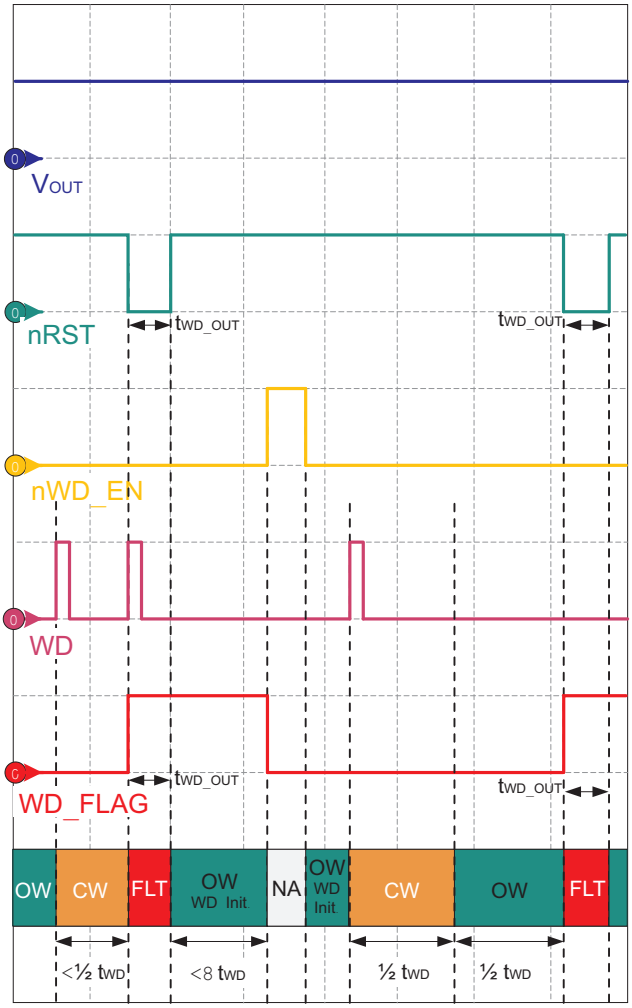


Figure 30. Watchdog Service Fault Conditions for TPS7A6401

For both device options, a watchdog fault condition occurs in following (non-exhaustive) cases:

i) When watchdog is serviced during a close window

ii) When watchdog is not serviced during an open window (this open window could be the one after watchdog initialization, or the one following a close window).

As shown in Figure 29, for TPS7A63xx the first watchdog fault is registered when watchdog is serviced during a close window. This causes watchdog fault pin (WD_FLT) to go low temporarily for t_{WD_OUT} duration. Following the fault, the watchdog reinitializes. Likewise, the second fault is registered when the watchdog is not serviced during an open window (following a close window). Again, the fault pin (WD_FLT) is asserted low for t_{WD_OUT} duration.

As shown in Figure 30, for TPS746401 the first watchdog fault is registered when watchdog is serviced during a close window. This causes watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, nRST pin goes low temporarily for t_{WD_OUT} duration. WD_FLAG remains high until the watchdog is disabled and re-enabled by toggling nWD_EN pin or watchdog is serviced properly (while nWD_EN is low and nRST is high). The second fault is registered when the watchdog is not serviced during an open window (following a close window). While WD_FLAG is high (i.e. during a fault condition), if the watchdog stays enabled, and reset is high; a watchdog service signal can also bring WD_FLAG low (about 5 µs after watchdog is serviced).

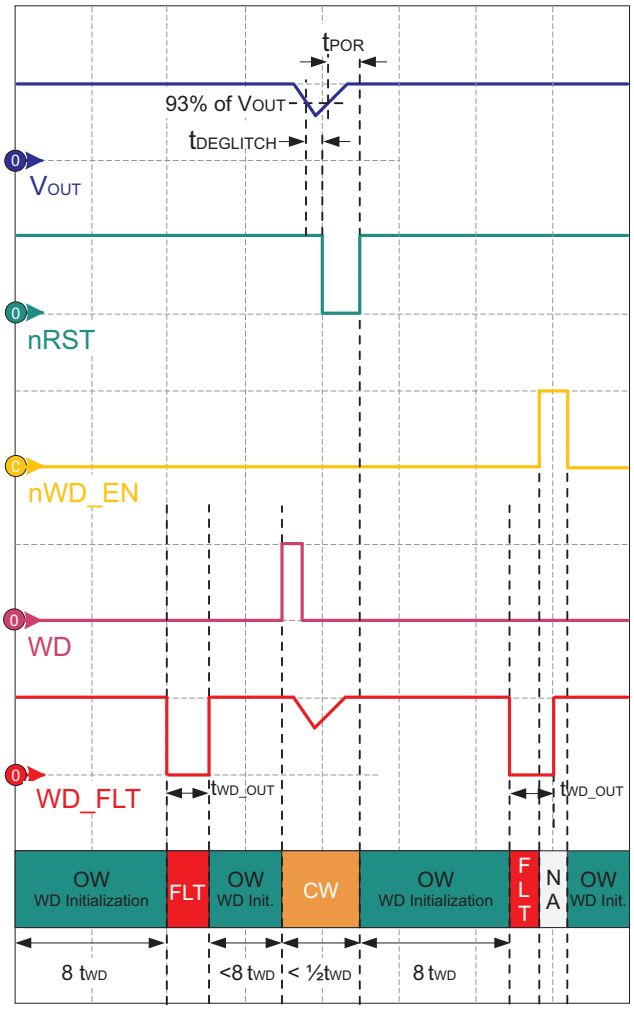


Figure 31. Watchdog Fault during Initialization, and Reinitialization during Reset for TPS7A63xx

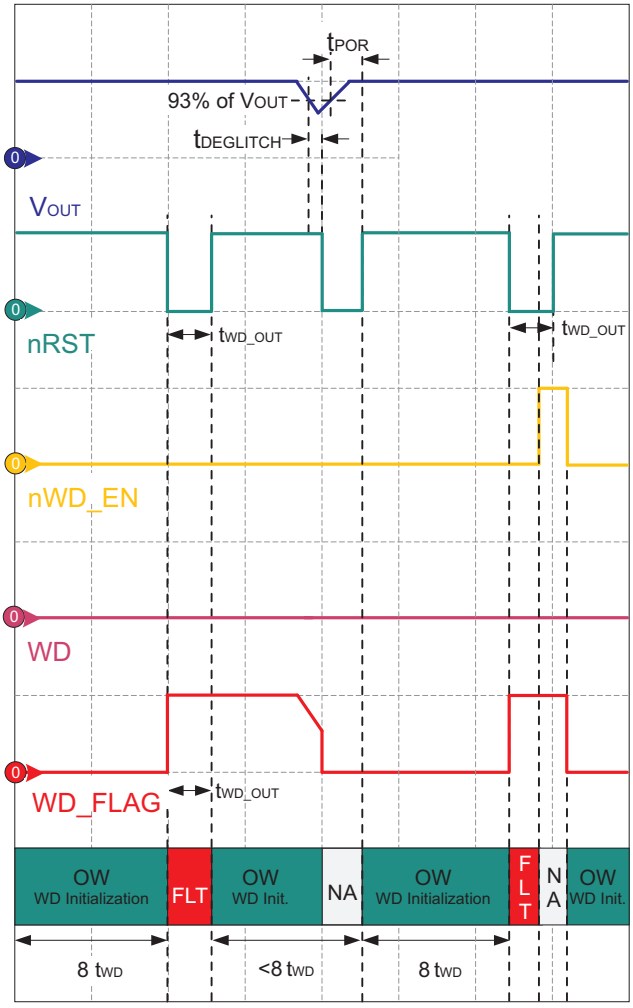


Figure 32. Watchdog Fault during Initialization, and Reinitialization during Reset for TPS7A6401

As shown in Figure 31 for TPS7A6401, the watchdog fault condition also occurs if watchdog is not serviced during the open window after watchdog initialization. i.e. if watchdog is not serviced during first 8 x t_{WD_OUT} duration after initialization, a fault condition will occur. This causes watchdog fault pin (WD_FLT) to go low temporarily for t_{WD_OUT} duration. In case of a load transient, if the regulated output voltage drops down causing reset (nRST) to go low, the rising edge on nRST will cause watchdog to reinitialize (i.e when reset become high while the watchdog is still enabled). During a fault condition (i.e. WD_FLT is low), if the watchdog is disabled, the fault output will continue to stay low until t_{WD_OUT} is elapsed. A falling edge on nWD_EN pin causes watchdog to reinitialize while nRST is still high.

As shown in Figure 32 for TPS7A6401, the watchdog fault condition also occurs if watchdog is not serviced during the open window after watchdog initialization. i.e. if watchdog is not serviced in first 8 x t_{WD_OUT} duration after initialization, a fault condition will occur. This causes watchdog flag pin (WD_FLAG) to become high and stay latched. At the same time, the nRST pin goes low temporarily for t_{WD_OUT} duration. In case of a load transient, if the regulated output voltage drops down causing reset output to go low, the WD_FLAG will be asserted low and the rising edge on nRST will cause watchdog to reinitialize (while the watchdog is still enabled). During a fault condition (i.e. WD_FLAG is high), if the watchdog is disabled, the flag output will continue to stay high as long as the watchdog is enabled or watchdog is serviced properly. However, nRST stays low till t_{WD_OUT} is elapsed. Re-enabling the watchdog causes watchdog to reinitialize (while nRST is still high).

APPLICATION INFORMATION

Typical application circuit for TPS7A6401 and 6333/50 are shown in Figure 33 and Figure 34. Depending upon an end application, different values of external components may be used. In order to program the output voltage, feedback resistors (R1 and R2) should be carefully selected. Using smaller resistors will result in higher current consumption, where as, using very large resistors will impact the sensitivity of the regulator. Therefore, It is recommended to select feedback resistors such that the sum of R1 and R2 is between 20KΩ and 200kΩ.

Example

If the desired regulayed output voltage is 5V, upon selecting R2; R1 can be calculated using (and vice versa) Equation 2. Knowing V_{REF} = 1.23V (typical), V_{OUT} = 5V, selecting R2 = 20kΩ, R1 is calculated to be 61.3kΩ.

A larger output capacitor may be required during fast load steps to prevent output from temporarily dropping down. A low ESR ceramic capacitor with dielectric of type X5R or X7R is recommended. Additionally, a bypass capacitor can be connected at the output to decouple high frequency noise as per the end application.

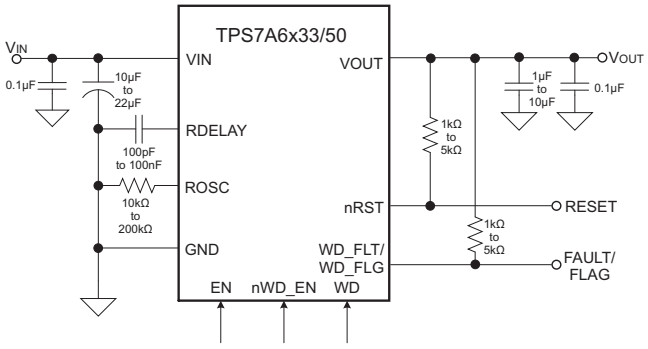


Figure 33. Typical Application Schematic TPS7A633/50

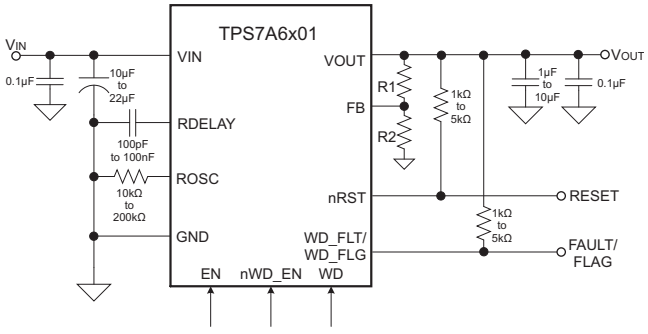


Figure 34. Typical Application Schematic TPS7A6401

Power Dissipation and Thermal Considerations

Power dissipated in the device can be calculated using Equation 8.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (8)$$

Where,

P_D = continuous power dissipation
I_{OUT} = output current
V_{IN} = input voltage
V_{OUT} = output voltage
$I_{QUIESCENT}$ = quiescent current

As $I_{QUIESCENT}$ << I_{OUT}, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in Equation 8 can be ignored.

For device under operation at a given ambient air temperature (T_A), the junction temperature (T_J) can be calculated using Equation 9.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (9)$$

Where,

θ_{JA} = junction to ambient air thermal impedance

The rise in junction temperature due to power dissipation can be calculated using Equation 10.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (10)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate can be calculated using Equation 11.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (11)$$

Example

If I_{OUT} = 100mA, V_{OUT} = 5V, V_{IN} = 14V, $I_{QUIESCENT}$ = 250µA and θ_{JA}= 50°C/W, the continuous power dissipated in the device is 0.9W. The rise in junction temperature due to power dissipation is 45°C. For a maximum junction temperature of 150°C, maximum ambient air temperature at which the device can operate is 105°C.

For adequate heat dissipation, it is recommended to solder the power pad (exposed heat sink) to thermal land pad on the PCB. Doing this provides a heat conduction path from die to the PCB and reduces overall package thermal resistance. Power derating curves for TPS7A63/4xx-PWP package and TPS7A6333-DRK are comparable and are shown in Figure 35.

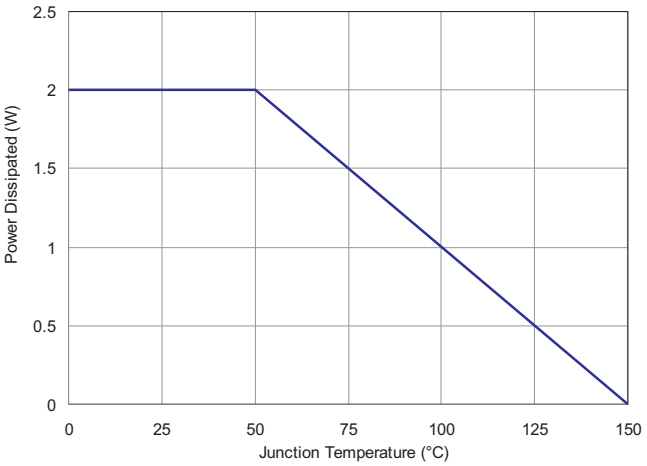
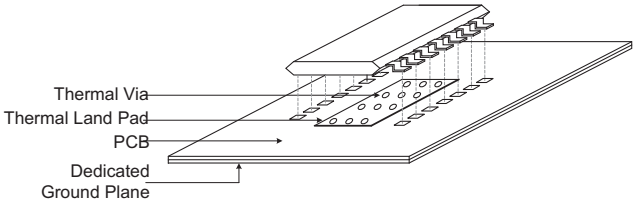
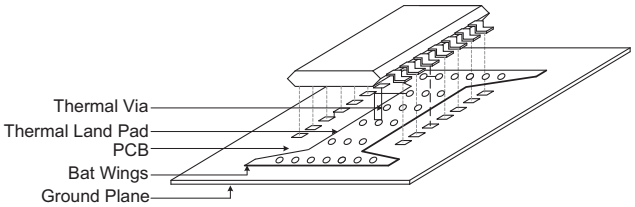


Figure 35. Power Derating Curve

For optimum thermal performance, it is recommended to use a high K PCB with thermal vias between ground plane and solder pad/ thermal land pad. This is shown in Figure 36 (a) and (b). Further, heat spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area. For a 2 layer PCB, a bat wing layout can enhance the heat spreading capabilites.



(a) Multilayer PCB with a dedicated ground plane



(b) Dual layer PCB with Bat wings for enhanced heat spreading

Figure 36. Using Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent.

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Deleted teh Ordering Information Table 2
- Changed values for V_{IL} and V_{IH} in the Watchdog Enable Input (nWD_EN pin) section 4
- Changed values for V_{IL} and V_{IH} in the Watchdog Input Pulse (WD pin) section 4

Changes from Revision A (August 2011) to Revision B **Page**

- Deleted devices TPS7A64333-Q1 and TPSA6450-Q1 1

Changes from Revision B (December 2011) to Revision C **Page**

- Changed regulated output voltage (6.1), added text to the test conditions (10mA to 200mA, $V_{IN} = V_{OUT}$ + 1V to 16V) 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6301QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6301	Samples
TPS7A6333QDRKRQ1	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PRGQ	Samples
TPS7A6333QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6333	Samples
TPS7A6350QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6350	Samples
TPS7A6401QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

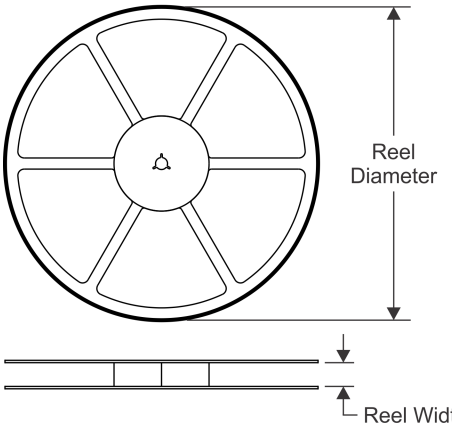
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

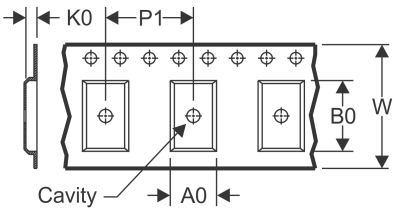
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

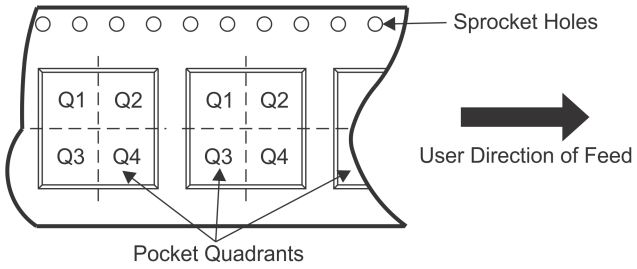


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

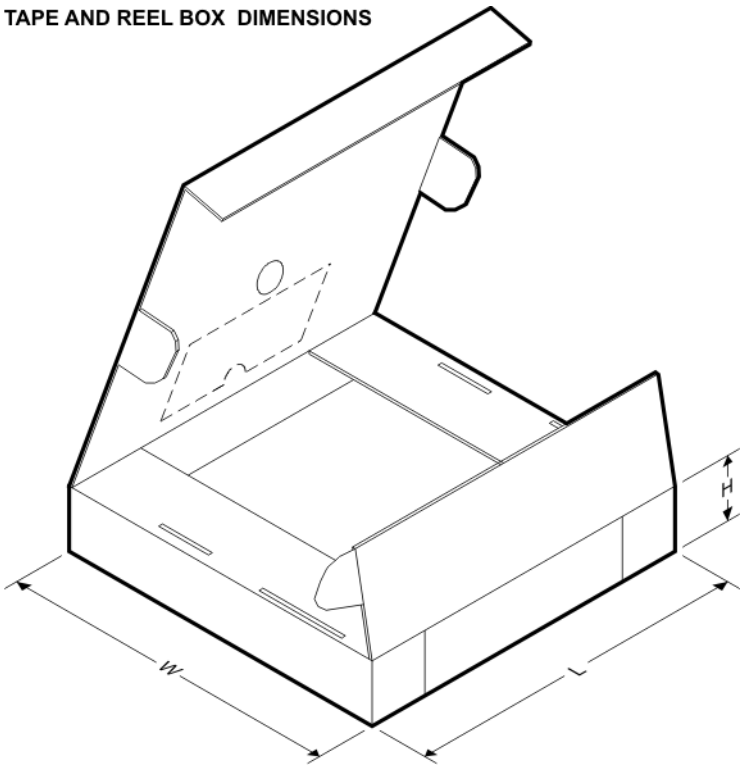
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

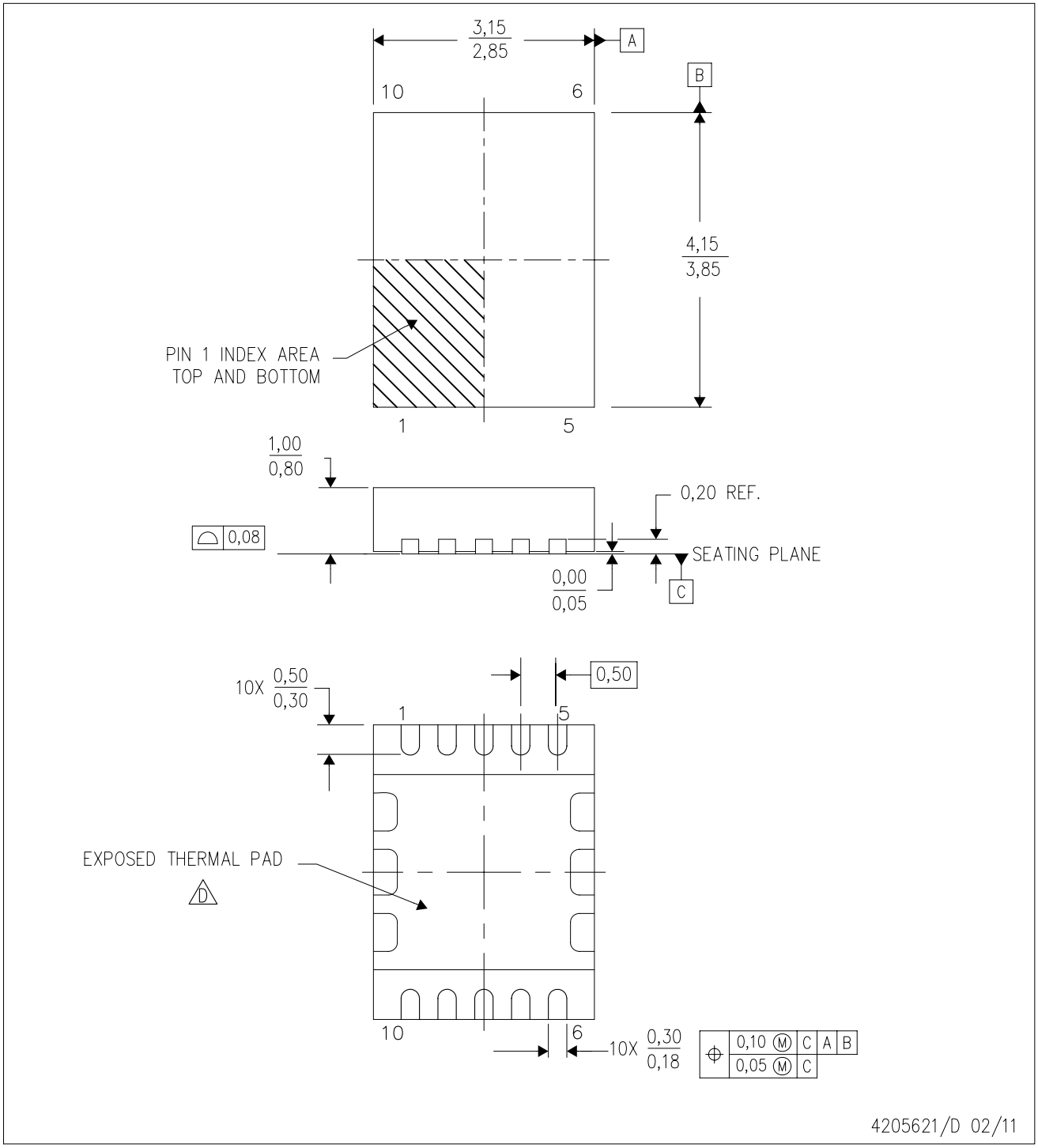
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	367.0	367.0	35.0
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

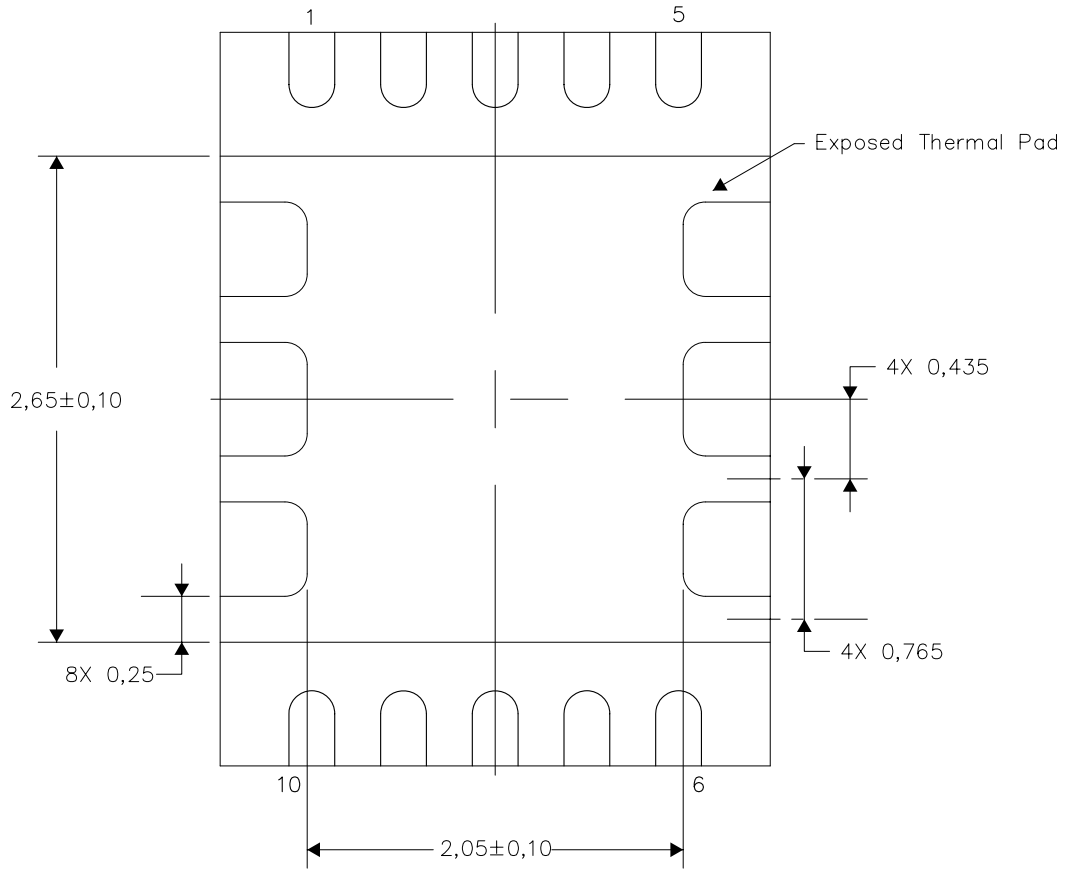
DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



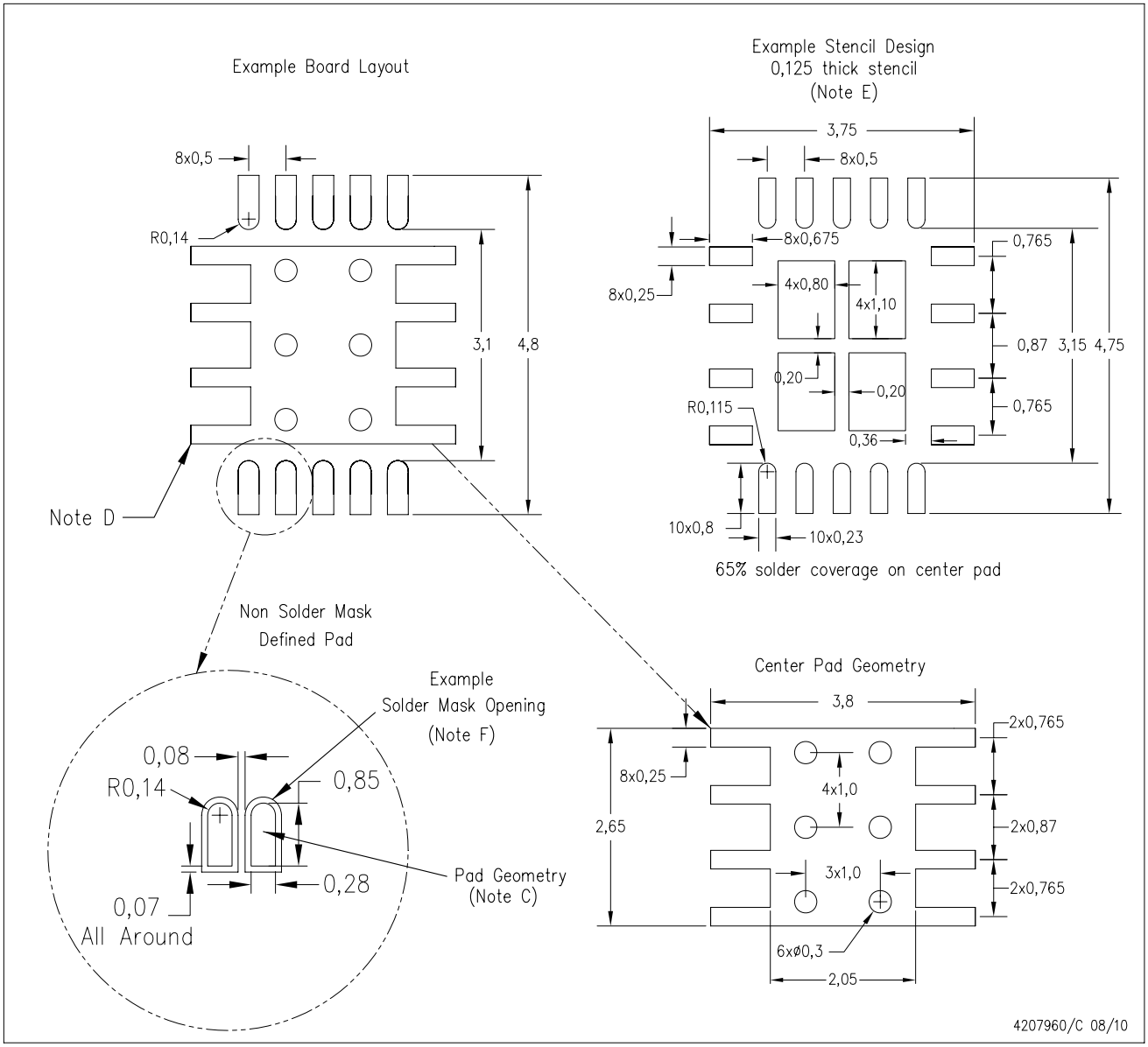
Bottom View

Exposed Thermal Pad Dimensions

4206317/F 08/10

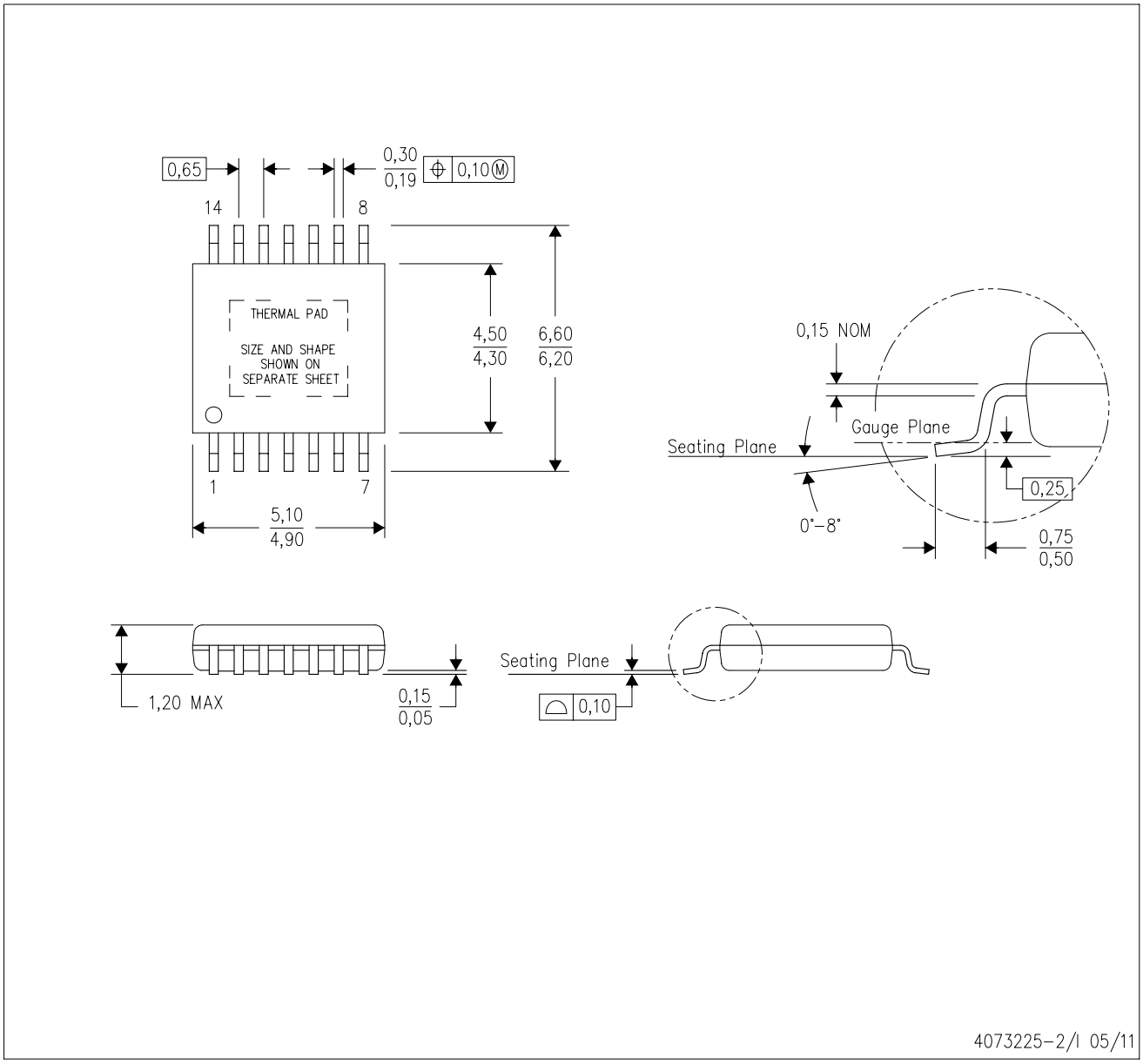
NOTE: A. All linear dimensions are in millimeters

DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

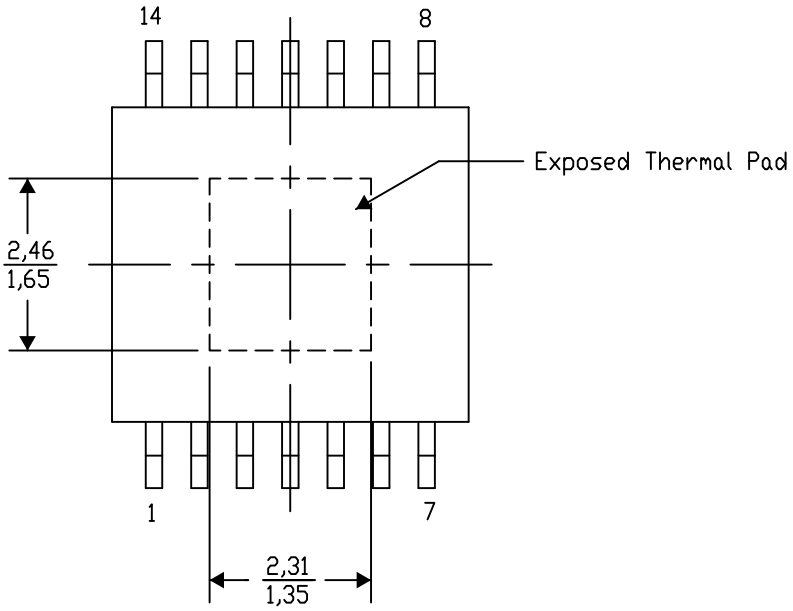
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

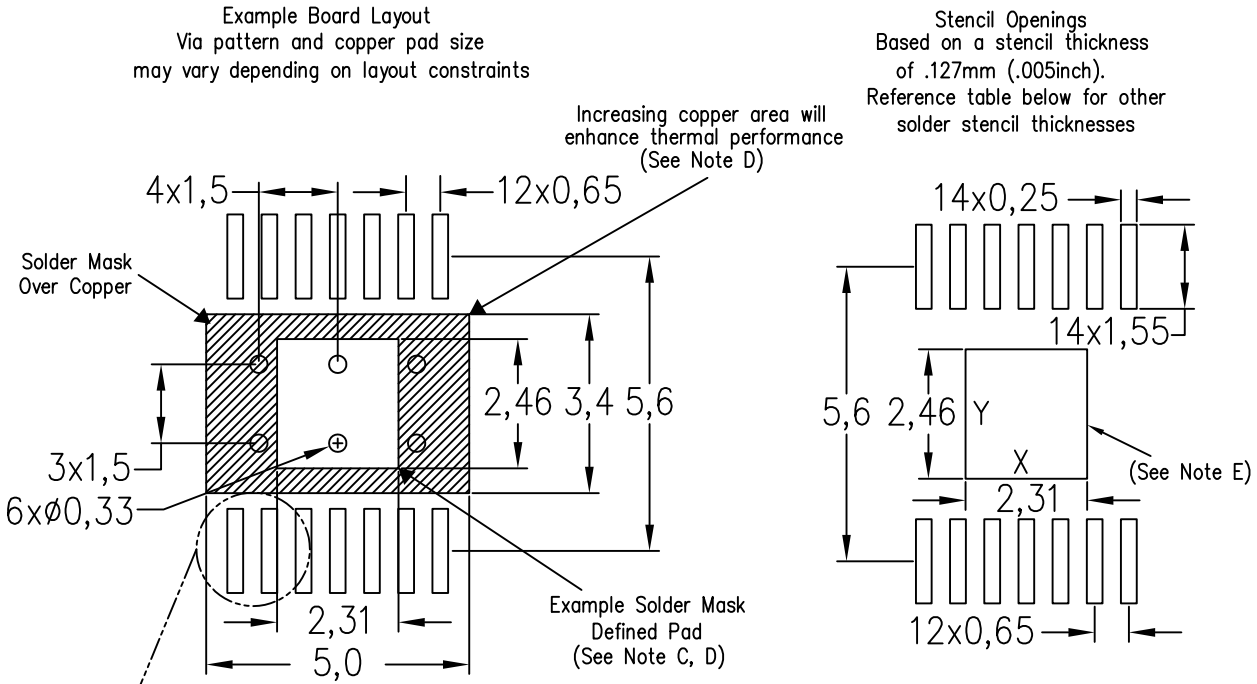
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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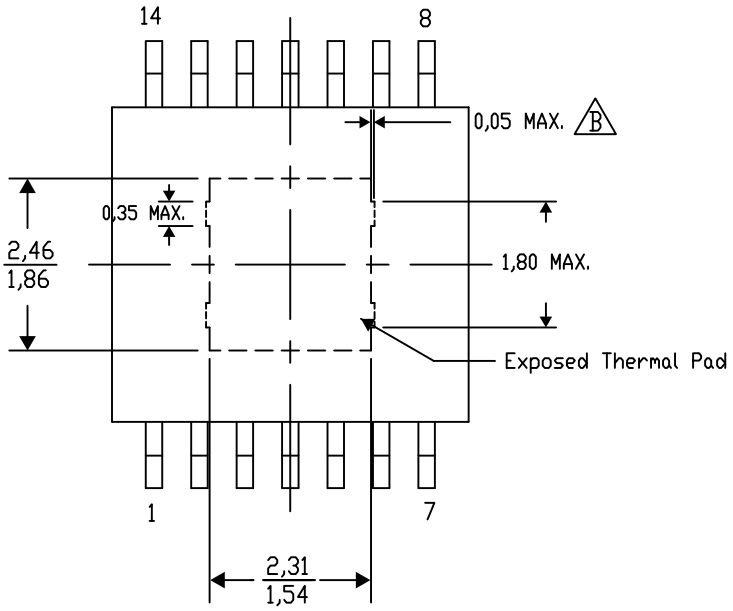


Top View

Exposed Thermal Pad Dimensions

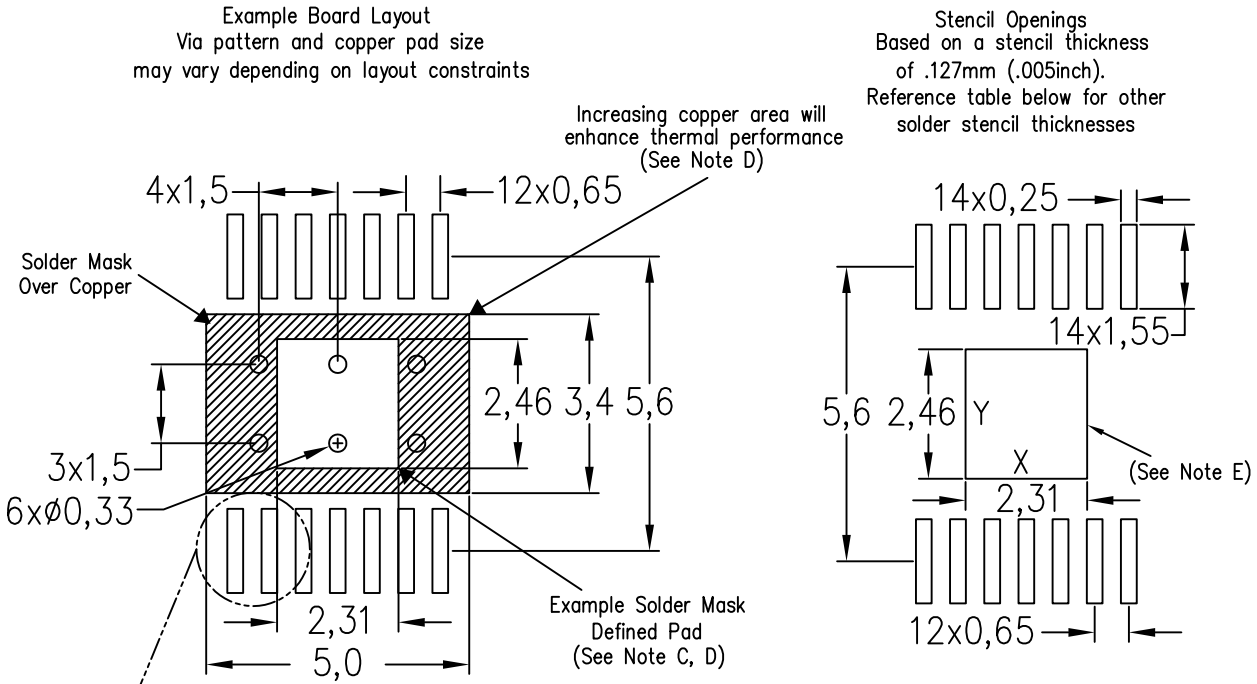
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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