Ordering & quality
Technical documentation
Design & development
Support & training

TPS7H2201-SP and TPS7H2201-SEP Radiation Hardened 1.5-V to 7-V, 6-A eFuse

1 Features

- Standard micro circuit available, SMD 5962R17220
- Vendor item drawing available, VID V62/23608
- Radiation performance:
  - Radiation hardness assurance (RHA) up to TID 100 krad(Si)
  - Single event latchup (SEL), single event burnout (SEB), and single event gate rupture (SEGR) immune to LET = 75 MeV-cm^2/mg
  - SEFI/SET characterized to LET = 75 MeV-cm^2/mg
- Integrated single channel eFuse
- Input voltage range: 1.5 V to 7 V
- Low on-resistance (R_{ON}) of :
  - 35-mΩ maximum at 25°C and VIN = 5 V for CFP and KGD
  - 21.8-mΩ maximum at 25°C and VIN = 5 V for HTSSOP
- 6-A maximum continuous switch current
- Low control input threshold enables use of 1.2-, 1.8-, 2.5-, and 3.3-V logic
- Configurable rise time (soft start)
- Reverse current protection
- Programmable and internal current limiting (fast-trip)
- Programmable fault timer (current limit and retry modes)
- Thermal shutdown
- Ceramic and plastic package with thermal pad

2 Applications

- Space satellite power management and distribution
- Radiation hardened and tolerant power tree applications
- Available in military (–55°C to 125°C) temperature range

3 Description

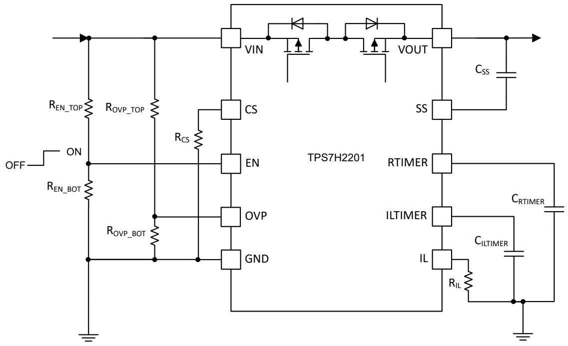
The TPS7H2201 is a single channel eFuse that provides configurable rise time to minimize inrush current and reverse current protection. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.5 V to 7 V and can support a maximum continuous current of 6 A. The switch is controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals.

The TPS7H2201 is available in a ceramic and plastic package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –55°C to 125°C.

Device Information

PART NUMBER(1)	GRADE	PACKAGE
5962R1722001VXC	Flight grade RHA 100 krad(Si)	16-Pin CDFP 11.00 × 9.60 mm Weight: 1.56 g(3)
5962-1722001VXC	Flight grade QMLV	
TPS7H2201HKR/EM	Engineering samples(2)	
TPS7H2201MDAPTSEP (4)	SEP	32-Pin HTSSOP 6.10 × 11.00 mm Weight: 0.191 g(3)
TPS7H2201EVM-CVAL	Ceramic evaluation board	EVM

(1) For all available packages, see the orderable addendum at the end of the data sheet. Also refer to Section 5.
(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
(3) Weight is accurate to ±10%.
(4) Product preview.



Simplified Schematic

Table of Contents

4 Revision History

Changes from Revision B (May 2019) to Revision C (June 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added TPS7H2201-SEP to the data sheet	1
• Added SMD and VID links	1
• Modified the Simplified Schematic	1
• Added Device Options table	3
• Added plastic package and corrected the bond-pad coordinates	4
• Added a clarifying footnote for V_{OUT} in the recommended operating condition and VIN_{EN} for all devices Electrical Characteristics	8
• Improved the forward leakage current (I_F) maximum limit from 3 mA to 250 µA and added additional typical values for all devices Electrical Characteristics	8
• Split Fast trip off off-time, Internal current limit timer (fast trip off current limit), and R_{ON} for CFP, KGD, and HTSSOP Electrical Characteristics	8
• Changed *I_{IL} vs R_{IL} Across Temperature* x-axis label from kΩ to Ω	14
• Added a waveform showing t_{LOW} and modified other waveform titles in Parameter Measurement Information	18
• Added the VREF = 0.5 V at the IL pin	20
• Add RTIMER and ILTIMER summary table	22
• Added reverse current protection description	29
• Added forward leakage current description	29
• Added VOUT connection table for OVP voltage condition	30

Changes from Revision A (January 2019) to Revision B (May 2019)	Page
• Added Bare Die Information table in *Pin Configuration and Functions* section	4
• Added Bond Pad Coordinates in Microns table in *Pin Configuration and Functions* section	4
• Added after TID specification for I_{SD} VIN	9
• Added Quality Conformance Inspection table to *Specifications* section	13

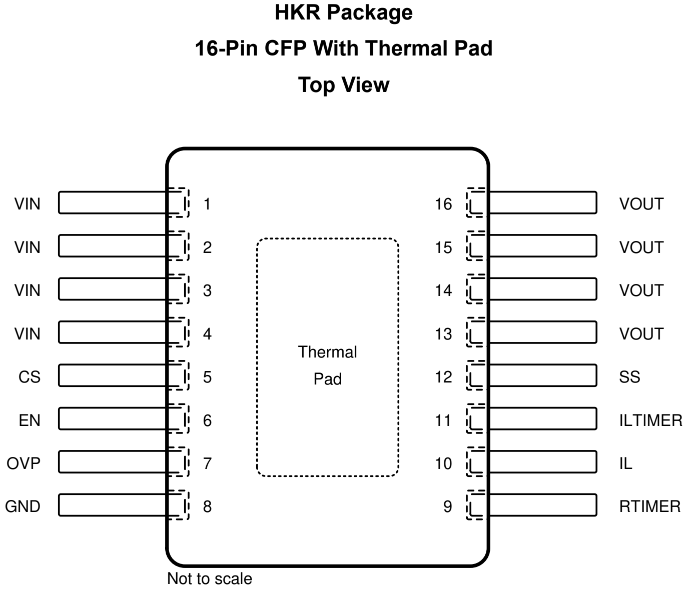
Changes from Revision * (September 2018) to Revision A (January 2019)	Page
• Changed the device status from *Advance Information* to *Production Data*	1

5 Device Options

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H2201-SP	TID of 100 krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	16-pin HKR CFP	5962R1722001VXC
		QMLP-RHA	32-pin DAP HTSSOP	5962R1722002PYE(5)
		KGD (QMLV-RHA)	Die	5962R1722001V9A
	None	Engineering Model (3)	16-pin HKR CFP	PTS7H2201HKR/EM
			Die	TPS7H2201Y/EM
TPS7H2201-SEP	TID of 50 krad(Si) RLAT, DSEE free to 43 MeV-cm^2/mg	Space Enhanced Plastic	32-pin DAP HTSSOP	TPS7H2201MDAPTSEP(4)

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
(4) Advanced information.
(5) Product preview.

6 Pin Configuration and Functions



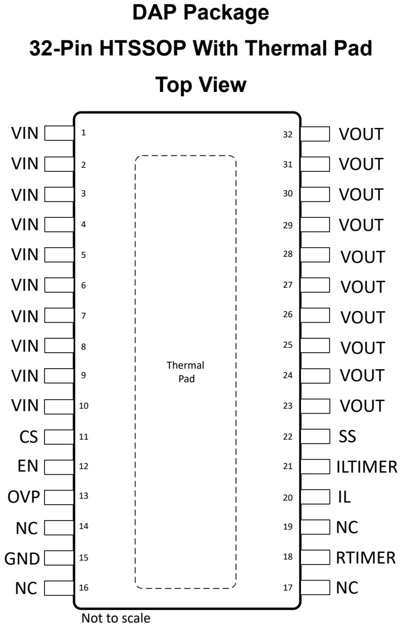


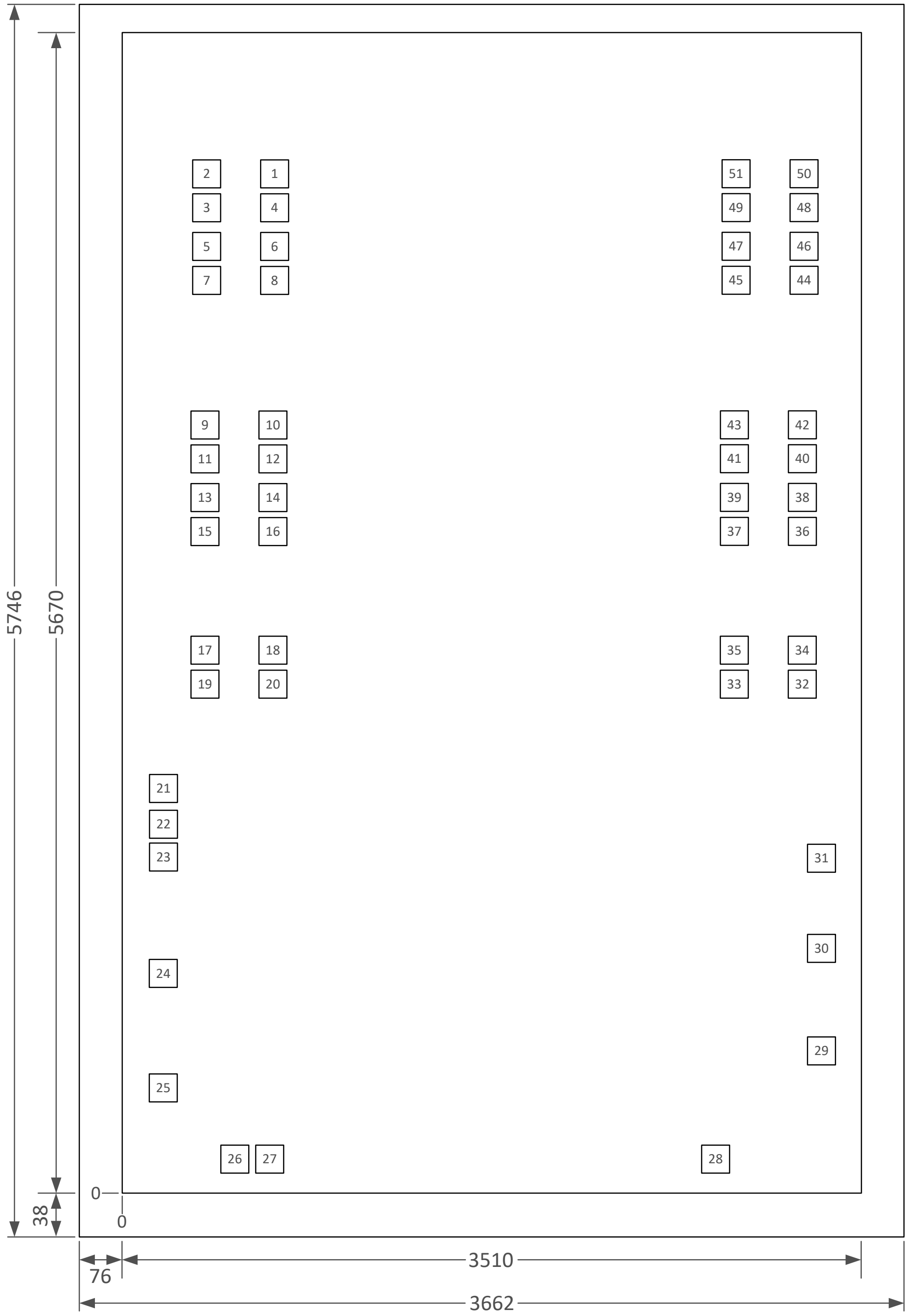
Table 6-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
HKR (16) NO.	PW (32) NO.	NAME		
1-4	1-10	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip.
5	11	CS	O	Current sense pin proportional to output current. Connect a resistor to GND.
6	12	EN	I	Active high switch control input. Do not leave floating.
7	13	OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
8	15	GND	—	Device ground. [2]
9	18	RTIMER	I/O	Capacitor programmed fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled. Do not float this pin or connect it to VIN.
10	20	IL	I/O	Current limiter control. Programmable using an external resistor to GND. Do not float this pin.
11	21	ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device will remain at programmed current limit indefinitely in the event of a short without going intro retry mode. Do not float this pin.
12	22	SS	I/O	Switch slew rate control. See the *Section 9.3.2* section for more information.
13-16	23-32	VOUT	O	Switch output. A minimum 10-μF output capacitor is recommended.
	14,16,17,19	NC	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
	—	Thermal Pad	—	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

(1) I = Input, O = Output, I/O = Input or Output, — = Other
(2) Thermal pad is internally connected to the seal ring and GND for HKR option.

Table 6-2. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	ALCU	1050 nm



1. All dimensions in microns (µm).
2. The inner rectangle is the die and the outer rectangle is the die plus scribe lines.

Table 6-3. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	611.78	4976.1	751.73	5116.05
VIN	2	258.17	4976.1	398.12	5116.05
VIN	3	258.17	4809.15	398.12	4949.1
VIN	4	611.78	4809.15	751.73	4949.1
VIN	5	258.17	4641.39	398.12	4781.34
VIN	6	611.78	4641.39	751.73	4781.34
VIN	7	258.17	4473.59	398.12	4613.54
VIN	8	611.78	4473.59	751.73	4613.54
VIN	9	258.17	3647.7	398.12	3787.65
VIN	10	611.78	3647.7	751.73	3787.65
VIN	11	258.17	3480.75	398.12	3620.7
VIN	12	611.78	3480.75	751.73	3620.7
VIN	13	258.17	3312.99	398.12	3452.94
VIN	14	611.78	3312.99	751.73	3452.94
VIN	15	258.17	3145.19	398.12	3285.14
VIN	16	611.78	3145.19	751.73	3285.14
VIN	17	258.17	2315.57	398.12	2455.52
VIN	18	611.78	2315.57	751.73	2455.52
VIN	19	258.17	2146.37	398.12	2286.32
VIN	20	611.78	2146.37	751.73	2286.36
AVDD	21	54.99	1842.03	194.94	1981.98
AVDD	22	54.99	1671.48	194.94	1811.43
CS	23	54.99	1480.77	194.94	1620.72
EN	24	54.99	972.68	194.94	1112.63
OVP	25	54.99	406.26	194.94	546.21
GND	26	407.21	54.99	547.16	194.94
GND	27	577.76	54.99	717.71	194.94
RTIMER	28	2792.88	54.99	2932.83	194.94
IL	29	3315.06	587.43	3455.01	727.38
ILTIMER	30	3315.06	1099.26	3455.01	1239.21
SS	31	3315.06	1544.09	3455.01	1684.04
VOUT	32	3111.66	2146.37	3251.61	2286.32
VOUT	33	2758.05	2146.37	2898	2286.32
VOUT	34	3111.66	2315.57	3251.61	2455.52
VOUT	35	2758.05	2315.57	2898	2455.52
VOUT	36	3111.66	3145.19	3251.61	3285.14
VOUT	37	2758.05	3145.19	2898	3285.14
VOUT	38	3111.66	3312.99	3251.61	3452.94
VOUT	39	2758.05	3312.99	2898	3452.94
VOUT	40	3111.66	3480.75	3251.61	3620.7
VOUT	41	2758.05	3480.75	2898	3620.7
VOUT	42	3111.66	3647.7	3251.61	3787.65
VOUT	43	2758.05	3647.7	2898	3787.65
VOUT	44	3111.66	4473.59	3251.61	4613.54
VOUT	45	2758.05	4473.59	2898	4613.54

Table 6-3. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	46	3111.66	4641.39	3251.61	4781.34
VOUT	47	2758.05	4641.39	2898	4781.34
VOUT	48	3111.66	4809.15	3251.61	4949.1
VOUT	49	2758.05	4809.15	2898	4949.1
VOUT	50	3111.66	4976.1	3251.61	5116.05
VOUT	51	2758.05	4976.1	2898	5116.05

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN	Input voltage	–0.3	7.5	V
VOUT	Output voltage	–0.3	7.5	V
EN, OVP	Enable and over voltage protection pins	–0.3	7.5	V
CS, ILTIMER, RTIMER, IL, SS	Current sense, current limit timer, retry timer, current limit and soft start pins	–0.3	VIN + 0.3	V
I_{MAX}	Maximum continuous switch current		9	A
I_{PLS}	Maximum pulsed switch current (t≤5µs)		45	A
T_J	Maximum junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input voltage	1.5	7	V
SR_{VIN}	Input voltage slew rate		0.01	V/µs
VOUT	Output voltage	0	7 (1)	V
I_{MAX}	Maximum continuous switch current		6	A
T_J	Operating junction temperature(2)	–55	125	°C

(1) This maximum VOUT voltage is only applicable when the device is disabled (EN = Low). When the device is enabled (EN = High), the maximum VOUT voltage is the input voltage, VIN.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A\ (max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC [1]		TPS7H2201-SP	TPS7H2201-SEP	UNIT
		HKR (CFP)	DAP (HTSSOP)	
		16 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	23.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	11.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	5.4	
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.1	
ψ_{JB}	Junction-to-board characterization parameter	42.5	5.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	0.5	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: All Devices

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP [1]	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
VIN_{HUVLO}	Internal VIN UVLO voltage, rising					1.32		V
VIN_{LUVLO}	Internal VIN UVLO voltage, falling					1.23		V
$HYST_{VIN-UVLO}$	Internal VIN UVLO hysteresis					92		mV
I_Q	Quiescent current	I_{OUT} = 0 mA, V_{IN} = EN = 5 V, CS resistor of 20 kΩ to GND		1, 2, 3		2.4	6.5	mA
I_F	VIN to VOUT forward leakage current	EN = VOUT = GND, measured VOUT current	1.5 V ≤ VIN ≤ 7 V	1, 2, 3			250	µA
			VIN =1.5 V	1, 2, 3		3.27		
			VIN = 1.8 V	1, 2, 3		3.35		
			VIN= 3.3 V	1, 2, 3		3.62		
			VIN = 5 V	1, 2, 3		4.11		
			VIN = 7 V	1, 2, 3		6.82		
I_{SD} VIN	VIN off-state supply current	EN = GND, I_{OUT} = 0 mA, measured VIN current	VIN = 5 V	1, 2, 3		0.4	3	mA
			VIN = 3.3 V	1, 2, 3		0.3	3	
			VIN = 1.8 V	1, 2, 3		0.2	3	
			After TID = 100 krad, VIN = 1.8, 3.3, and 5 V	1			3.1	
I_{RCP}	Reverse current protection leakage current	EN = 0 V, VIN = 0 to 7 V, VOUT = 0 to 7 V for VOUT > VIN		1, 2, 3		0.45	2.5	mA
		EN = 7 V, VIN = 0 V, VOUT = 0 to 7 V						
SOFT START								
I_{SS}	Soft start charge current	1 V on SS pin		1, 2, 3		65	83	µA
SR_{SS}	Soft start slew rate	SS pin floating, COUT = 10 µF				295		mV/µs
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT								
V_{IHEN}	EN/UVLO threshold voltage, rising			1, 2, 3	0.56	0.61	0.65	V
V_{ILEN}	EN/UVLO threshold voltage, falling			1, 2, 3	0.47	0.51	0.55	V
$HYST_{EN}$	EN/UVLO hysteresis voltage			1, 2, 3		93	124	mV
t_{LOW}	EN signal low time during cycling	RTIMER = GND, IL = 1 A, I_{VOUT} = 2 A	See Figure 8-3	9, 10, 11	20			µs
VIN_{EN}	VIN percentage for enable[2]			4, 5, 6	75%			
I_{EN}	EN pin input leakage current	EN = VIN = 5 V		1, 2, 3			12	nA

7.5 Electrical Characteristics: All Devices (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUBGROUP [1]	MIN	TYP	MAX	UNIT
OVERVOLTAGE PROTECTION (OVP)							
V_{OVPR}	OVPR thresold voltage, rising		1, 2, 3	0.52	0.57	0.63	V
V_{OVPF}	OVPF threshold voltage, falling		1, 2, 3	0.5	0.55	0.59	V
$HYST_{OVP}$	OVP hysteresis voltage	1.6 V < VIN < 7 V	1, 2, 3		20	55	mV
I_{OVP}	OVP pin input leakage current		1, 2, 3			15	nA
CURRENT LIMIT AND CURRENT SENSE							
t_{CSEN}	Time for valid CS output after enable	C_{SS} = 120 nF	9, 10, 11			5	ms
Minimum VOUT current for valid CS output			1, 2, 3	750			mA
VOUT current change to CS change delay time		0.5-A rising step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	74	µs
VOUT current change to CS change delay time		0.5-A falling step, 100 mA/µs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	73	µs
CS pin accuracy		0.75 A ≤ I_{VOUT} ≤ 7.5 A	4, 5, 6	–10%		10%	
CS pin voltage		0.75 A ≤ I_{VOUT} ≤ 7.5 A, no OCP	1, 2, 3			VIN – 0.4	V
Current limit setting, I_{IL}		I_{VOUT} ≤ 1 A	1, 2, 3	I_{VOUT} + 0.5			A
		1A < I_{VOUT} ≤ 3 A	1, 2, 3	I_{VOUT} + 1			
		I_{VOUT} > 3 A	1, 2, 3	I_{VOUT} + 1.5			
Programmable current limit accuracy		1.5 V ≤ VIN ≤ 7 V	4, 5, 6	–20%		20%	
Fast trip off current limit		VIN = 5 V, 10-mΩ short in 10 µs			22		A
TIMERS							
$I_{ILTIMER}$	ILTIMER charge current		1, 2, 3	0.7	1	1.38	µA
$PD_{ILTIMER}$	ILTIMER internal pull-down resistance	40 mV on ILTIMER pin	1, 2, 3		38	153	Ω
I_{RTIMER}	RTIMER charge current		1, 2, 3	0.7	1	1.38	µA
PD_{RTIMER}	RTIMER internal pull-down resistance	40 mV on RTIMER pin	1, 2, 3		38	153	Ω
THERMAL SHUTDOWN							
Thermal shutdown		VIN = 5 V			175		°C
Thermal shutdown hysteresis		VIN = 5 V			20		°C

(1) For subgroup definitions, see Quality Conformance Inspection table.
(2) VIN must be ≥ 75% of its final value before EN is asserted only if VIN_{SR} > $VOUT_{SR}$.

7.6 Electrical Characteristics: CFP and KGD Options

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP(1)	MIN	TYP	MAX	UNIT
CURRENT LIMIT AND CURRENT SENSE								
Fast trip off off-time		VIN = 5 V, C_{SS} = 2.7 nF		9, 10, 11		61	158	µs
Internal current limit timer (fast trip off current limit)		VIN = 5 V, I_{VOUT} = 3 A, IL = 6 A, ILTIMER = VIN, 10-mΩ short in 10 µs		9, 10, 11		15	35	
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance, lead length = 2.5 mm	VIN = 7 V, I_{IL} = 7.5 A	–55°C	1, 2, 3			24	mΩ
			–40°C				26	
			25°C			31	34	
			85°C			37	40	
			125°C			41	45	
		VIN = 5 V, I_{IL} = 7.5 A	–55°C	1, 2, 3			26	
			–40°C				27	
			25°C			32	35	
			85°C			39	42	
			125°C			43	47	
		VIN = 3.3 V, I_{IL} = 7.5 A	–55°C	1, 2, 3			28	
			–40°C				30	
			25°C			35	38	
			85°C			42	46	
			125°C			47	52	
		VIN = 1.8 V, I_{IL} = 7.5 A	–55°C	1, 2, 3			36	
			–40°C				39	
			25°C			45	51	
			85°C			55	62	
			125°C			61	70	
		VIN = 1.5 V, I_{IL} = 7.5 A	–55°C	1, 2, 3			44	
			–40°C				48	
			25°C			52	63	
			85°C			63	77	
			125°C			70	87	

(1) For subgroup definitions, see Quality Conformance Inspection table.

7.7 Electrical Characteristics: HTSSOP Option

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
CURRENT LIMIT AND CURRENT SENSE								
Fast trip off off-time		VIN = 5 V, C_{SS} = 2.7 nF		9, 10, 11		61		μs
Internal current limit timer (fast trip off current limit)		VIN = 5 V, I_{VOUT} = 3 A, IL = 6 A, ILTIMER = VIN, 10-mΩ short in 10 μs		9, 10, 11		15		
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	VIN = 7 V, I_{IL} = 7.5 A	–55°C	1, 2, 3		15.1	15.8	mΩ
			–40°C			16		
			25°C			19.4	20.3	
			85°C			22.4		
			125°C			24.5	25.5	
		VIN = 5 V, I_{IL} = 7.5 A	–55°C	1, 2, 3		16.1	16.8	
			–40°C			17.1		
			25°C			20.8	21.8	
			85°C			24.1		
			125°C			26.4	27.4	
		VIN = 3.3 V, I_{IL} = 7.5 A	–55°C	1, 2, 3		18	18.8	
			–40°C			19.2		
			25°C			23.5	24.6	
			85°C			27.4		
			125°C			30.1	31.3	
		VIN = 1.8 V, I_{IL} = 7.5 A	–55°C	1, 2, 3		24.8	25.9	
			–40°C			26.5		
			25°C			32.9	34.5	
			85°C			38.5		
			125°C			42.5	44.2	
		VIN = 1.5 V, I_{IL} = 7.5 A	–55°C	1, 2, 3		29.8	31.2	
			–40°C			31.8		
			25°C			39.5	41.5	
			85°C			46.2		
			125°C			51	53.3	

(1) For subgroup definitions, see Quality Conformance Inspection table.

7.8 Switching Characteristics (All Devices)

over operating free-air temperature range (unless otherwise noted)

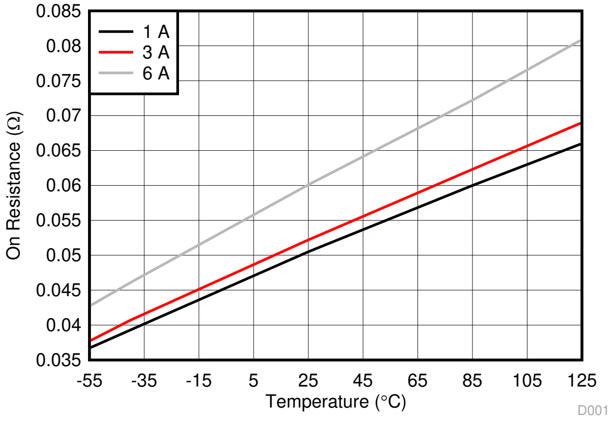
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = EN = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		208		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		60		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		90		µs
t_{ASSERT}	OVP assert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		4.5		µs
$t_{DEASSERT}$	OVP deassert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		9.6		µs
VIN = EN = 1.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		173		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		64		µs
t_F	VOUT fall time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		70		µs
t_{ASSERT}	OVP assert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		2.65		µs
$t_{DEASSERT}$	OVP deassert time	R_L = 10 Ω, C_L = 10 µF, C_{SS} = 1000 pF		6.56		µs

7.9 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

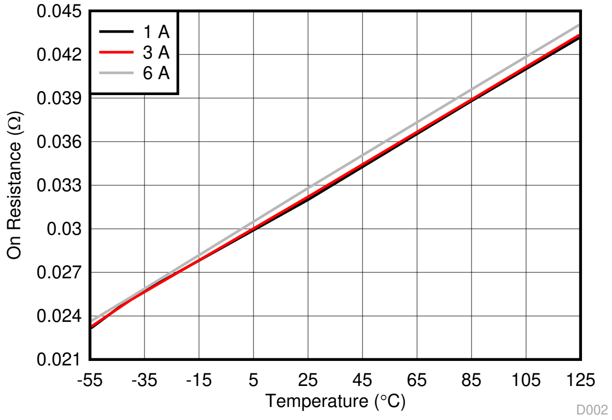
SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

7.10 Typical Characteristics



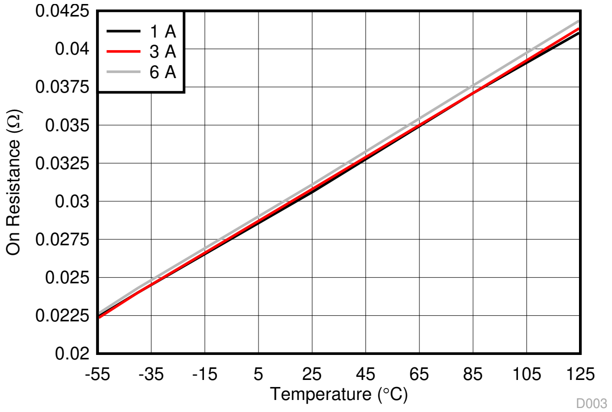
I_{IL} = 7.5 A

Figure 7-1. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 1.5 V



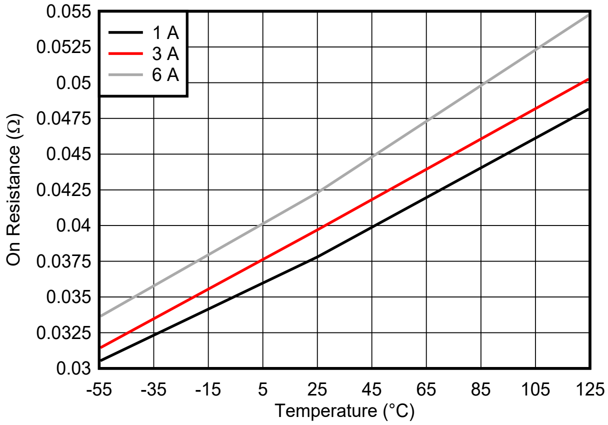
I_{IL} = 7.5 A

Figure 7-2. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 5 V



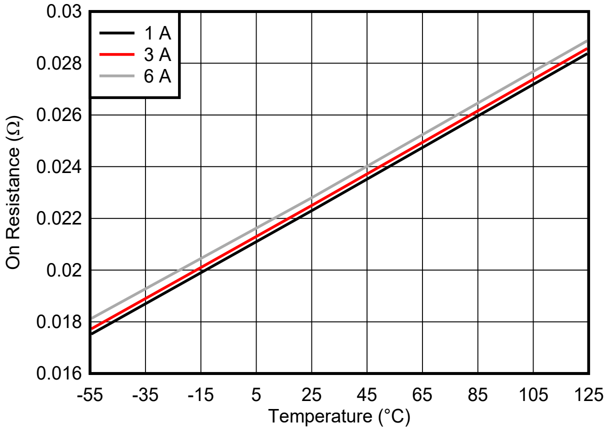
I_{IL} = 7.5 A

Figure 7-3. On-Resistance vs Temperature Across Loads for CFP and KGD at VIN = 7 V



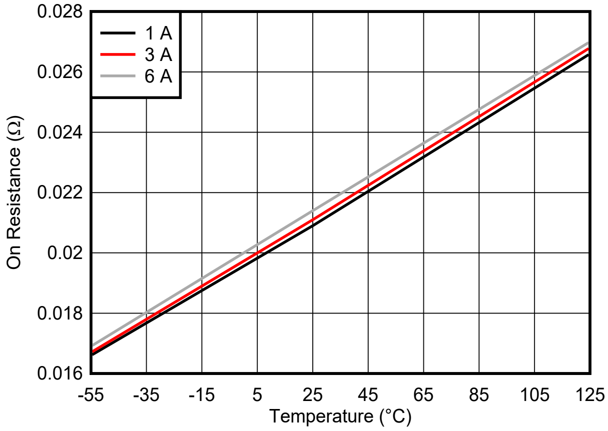
I_{IL} = 7.5 A

Figure 7-4. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 1.5 V



I_{IL} = 7.5 A

Figure 7-5. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 5 V



I_{IL} = 7.5 A

Figure 7-6. On-Resistance vs Temperature Across Loads for HTSSOP at VIN = 7 V

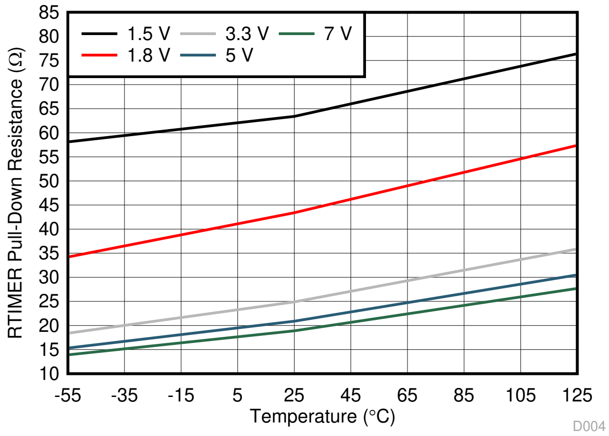


Figure 7-7. RTIMER Pull-Down Resistance vs Temperature Across VIN

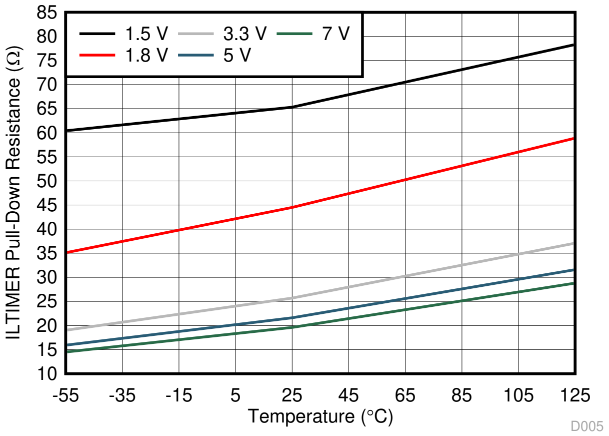


Figure 7-8. ILTIMER Pull-Down Resistance vs Temperature Across VIN

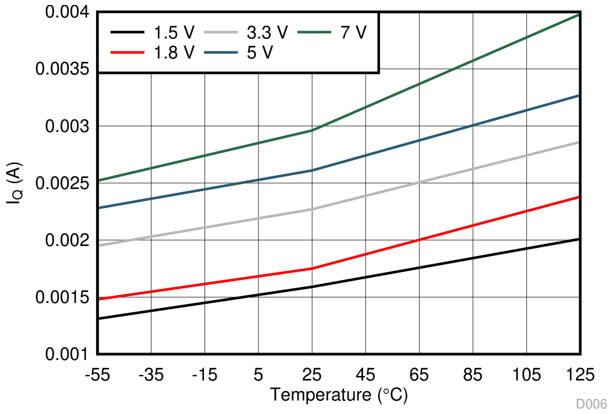


Figure 7-9. I_Q vs Temperature Across VIN

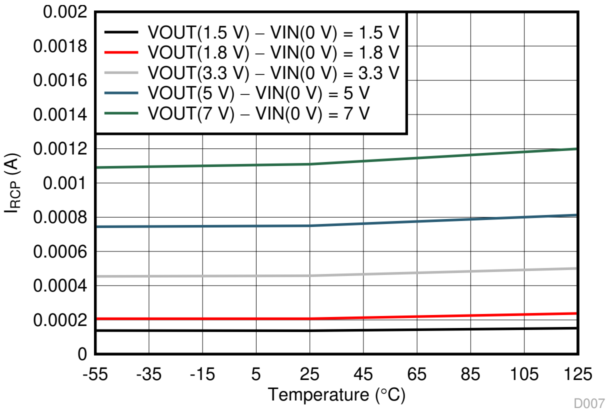


Figure 7-10. I_{RCP} vs Temperature With EN = 7 V

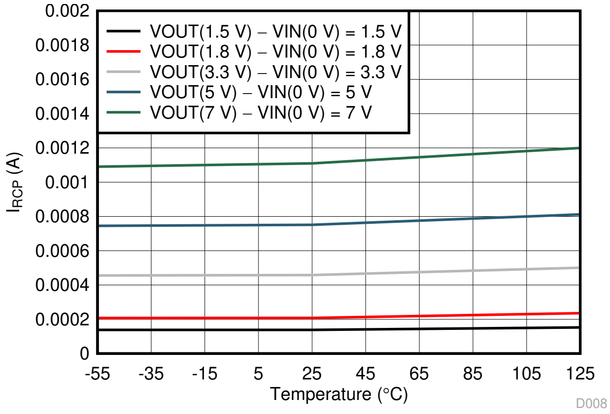


Figure 7-11. I_{RCP} vs Temperature With EN = GND

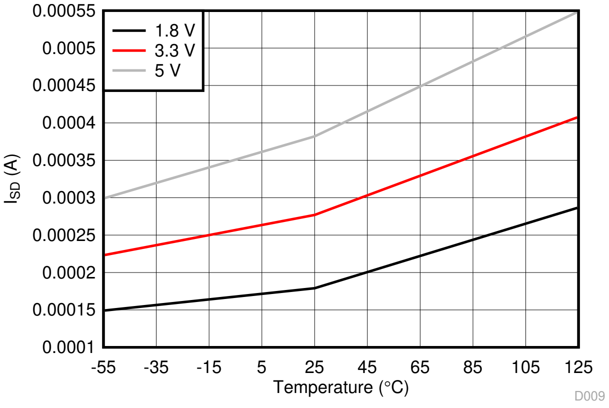


Figure 7-12. I_{SD} VIN vs Temperature Across VIN

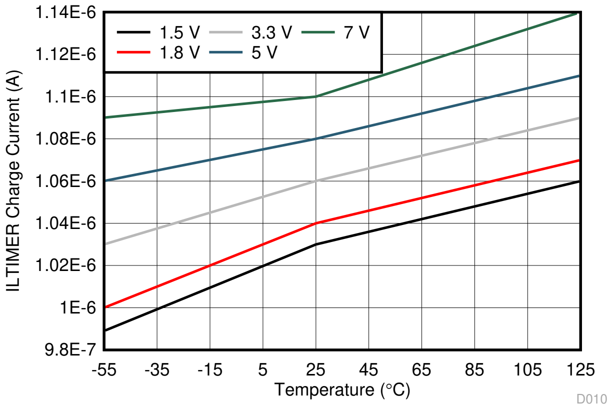


Figure 7-13. ILTIMER Charge Current vs Temperature Across VIN

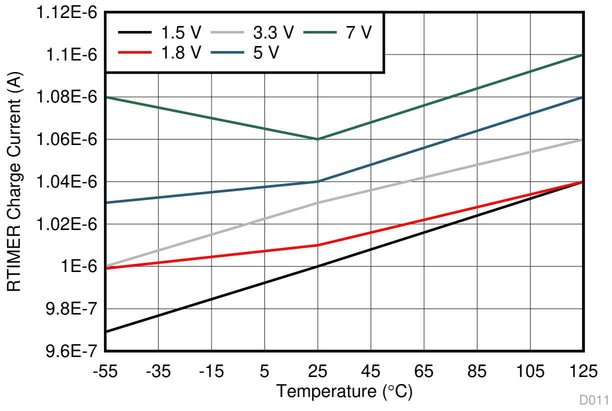


Figure 7-14. RTIMER Charge Current vs Temperature Across VIN

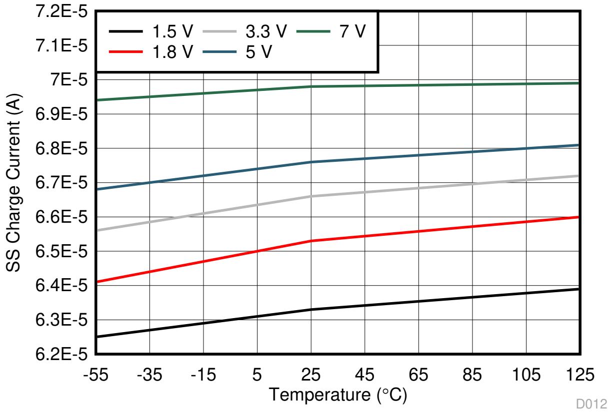
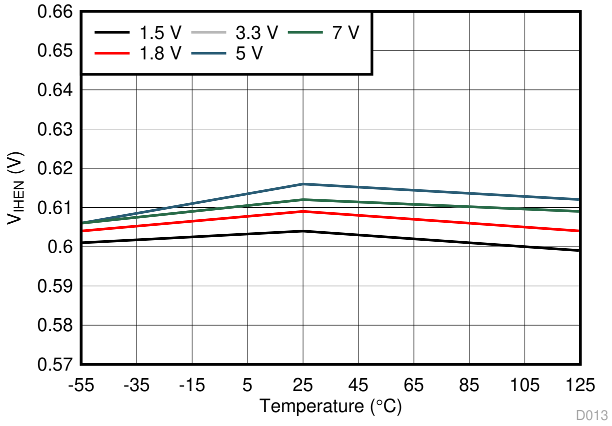
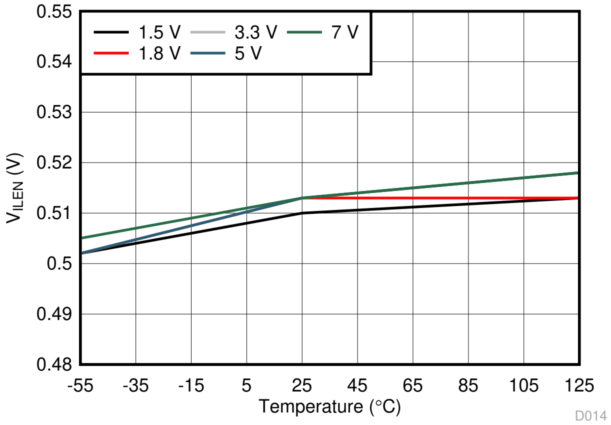


Figure 7-15. SS Charge Current vs Temperature Across VIN



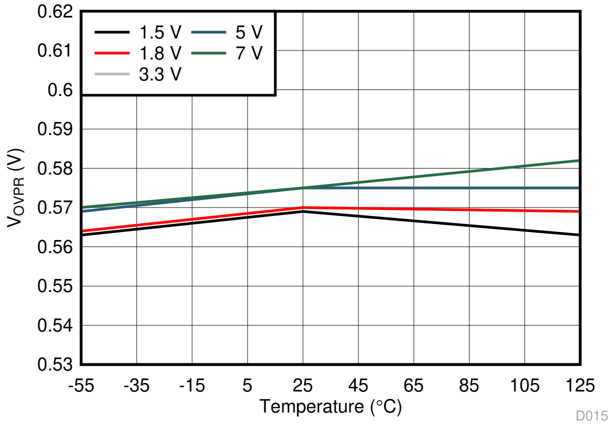
EN pin driven directly

Figure 7-16. V_{IHEN} vs Temperature Across VIN



EN pin driven directly

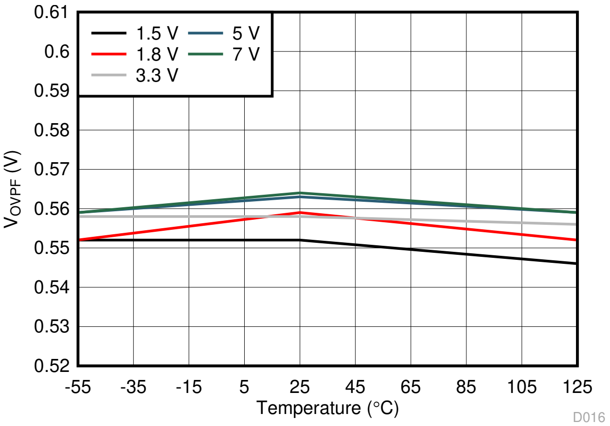
Figure 7-17. V_{ILEN} vs Temperature Across VIN



OVP pin driven directly

Waveform at 3.3 V is obscured by the 5 V

Figure 7-18. V_{OVPR} vs Temperature Across VIN



OVP pin driven directly

Figure 7-19. V_{OVPF} vs Temperature Across VIN

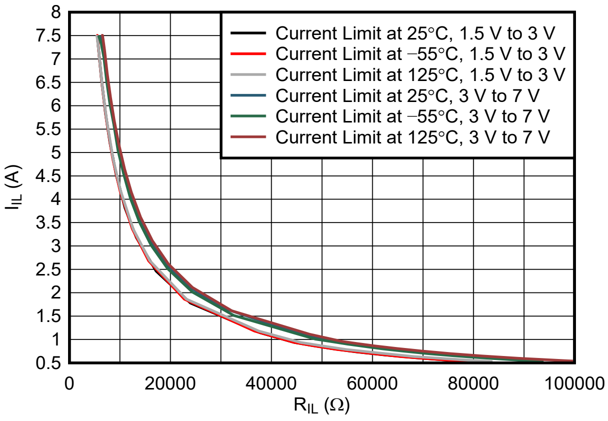


Figure 7-20. I_{IL} vs R_{IL} Across Temperature

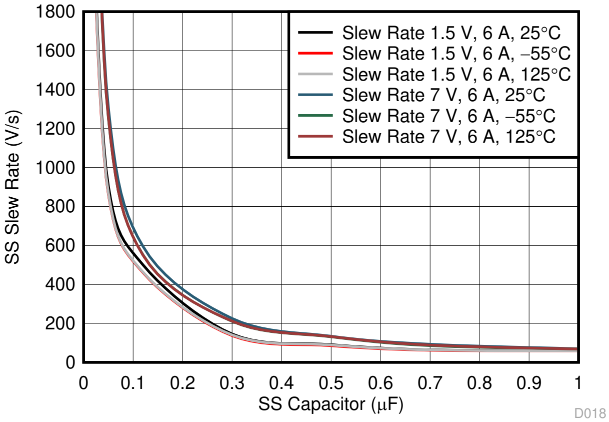


Figure 7-21. SS Slew Rate vs SS Capacitor Across Temperature

8 Parameter Measurement Information

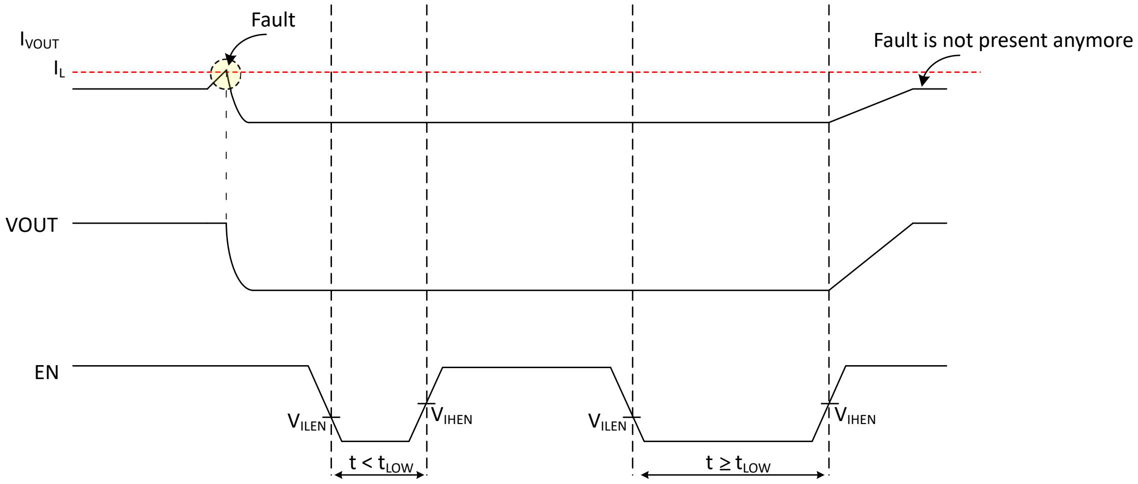


Figure 8-1. EN Signal Low Time to Restart Device (t_{LOW})

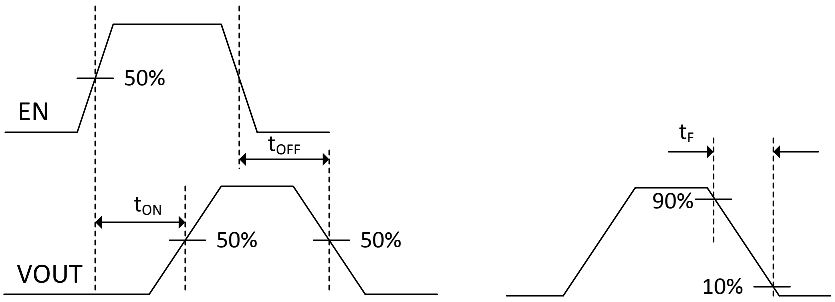


Figure 8-2. Turn-On (t_{ON}), Turn-Off (t_{OFF}) and VOUT Fall Time (t_F) Waveforms

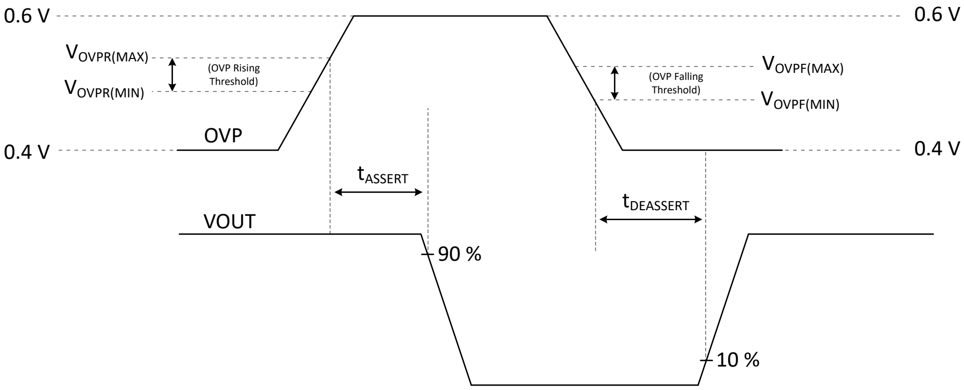


Figure 8-3. OVP Assert (t_{ASSERT}) and OVP Deassert ($t_{DEASSERT}$) Waveforms

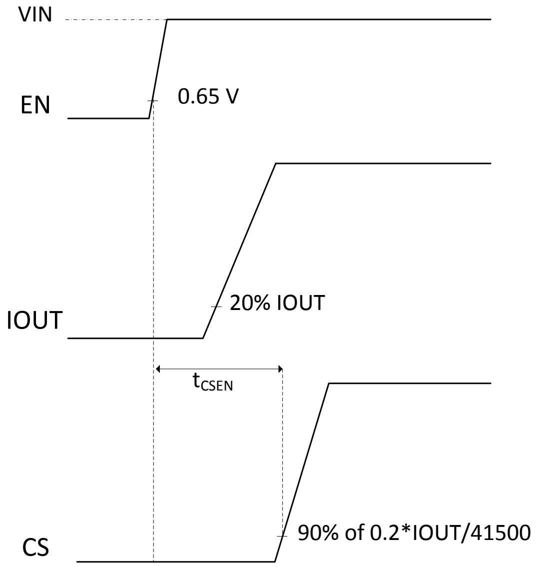


Figure 8-4. t_{CSEN} Waveforms

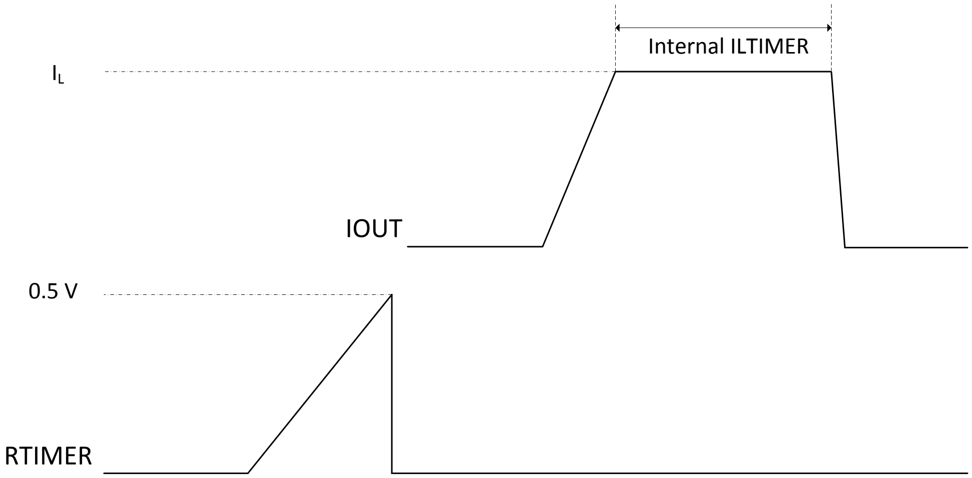


Figure 8-5. Internal ILTIMER Waveforms

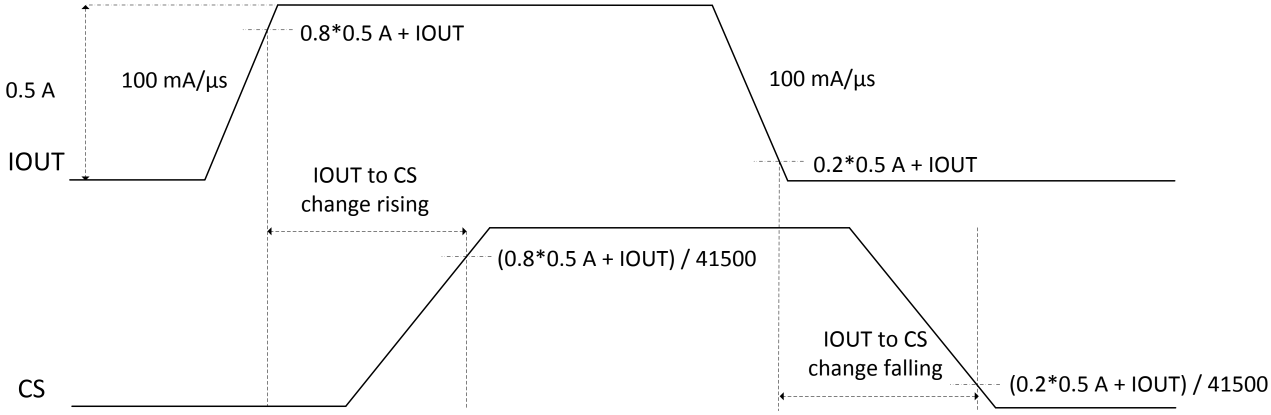


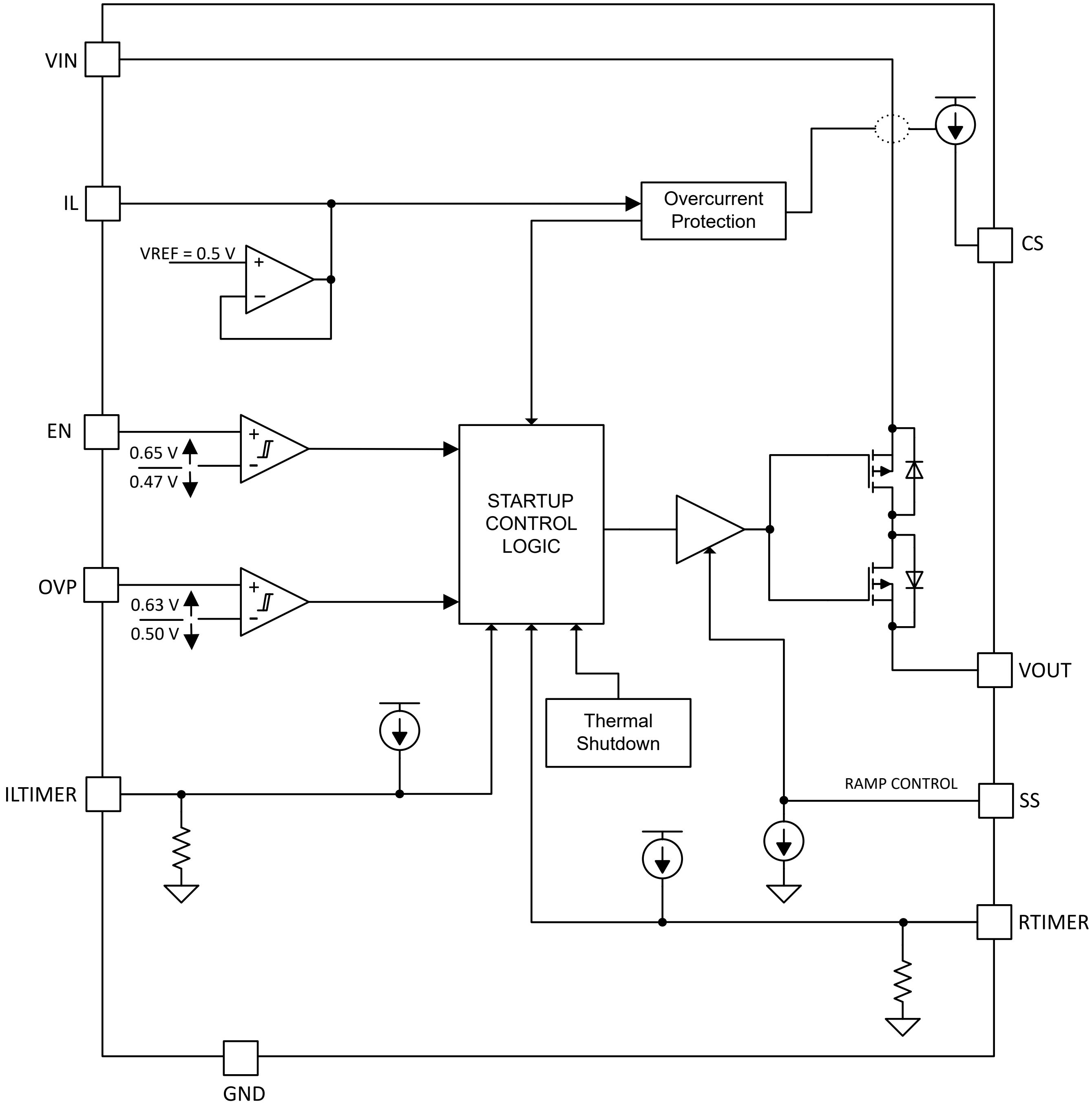
Figure 8-6. VOUT Current to CS Change Delay Time

9 Detailed Description

9.1 Overview

The TPS7H2201 device is a single channel, 6-A eFuse with a programmable slew rate for applications that require specific rise-time as well as programmable current limit for protection purposes. In addition, the TPS7H2201 features a reverse current protection capability for power distribution applications.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Enable, Undervoltage, and Overvoltage Protection

Figure 9-1 shows how resistor dividers from VIN connected to the EN and OVP pins can be used to set the UVLO and OVP trip voltages. The EN pin controls the ON and OFF state of the internal FET. A voltage at this pin greater than V_{IHEN} turns on the FET and a voltage less than V_{ILEN} turns it off. The addition of an external resistor divider from VIN allows the EN pin to configure a different enable rising voltage or an undervoltage monitor (UVLO) based on the V_{IHEN} and V_{ILEN} specifications respectively. Typically, applications are optimized to either configure the enable rising voltage or the UVLO threshold. As an example, Equation 1 can be used to calculate the UVLO trip point fixing R_{TOP_EN} = 100 kΩ.

In a similar way to the EN pin, the overvoltage protection (OVP) feature of the device can be configured using a resistor divider from VIN connected to the OVP pin. The trip voltage for the OVP has to be less than the absolute maximum VIN voltage. A voltage at the OVP pin greater than V_{OVPR} will trip the OVP feature and will turn off the FET and a voltage less than V_{OVPF} will keep the FET on. If this feature is not desired, the OVP pin should be grounded. Equation 2 can be used to calculated the rising OVP trip point fixing R_{TOP_OVP} = 100 kΩ.

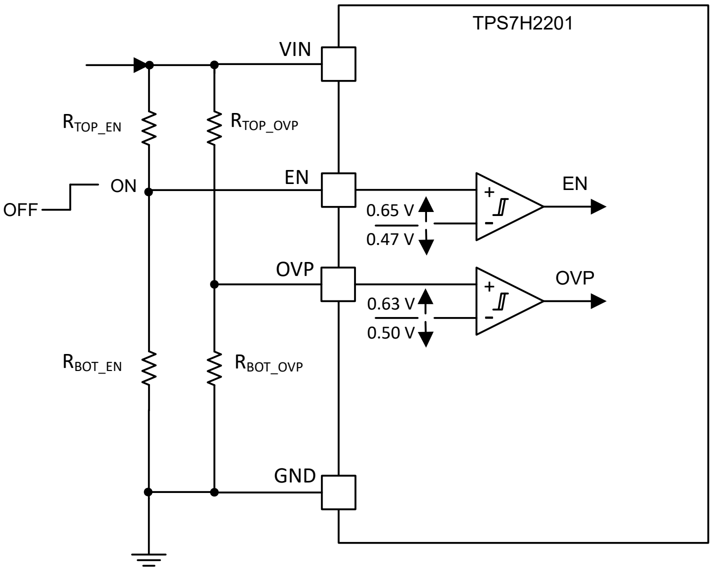


Figure 9-1. UVLO and OVP Thresholds Set by Resistor Dividers

$$R_{BOT\_EN}\,(k\Omega) \le \frac{47}{V_{UVLO\_TRIP}\,(V) - 0.47} \tag{1}$$

$$R_{BOT\_OVP}\,(k\Omega) \ge \frac{63}{V_{OVP\_TRIP}\,(V) - 0.63} \tag{2}$$

9.3.2 Adjustable Rise Time

An external capacitor, C_{SS}, connected between the VOUT and SS pins sets the slew rate. The desired slew rate $VOUT_{SR}$ is determined by t_r, the rise time in seconds, and ΔV, the change in VOUT voltage in Volts as shown in Equation 3.

$$VOUT_{SR}\,(V/s) = \frac{\Delta V_{OUT}\,(V)}{t_r\,(s)} \tag{3}$$

In order to avoid false trips due to the programmable current limit, the desired slew rate must be less than $VOUT_{SR,MAX}$ as shown in Equation 4, where I_L is the programmed current limit, I_{VOUT} is the normal operation current flowing through the switch, and C_{OUT} is the output capacitor.

$$\mathrm{VOUT_{SR,MAX}}\ (\mathrm{V/s}) < \frac{0.8 \times \mathrm{I_L}\ (\mathrm{A}) - 0.95 \times \mathrm{I_{VOUT}}\ (\mathrm{A})}{\mathrm{C_{OUT}}\ (\mathrm{F})} \tag{4}$$

Once the slew rate has been calculated and meeting the constraint in Equation 4, the C_{SS} capacitor is then calculated using Equation 5 for VIN < 3-V and IOUT ≥ 3-A applications. For all other applications, use Equation 6.

$$\mathrm{C_{SS}}\ (\mu\mathrm{F}) = \frac{45}{\mathrm{VOUT_{SR}}\ (\mathrm{V/s})} \tag{5}$$

for VIN < 3 V and IOUT ≥ 3 A

$$\mathrm{C_{SS}}\ (\mu\mathrm{F}) = \frac{65}{\mathrm{VOUT_{SR}}\ (\mathrm{V/s})} \tag{6}$$

for all other conditions

9.3.3 Programmable Current Limiting

A current limit can be programmed using an external resistor connected from the IL pin to GND. This programmed current limit (±20% accurate) refers to the continuous current through the device and therefore, when operated at its maximum current rating (6 A), the programmed current limit needs to be set 20% higher. As shown in Figure 9-2, a current limit event of this nature is defined as a soft short. The resistor value R_{IL}, can be calculated using Equation 7 for VIN ≤ 3 V, and Equation 8 for VIN > 3 V, where I_L is the programmed current limit value in amperes. This programmable current limiting feature is different from the internal current limiting activated during fast trip mode as shown in Figure 9-3. A current limit event in this case is defined as a hard short and this current limit (typical of 22 A) cannot be programmed.

$$\mathrm{R_{IL}}\ (\Omega) = \frac{45500}{\mathrm{I_L}\ (\mathrm{A})} \tag{7}$$

for VIN ≤ 3 V

$$\mathrm{R_{IL}}\ (\Omega) = \frac{49000}{\mathrm{I_L}\ (\mathrm{A})} \tag{8}$$

for VIN > 3 V

9.3.4 Programmable Fault Timer

A capacitor connected from the ILTIMER pin to GND determines the programmable current limit fault time duration. The ILTIMER pin will charge the capacitor to 0.5 V during an overload condition and will discharge it otherwise through an internal pull down resistance. The time that the device will be in current limit before turning off is configured by $C_{ILTIMER}$ and the time can be calculated using Equation 9. Connecting this pin to VIN will cause the device to be disabled once the internal current limit timer expires as shown in Figure 8-5. However, connecting it to GND will disable the internal timer functionality completely and therefore, in the case of a short, the device will remain at the programmed current limit indefinitely. When using the internal timer, the programmable current limit may not have time to settle to its programmed value. Because of this, the programmable current limit could briefly fall outside of its defined accuracy threshold. The fast trip off current limit, however, will remain valid.

$$\mathrm{t}(\mu\mathrm{s}) = \frac{\mathrm{C(pF)}}{2} \tag{9}$$

The time that the device remains disabled after the current limit timer expires is configurable through a capacitor connected from the RTIMER pin to GND. The RTIMER pin will charge the capacitor to 0.5 V after the switch is turned off and will discharge it otherwise. The time can be calculated using Equation 9. Connecting this pin to GND will keep the device disabled and it will require the device to be enabled by cycling the EN pin (Refer to EN Signal Low Time to Restart Device (t_{LOW})). The behavior of the ILTIMER and RTIMER pins for a soft short, hard short and internal timer conditions are shown in Figure 9-2, Figure 9-3, and Figure 9-4, respectively. Please notice that Figure 9-2 and Figure 9-3 assume the fault is not present after the switch has been disabled and enabled again (retry mode). If the fault is present after the retry mode, the device will go into current limit mode and this cycle will repeat until the fault is no longer present.

Table 9-1 and Table 9-2 summarizes the fault duration time and retry time based on the pin conditions.

Table 9-1. Fault time duration for ILTIMER pin conditions

ILTIMER pin Condition	Fault time duration during overload
VIN	15µs (typ), 35 µs (max)
GND	Indefinitely
Capacitor to GND ($C_{ILTIMER}$)	Equation 9
Float	Not Valid (Do not Float Pin)

Table 9-2. Time to retry during an overload condition for RTIMER pin conditions

RTIMER pin condition	time to retry during an overload
GND	Disabled (switch off) until EN is low for t > t_{LOW} (20µs)
Capacitor to GND (C_{RTIMER})	Equation 9
Float	Not Valid (Do not Float Pin)

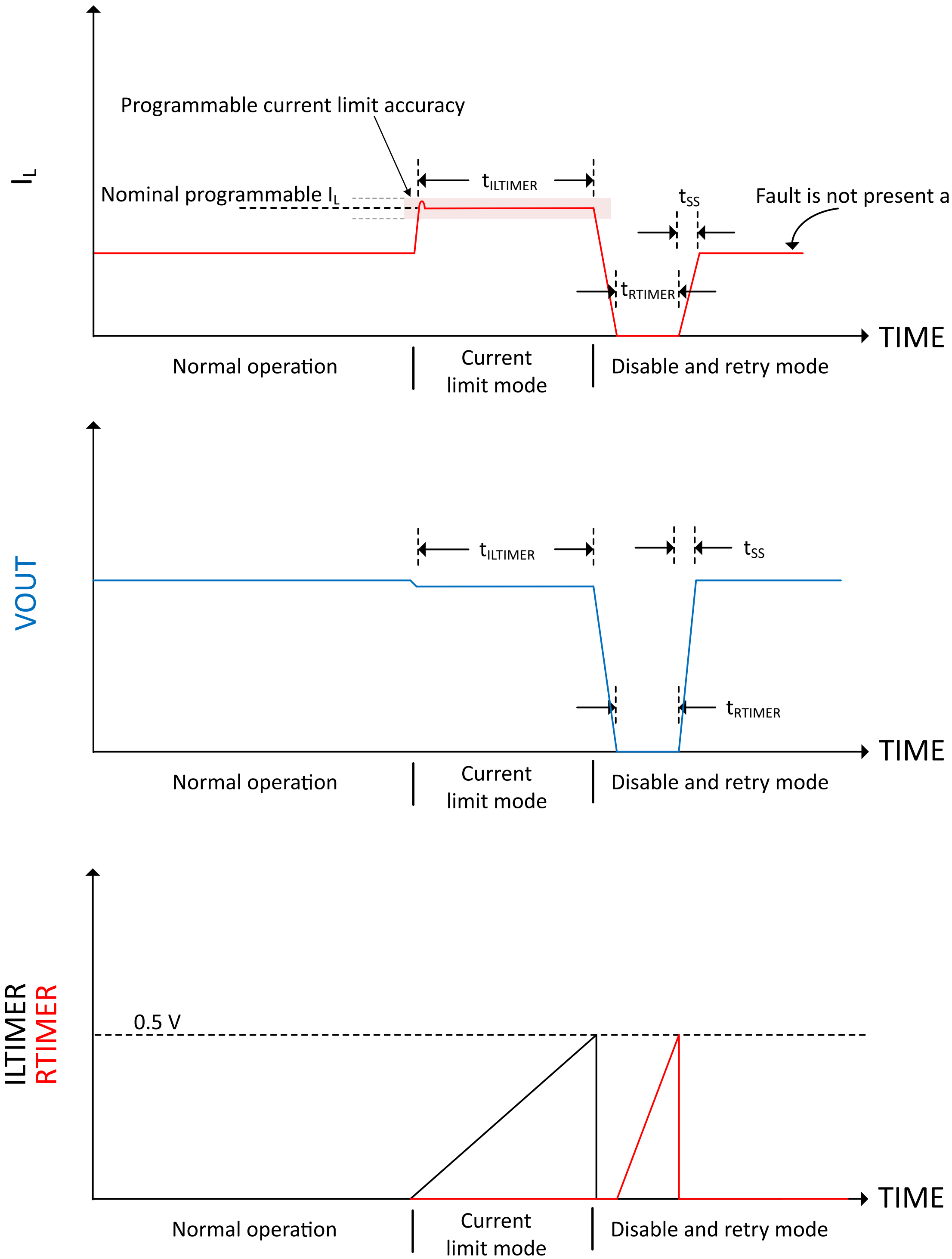


Figure 9-2. Soft Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

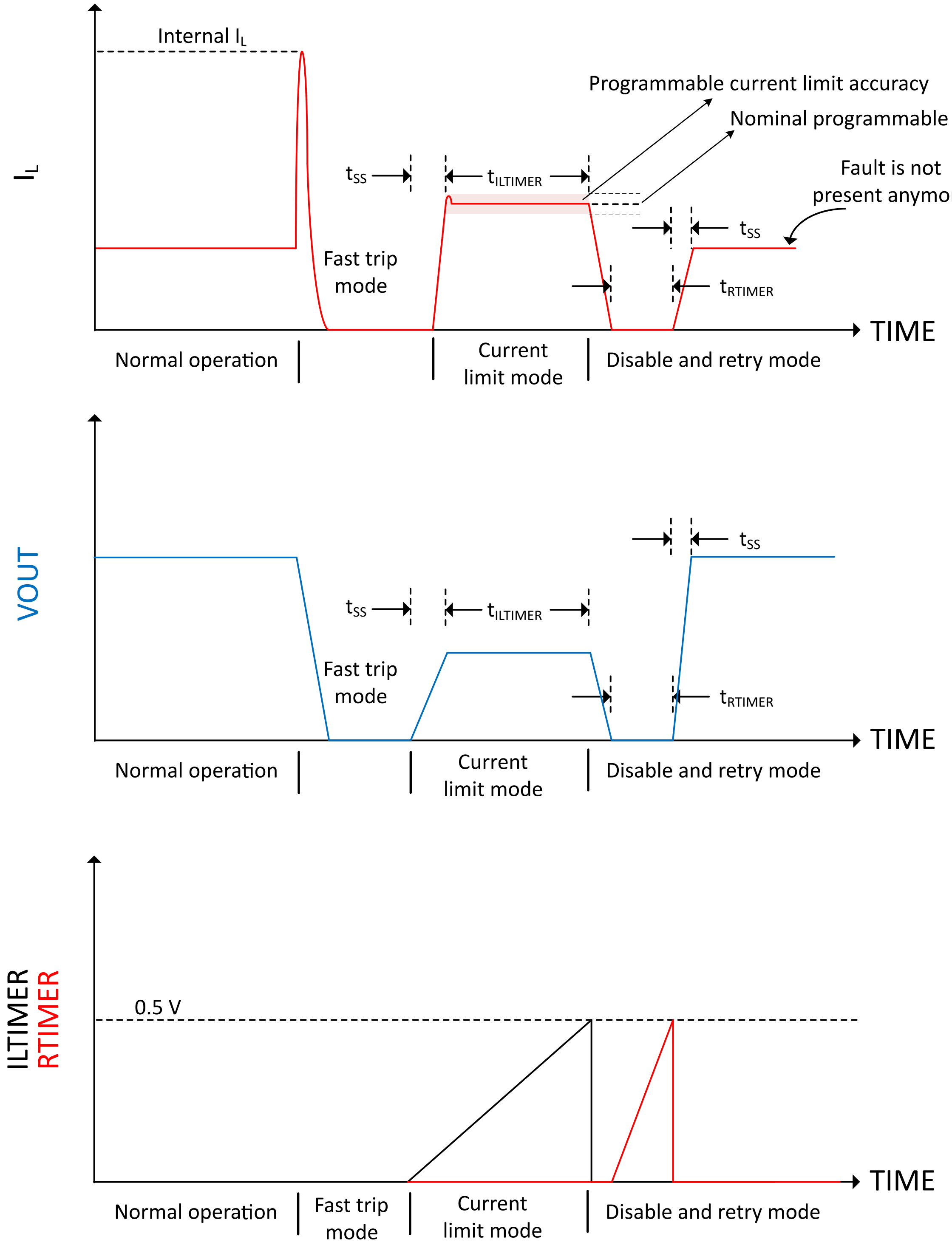


Figure 9-3. Hard Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

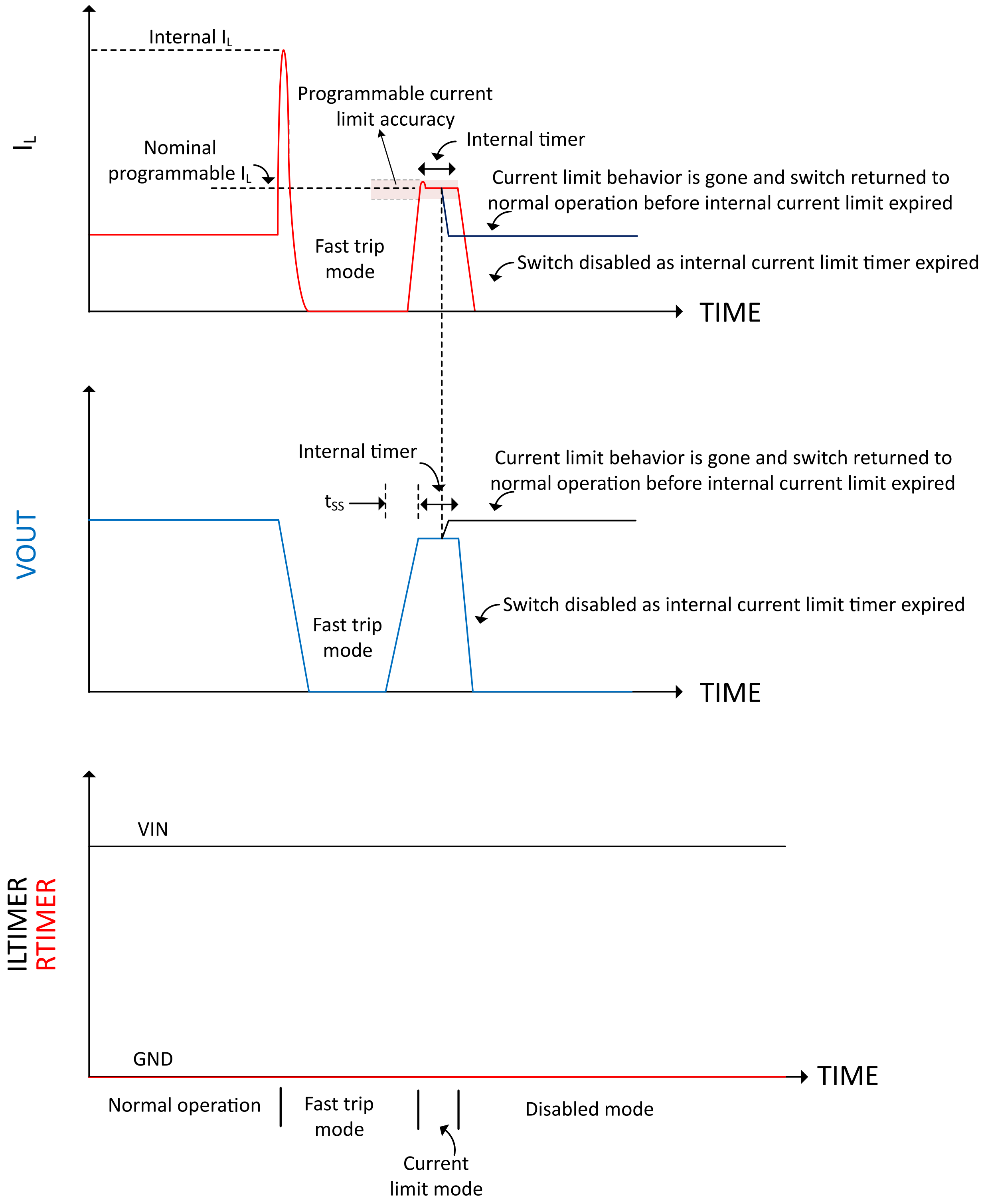


Figure 9-4. Programmable Fault Timer Operation Using the Internal Current Limit Timer and Disabling the Retry Mode

The programmable fault timers, ILTIMER and RTIMER, should be set in such a way that the capacitor for one timer is discharged before the other timer expires to ensure proper operation. In the specific case of using the internal ILTIMER, the RTIMER capacitor should be sized such that it is discharged before the internal ILTIMER expires, assuming the fault is still present. Figure 9-5 shows a situation where this constraint is not met as the RTIMER is much larger than the ILTIMER and therefore, the C_{RTIMER} is not discharged before the

$C_{ILTIMER}$ reaches 0.5 V, which is when the ILTIMER will expire. In order to avoid this situation, the constraint shown in Equation 10 must be met. Using this equation, once a capacitor for a timer has been selected (C_1 in Equation 10), the maximum value for the capacitor of the second timer can be determined. The internal pull-down resistance for each of the timers can be found in the table. For the situation shown in Figure 9-5, C_1 and R_{PD1} in Equation 10 correspond to the RTIMER.

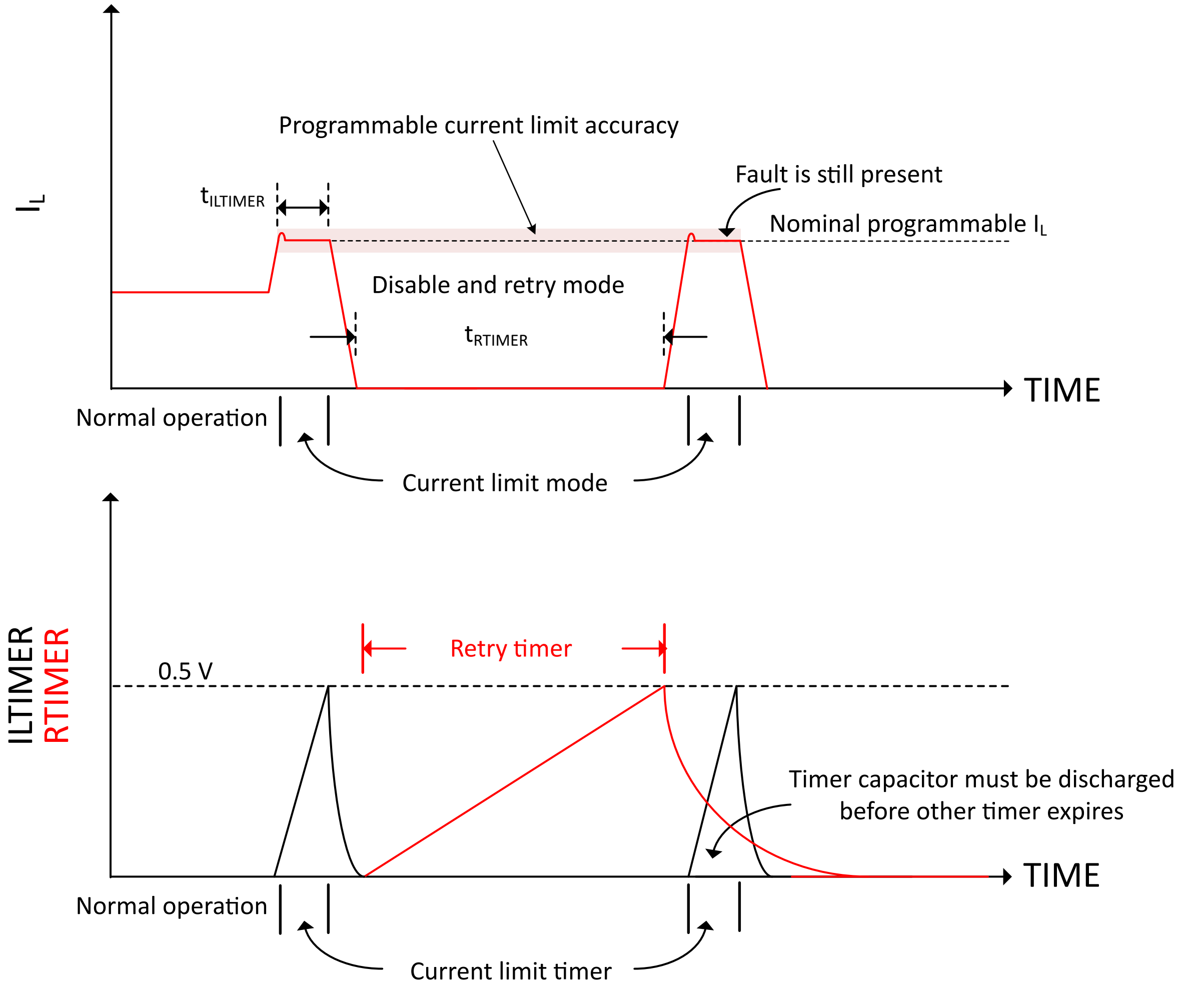


Figure 9-5. Programmable Fault Timer Capacitors Constraint

$$C_1(\mu F) < \frac{C_2(pF)}{8 \times R_{PD\,1}(\Omega)} \tag{10}$$

9.3.5 Current Sense

This pin will output a current proportional to the output current of the switch for current sensing applications. A resistor to GND will convert this current to voltage for current sensing purposes. The output current will be the switch current divided by 41,500. The CS pin will have a valid output 5 ms after the device has been enabled. To operate the current sense in the linear region, the voltage at the CS pin at the application maximum load, should not exceed the CS pin voltage sepcification (VIN - 400 mV).

9.3.6 Parallel Operation

The TPS7H2201 can be configured in parallel operation either to increase the current capability, up to 12 A, or to reduce the on-state resistance. In this case, all pins are shared as shown in Figure 9-6, except the current limit resistor (R_{IL}) for proper operation of the internal current limit loop. The current limiting resistors must be sized as described in the *Section 9.3.3* section.

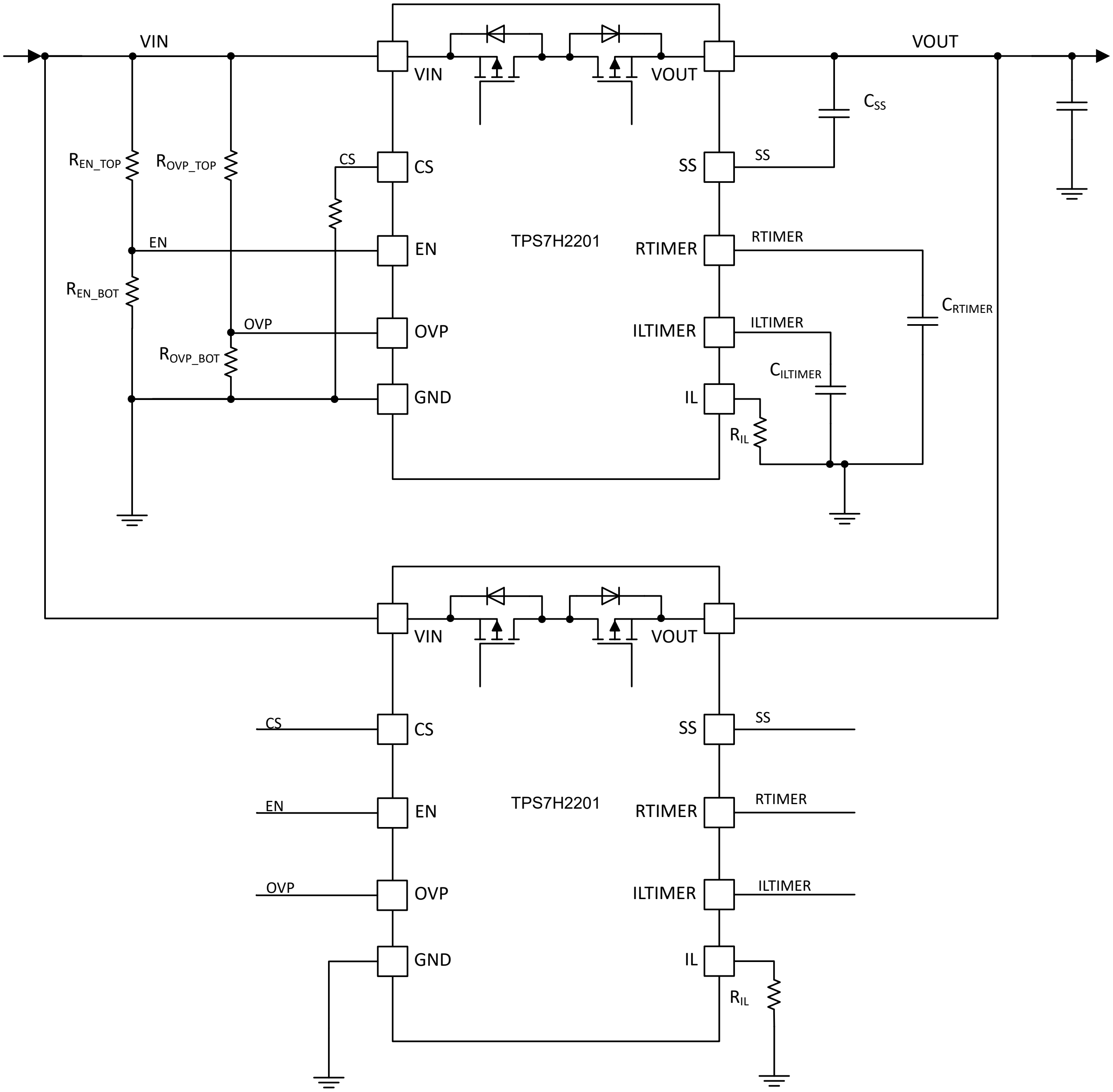


Figure 9-6. Parallel Configuration to Reduce Resistance or Increase Current Capability

9.3.7 Reverse Current Protection

The TPS72201 eFuse features back to back FETs to prevent current flow from VIN to VOUT and from VOUT to VIN when the switch is disabled (excluding leakage currents). This supports cold sparing (redundancy) applications. For example, VOUT may be up to 7 V while VIN is between 0 V and 7 V. In all cases, only small leakage current will result.

9.3.8 Forward Leakage Current

When VIN is powered but the TPS7H2201 is disabled (EN is low), the internal FETs are disabled, creating a high impedance path from VIN to VOUT. However, there are parasitic leakage paths that can cause VOUT to slowly charge. The forward leakage current, I_F, indicates how much current flows from VIN to VOUT during this situation. The maximum forward of the TPS7H2201-SP current is specified at 250 μA across voltage, temperature and radiation.

Some applications need to pay particular attention to this behavior. Is particularly relevant when VOUT is a high impedance node (and therefore the leakage current goes entirely to charging VOUT instead of being dissipated). By using the basic capacitor equation shown in Equation 11, the time for the voltage to rise to a given value can be theoretically calculated.

$$\Delta t = \Delta V_{OUT} \times C_{OUT} / I_F \tag{11}$$

where

- Δt = time to charge to final value
- ΔV_{OUT} = change in output voltage; for a 0 V starting voltage, use V_{IN}

For example, with a 7-V input voltage and a 220-μF output capacitance, VOUT typically charge to 7 V in aproximatelly 6.2 seconds (using I_F = 150 μA, ΔV_{OUT} = 7 V, C_{OUT} = 220 μF).

If the output voltage must remain below a certain value, a pull-down resistor can be utilized with a value as calculated by .

$$VOUT_{LKG\_MAX} = I_F \times R_{PULL\_DOWN} \tag{12}$$

where

- $VOUT_{LKG\_MAX}$ = maximum output voltage due to leakage current, I_F
- R_{PULL_DOWN} = external pull-down resistor from VOUT to GND

For example, placing a 2.6-kΩ resistor between VOUT and ground makes sure VOUT does not rise above 0.65-V worse case due to the I_F current. The resistor need to be able to handle the worst case power dissipation when the switch is enabled and VOUT ≈ VIN.

9.4 Device Functional Modes

VOUT Connection due to V_{EN} and V_{OVP} lists the VOUT pin state as determined by the EN and OVP pin voltages.

Table 9-3. VOUT Connection due to V_{EN} and V_{OVP}

EN PIN	OVP PIN	TPS7H2201-SP and TPS7H2201-SEP (5) (6)
0 (1)	0 (3)	Open
0	1 (4)	Open
1 (2)	0	VIN
1	1	Open

(1) $V_{EN} < V_{ILEN(MIN)} = 0$
(2) $V_{EN} > V_{IHEN(MAX)} = 1$
(3) $V_{OVP} < V_{OVPF(MIN)} = 0$
(4) $V_{OVP} > V_{OVPR(MAX)} = 1$
(5) Refer to Turn-On (t_{ON}), Turn-Off (t_{OFF}) and VOUT Fall Time (t_F) Waveforms for more details.
(6) Refer to OVP Assert (t_{ASSERT}) and OVP Deassert ($t_{DEASSERT}$) Waveforms for more details.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS7H2201 device is a single channel, 6-A eFuse with multiple programmable features such as current limit, undervoltage and overvoltage, current limit and retry timers, and soft start. In addition, the TPS7H2201 features a reverse current protection capability for power distribution applications and current sensing for load monitoring purpose. The TPS7H2201-SP user's guide is available on the TI website, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*. The guide highlights standard EVM configurations, test results, schematic, and BOM for reference.

10.2 Typical Applications

In addition to the standard power management applications where a power switch can be used, there are 2 main applications in which the TPS7H2201 can be used in space power applications:

- Redundancy for primary and secondary voltage rails common in satellite applications
- Protection for critical or SEL sensitive loads

10.2.1 Redundancy

In applications where primary and secondary (redundant) power rails are present, the TPS7H2201 is ideal to implement redundancy because of its reverse current blocking capability. In this case, since the eFuse is placed at the input of the point of load regulator, the on-resistance of the switch is not as critical.

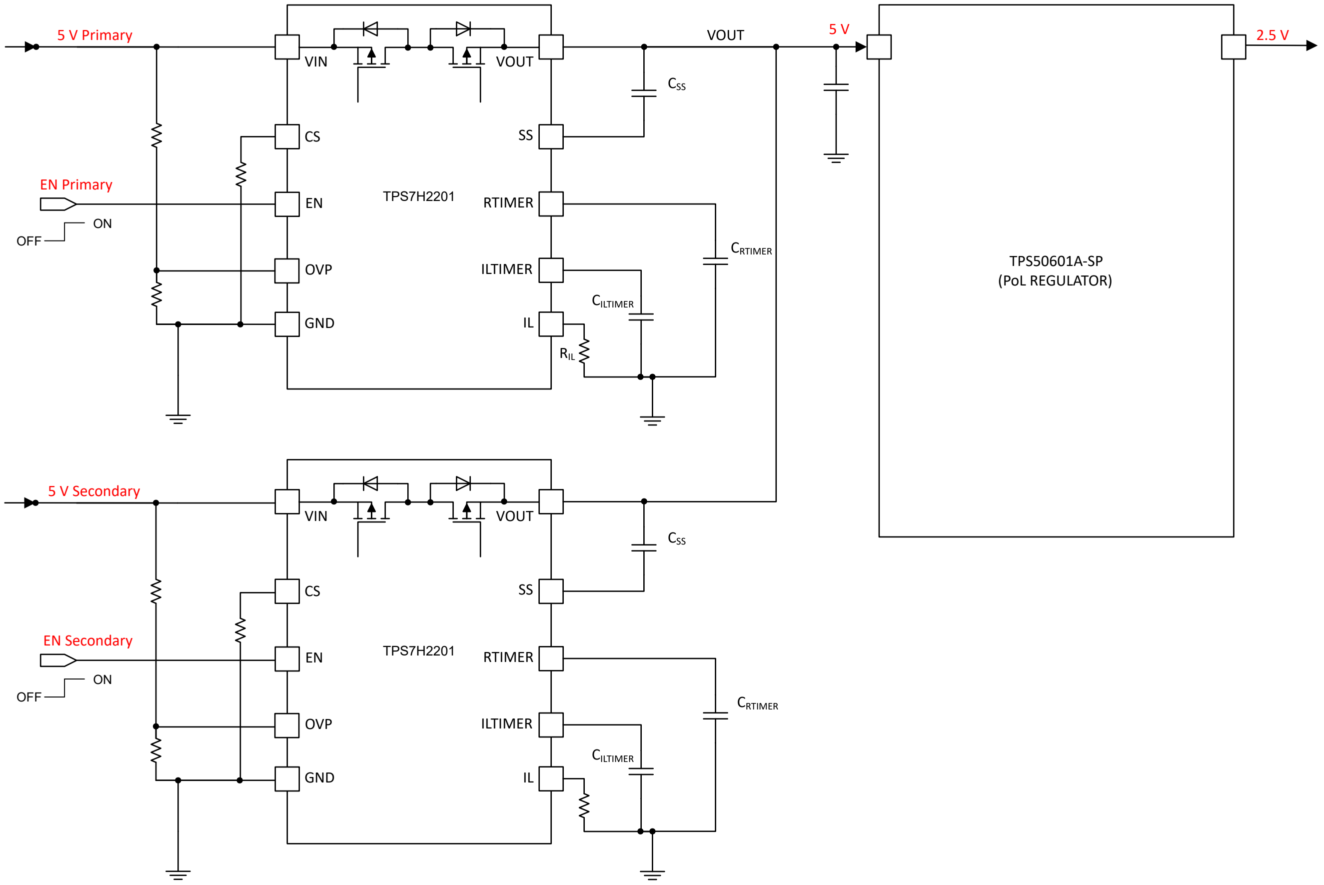


Figure 10-1. Redundancy Example Using the TPS7H2201

10.2.2 Protection

The protection features of the TPS7H2201 can also be used for SEL sensitive loads. In such case, the on-resistance of the switch might be more relevant as it is placed after the point of load regulator but in such case, two eFuse can be placed in parallel to reduce the on-resistance if needed. The main advantages of using the eFuse at this location is faster response to SEL events and automatic recovery due to the retry mode of the programmable fault timer.

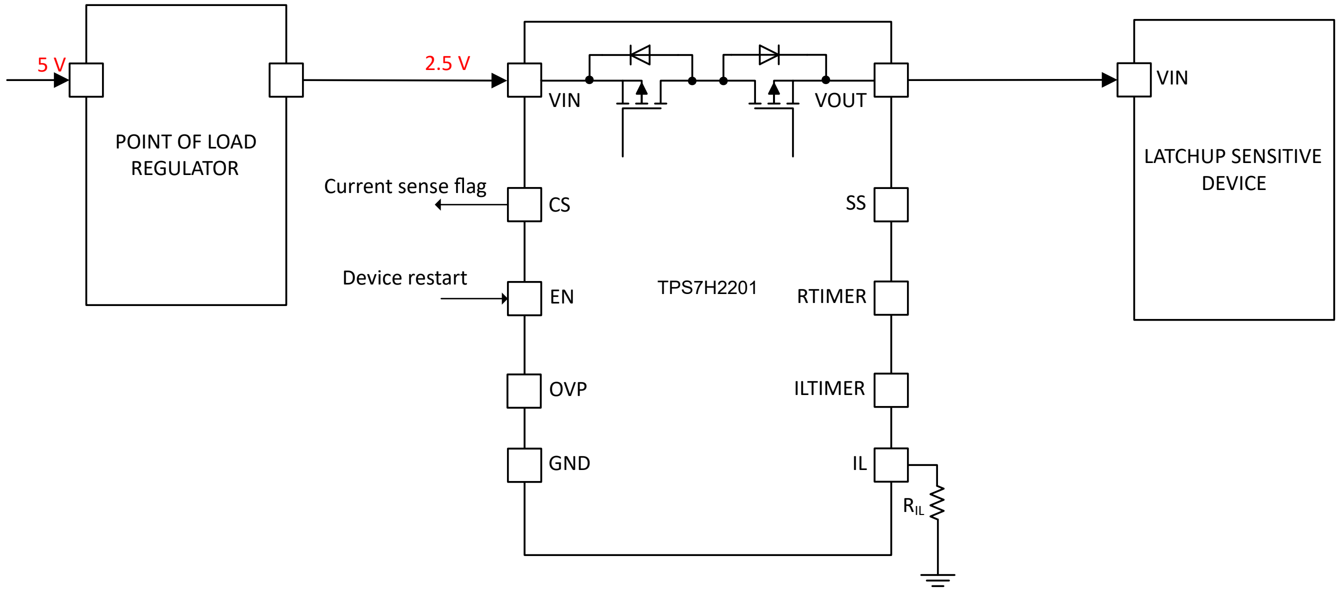


Figure 10-2. Protection Example Using the TPS7H2201

10.2.3 Design Requirements

Figure 10-3 shows a typical application schematic that is applicable to both the redundancy and the protection applications previously discussed.

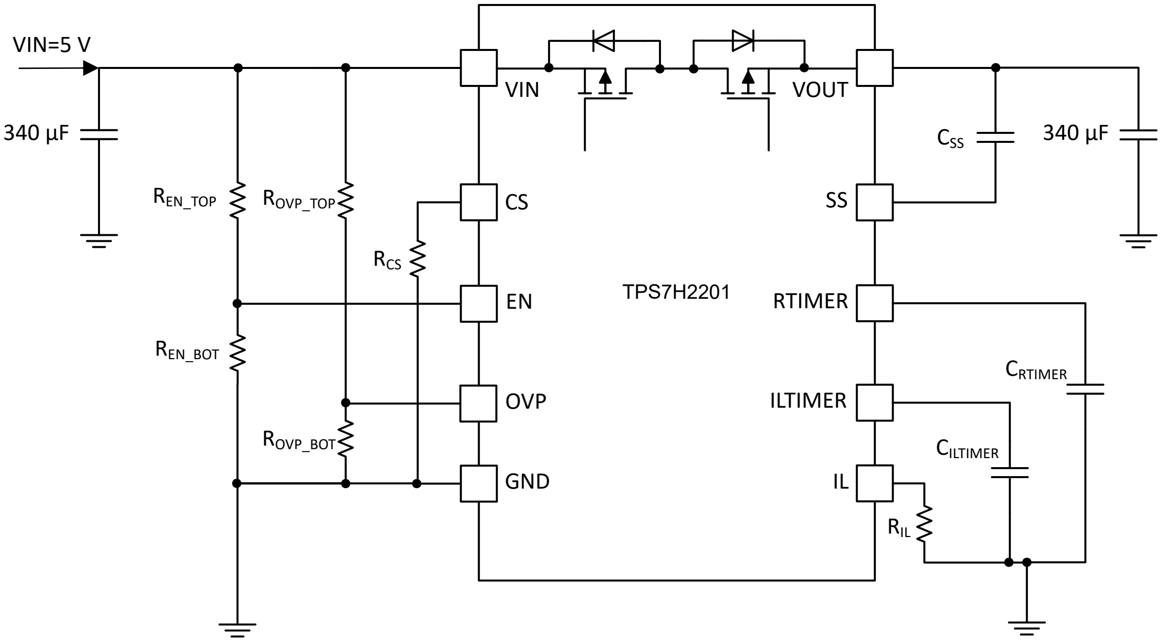


Figure 10-3. Typical Application Schematic

Table 10-1 shows the design parameters.

Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN	5 V
Undervoltage lockout set point	3.5 V
Overvoltage protection set point	6.5 V

Table 10-1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Output current	6 A
Current limit	7.5 A
Current limit timer	1 ms
Retry timer	1 ms
Soft start time	9 ms
Input and output capacitors	340 µF

10.2.4 Detailed Design Procedure

10.2.4.1 Undervoltage Lockout

The undervoltage lockout set point is configured using the resistor divider, R_{EN_TOP} and R_{EN_BOT} connected to the EN pin. Set the R_{EN_TOP} = 100 kΩ and, using Equation 1, calculate the value for R_{EN_BOT}. For an UVLO = 3.5 V, R_{EN_BOT} = 15.5 kΩ. When choosing the UVLO set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the V_{IHEN} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is smaller than the VIN used in the application. Equation 13 shows this VIN and V_{IHEN} requirement to set the UVLO point. For this particular application, the requirement is met as the result is 4.84 V.

$$V_{IHEN} \times \frac{R_{EN\_TOP} + R_{EN\_BOT}}{R_{EN\_BOT}} \leq VIN \tag{13}$$

10.2.4.2 Overvoltage Protection

In a similar way to the UVLO set point, the overvoltage protection set point is configured using the resistor divider, R_{OVP_TOP} and R_{OVP_BOT} connected to the OVP pin. Set the R_{OVP_TOP} = 100 kΩ and, using Equation 2, calculate the value for R_{OVP_BOT}. For an OVP = 6.5 V, R_{OVP_BOT} = 10.7 kΩ. When choosing the OVP set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the V_{OVPF} requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is larger than the VIN used in the application. Equation 14 shows this VIN and V_{OVPF} requirement to set the OVP point. For this particular application, the requirement is met as the result is 5.16 V.

$$V_{OVPF} \times \frac{R_{OVP\_TOP} + R_{OVP\_BOT}}{R_{OVP\_BOT}} \geq VIN \tag{14}$$

10.2.4.3 Current Limit

The current limit is configured using R_{IL}. Based on the output current for this design, the minimum current limit that can be programmed is IOUT + 1.5 A for a total of 7.5 A. As a result, using Equation 8, the resistor value is 6.53 kΩ.

10.2.4.4 Programmable Fault Timers

The programmable fault timers are configured using the $C_{ILTIMER}$ and the C_{RTIMER} capacitors. For this particular design, both timers are set to 1 ms. Therefore, using Equation 9, the value for each capacitor is 2000 pF. These capacitor values meet the requirement in Equation 10.

10.2.4.5 Soft Start Time

The soft start time is configured using the C_{SS} capacitor. In order to calculate the value of the capacitor, the VOUT slew rate needs to be calculated using Equation 3 to make sure the maximum VOUT slew rate requirement shown in Equation 4 is satisfied. This requirement is particularly important for space applications where large output capacitance is typically used, which translates to a lower maximum allowable VOUT slew rate. For this particular design, the VOUT slew rate is 555 V/s which is less than the maximum VOUT slew rate of 882 V/s, meeting the requirement from Equation 4. Now, the soft start capacitor value can be calculated as 117 nF using Equation 6, since VIN = 5 V for this application.

10.2.5 Application Curves

The power-up behavior of this design example is shown in Figure 10-4 and the current limit behavior is shown in Figure 10-5.

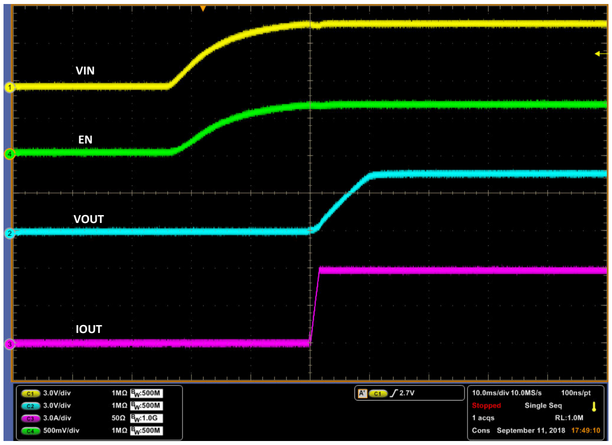


Figure 10-4. Power-up Behavior of the TPS7H2201-SP

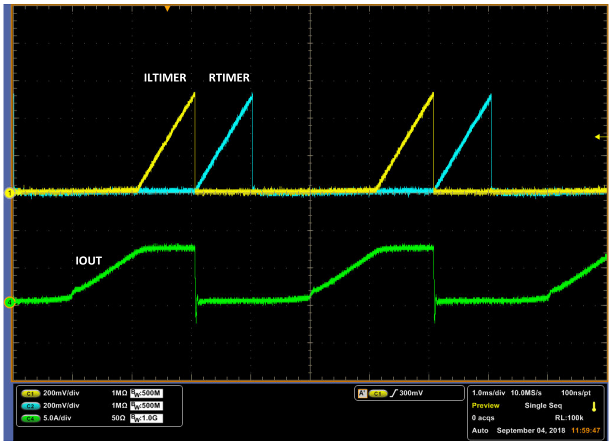


Figure 10-5. ILTIMER and RTIMER Waveforms When IL is Set to 7.5 A

10.3 Power Supply Recommendations

The TPS7H2201 is designed to operate from an input voltage supply range between 1.5 V to 7 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from VIN to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2201-SP Evaluation Module uses one 330-μF tantalum capacitor in parallel with one 10-μF and one 0.1-μF ceramic capacitor.

10.4 Layout

10.4.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects. In general, the components should be placed close to the device such that traces remain as short as possible to avoid parasitic capacitance. In addition, due to the possibility of large power dissipation in fault conditions (short at VOUT), thermal vias should be placed in the PCB for the thermal pad.

10.4.2 Layout Example

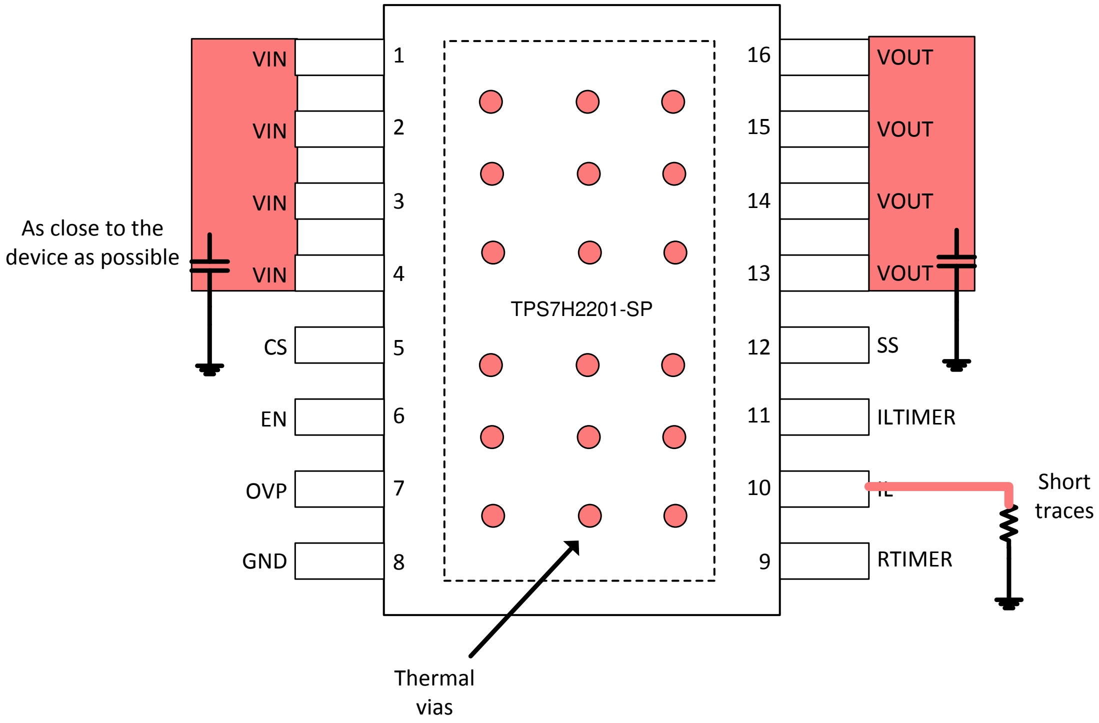


Figure 10-6. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H2201-SP Total Ionizing Dose (TID) Report*
- Texas Instruments, *Single-Events Effects Test Report of the TPS7H2201-SP eFuse*
- Texas Instruments, *TPS7H2201-SP Neutron Displacement Damage Characterization*
- Texas Instruments, *TPS7H2201EVM-CVAL Evaluation Module (EVM) User's Guide*
- Texas Intruments, Unencrypted PSpice Transient Model
- Texas Intruments, *Load Switch Thermal Considerations*
- Texas Intruments, *Basics of eFuses*
- Texas Intruments, *Basics of Load Switches*
- *Standard Microcircuit Drawing, 5962R17220*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962-1722001VXC TPS7H2201MHKRV	Samples
5962R1722001V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1722001VXC TPS7H2201MHKRV	Samples
TPS7H2201HKR/EM	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H2201HKREM	Samples
TPS7H2201Y/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

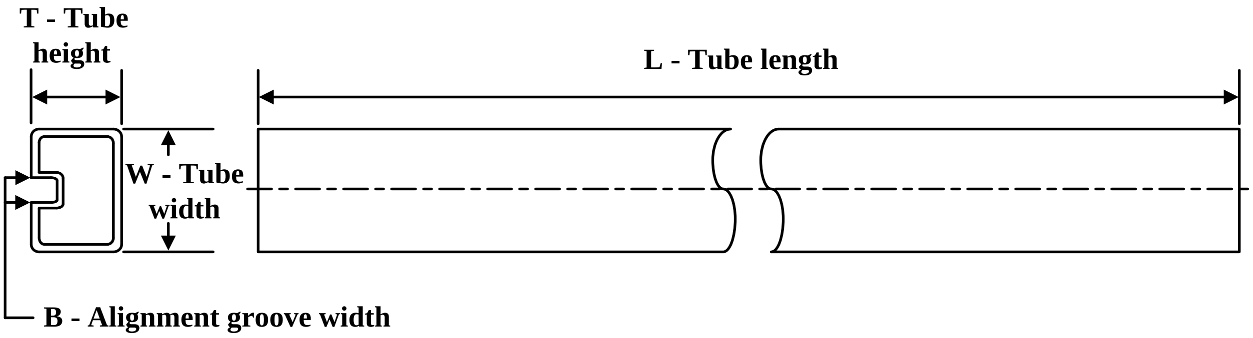
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

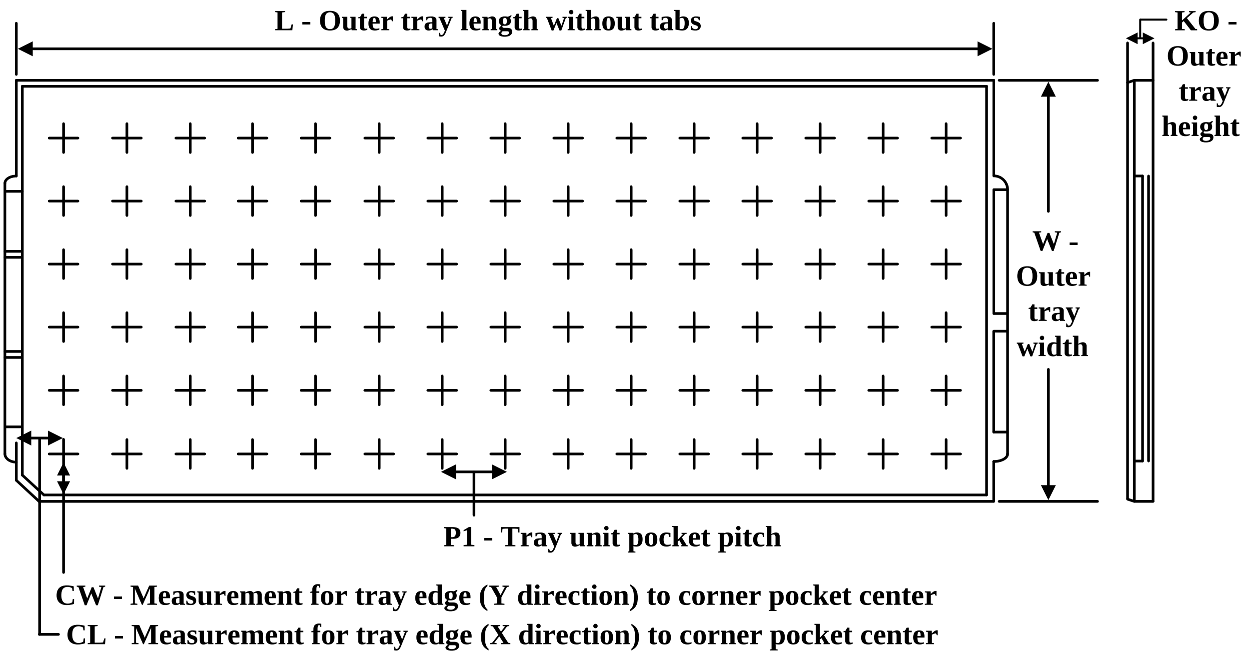
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
5962R1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
TPS7H2201HKR/EM	HKR	CFP	16	1	506.98	26.16	6220	NA

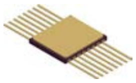
TRAY

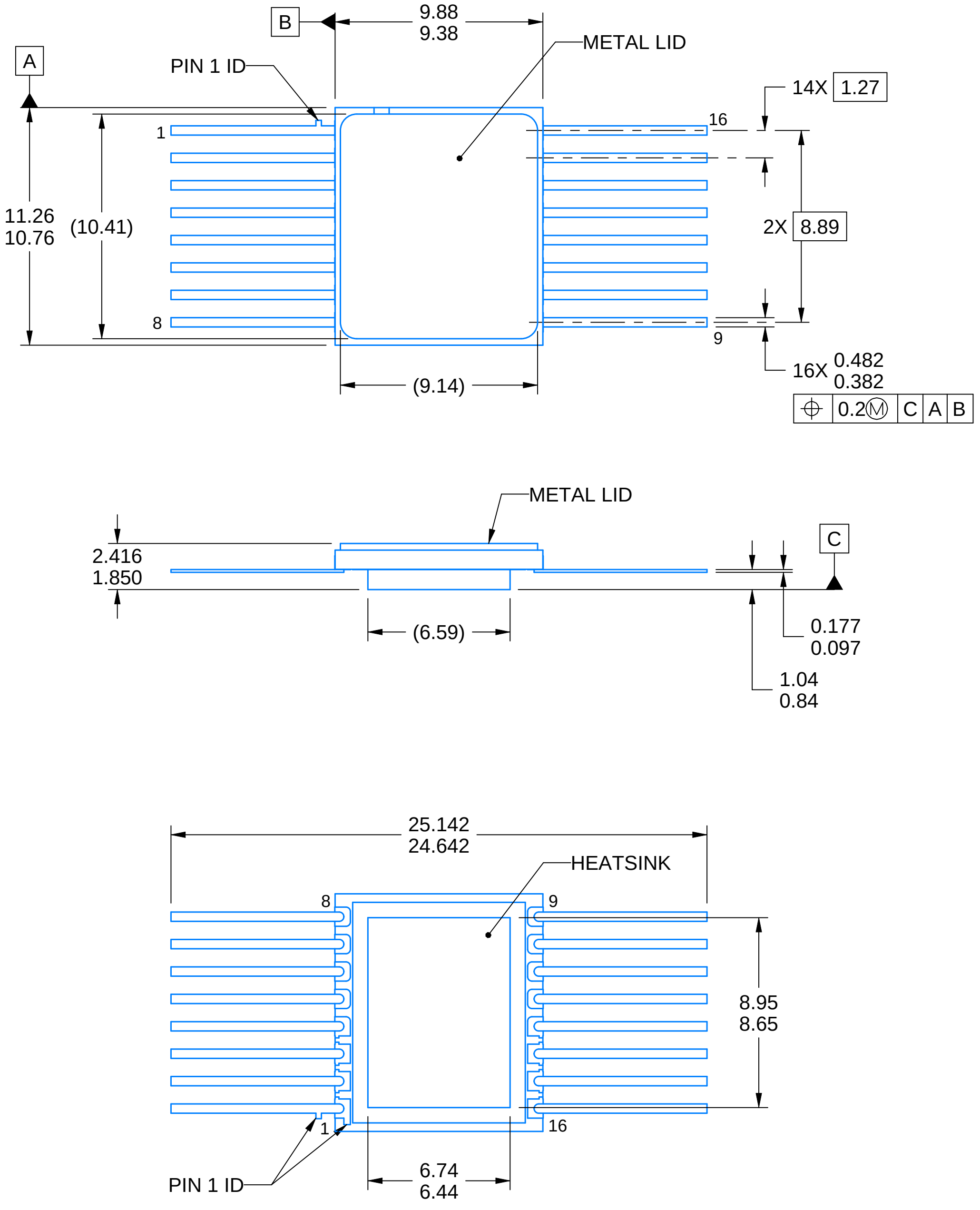


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS7H2201Y/EM	KGD	XCEPT	0	5	5 x 5	70	6.35	3.81	610	1.3	8.89	8.13

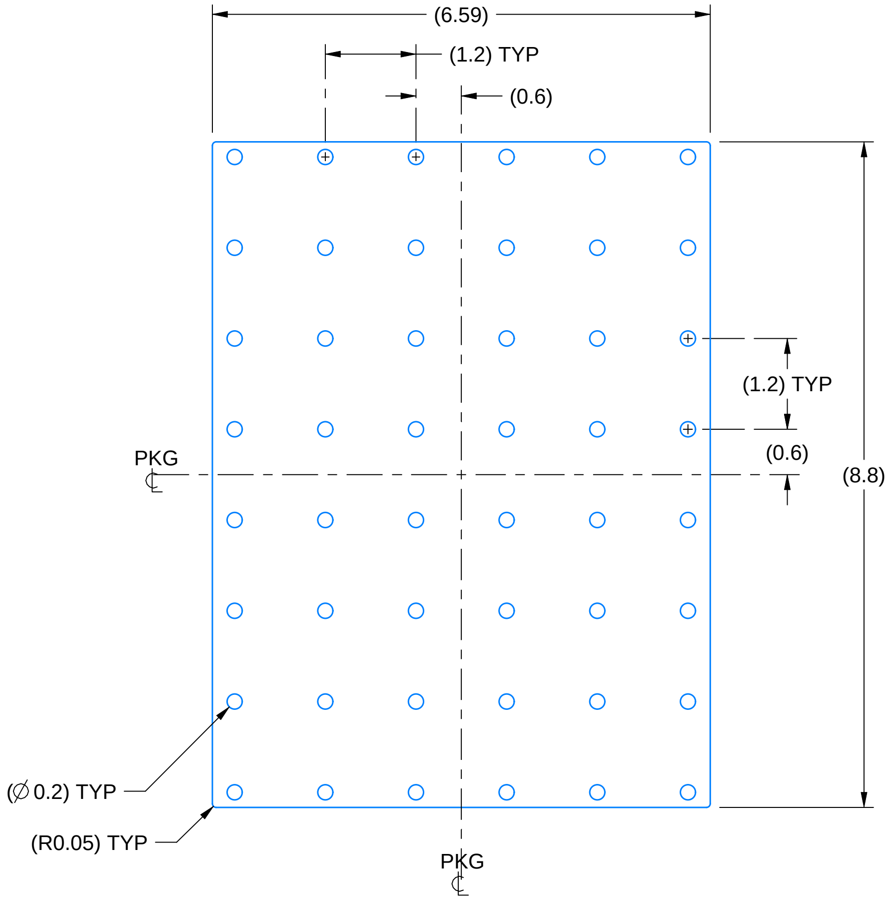




4226020/C 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated