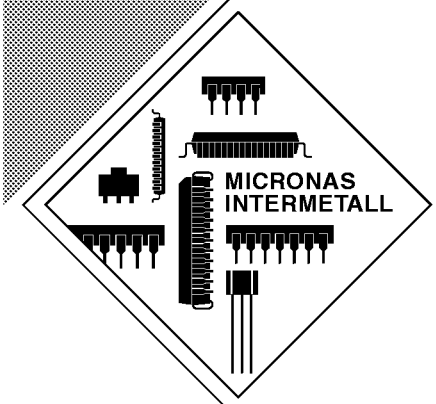


PRELIMINARY DATA SHEET

TPU 3035,
TPU 3040,
TPU 3050
Teletext Processors

Edition Feb. 23, 1999
6251-349-6PD

MICRONAS
INTERMETALL

Contents

Contents, continued

Multistandard Teletext Processor for Level 1 and 2

Release Note:
This data sheet describes functions and characteristics of TPU3040–A25 and TPU3050–C4.

If not otherwise designated, the pin numbers mentioned refer to the 44-pin PLCC package. For corresponding PDIP and PSDIP numbers, see page 11. Revision bars indicate significant changes to the previous version.

1. Introduction

The TPU 3040 is a single chip World System Teletext (WST) decoder for applications in analog and digital TV sets. Based on a 65C02 core with RAM and ROM on chip, an adaptive data slicer, a display controller, and a number of interfaces, the TPU 3040 offers acquisition and display of various teletext and data services such as WST, PDC, VPS, and WSS.

1.1. Features

The TPU 3040 is an integrated circuit designed in CMOS technology. As a stand-alone system or in combination with the DIGIT 3000 system, the TPU 3040 offers a wide range of new and interesting features, some of them unique in comparison with other products on the market.

The TPU 3035 is a stripped-down version of TPU 3040, designed for low-cost applications. The basic chip architecture remains unchanged, whereas some of the more sophisticated features are removed.

The TPU 3050 offers all features of the TPU 3040 plus the possibility of connecting the SRAM instead of the DRAM memory.

This data sheet describes the full feature set of the TPU 3040. Differences between TPU 3035, TPU 3040, and TPU 3050 are denoted when necessary (see Table 1–1).

Table 1–1: Feature List

TPU	3035	3040	3050
Acquisition			
No. of analog comp. video inputs	1	2	2
Clamping	x	x	x
AGC	x	x	x
Sync. separation with PLL	x	x	x
Adaptive data slicer	x	x	x
Signal quality detection	x	x	x
PAL VBI acquisition	x	x	x
NTSC VBI acquisition	–	–	–
MAC VBI acquisition (PLCC44 only)	–	x	–
MAC packet text acquisition (PLCC44 only)	–	–	–
Full-field acquisition	–	–	–
Asynchronous acquisition and display	x	x	x
Ghost row acquisition	x	x	x
EPG support	–	x	x
Internal row 26 processing (extended character sets)	–	x	x
FLOF/TOP s/w support on chip	x	x	x
PDC acquisition	x	x	x
VPS acquisition	x	x	x
WSS acquisition	–	x	x
US captioning	–	x	x
Software acquisition (advanced header, magazine shuffle, ...)	x	x	x
Full parallel acquisition	x	x	x

Table 1–1, continued

TPU	3035	3040	3050
Display			
No. of different characters	512	512	512
No. of national language character sets	16	16	16
Character matrix size	10x10	10x10	10x10
No. of display rows	> 26	> 26	> 26
Pixel graphics	–	–	–
16:9 display (25% shrink)	–	x	x
1/2 screen display (50% shrink)	–	x	x
1/2 screen 16:9 display (62.5% shrink)	–	x	x
32 kHz mode	–	x	x
Non-interlace display	x	x	x
50/60 Hz display	x	x	x
100/120 Hz display	–	x	x
Scrolling vertical	x	x	x
Scrolling horizontal	–	–	–
Double height page display	x	x	x
Status row single height	x	x	x
Two page display side by side	–	–	–
Stable (line locked) display with noisy video	x	x	x
Display synchronized by input video	–	–	–
75 Ohm output	–	–	–
Half contrast RGB out	x	x	x
RGB level adjustable (externally)	–	–	–
Level 3 DRCS	–	–	–
Level 2 CLUT	D3000	D3000	D3000
Level 2 double width	x	x	x
Level 2 double height	x	x	x
Level 2 full screen color	x	x	x

TPU	3035	3040	3050
OSD – layer independent	x	x	x
Display priority via software-ID	D3000	D3000	D3000
RGB input from SCART and Fast Blank interface	x	x	x
Hardware cursor	–	–	–
Memory			
No. of pages on-chip	–	–	–
No. of pages off-chip	112	2032	2032
Minimum DRAM (ext.)	256 Kbit	256 Kbit	256 Kbit
Maximum DRAM (ext.)	1 Mbit	16 Mbit	16 Mbit
DRAM organization	1 bit	1 bit	1 bit
DRAM access time (page mode)	90 ns	90 ns	90 ns
Minimum SRAM (ext.)	–	–	256 Kbit
Maximum SRAM (ext.)	–	–	1 Mbit
SRAM organization	–	–	8 bit
SRAM access time	–	–	100 ns
Automatic memory/config. check	x	x	x
Variable no. of subpages (internal subpage management)	x	x	x
Constant page access time	x	x	x
Dyn. pg. storage (data compression)	–	–	–
General Product Info			
Supply voltage [V]	5	5	5
Power dissipation [mW]	250	250	300
Control bus	I^2C	I^2C	I^2C
IR decoder and control	–	–	–
Software macro interface	x	x	x
System clock [MHz]	20.25	20.25	20.25
Package	PDIP40	PLCC44 PDIP40	PSDIP52
Technology	0.8 µm CMOS	0.8 µm CMOS	0.8 µm CMOS

2. Functional Description

2.1. Conceptional Overview

The basic idea behind the TPU 3040 concept is the replacement of random logic by software. The still existing hardware supports the on-chip CPU in tasks with high data rates and ineffective software solutions. Typical tasks of a teletext decoder are listed below (realization on TPU 3040 in brackets):

– teletext data acquisition (hardware)
– teletext data decoding (software)
– page generation (software)
– page memory management (software)
– page display (hardware)
– user interface (software)

Fig. 2–1 shows the functional block diagram of the TPU 3040. The software approach is realized using a 65C02 core with RAM and program ROM on chip. Via the I/O, the CPU is connected to a DRAM interface. The DRAM contains an acquisition scratch buffer which is filled automatically by the teletext slicer circuit. After processing this scratch buffer, the CPU stores reorganized teletext lines into the page memory which takes up the greatest space in the DRAM capacity. A third part of the DRAM holds WST level 2 display data, which are read out by the WST layer. The CPU has to generate the display data by decoding teletext information from the page memory.

Apart from the WST layer, there is also one additional on-chip OSD layer. The OSD layer accesses the on-chip memory to read text and character font information. The RGB outputs of the OSD layer can have higher priority than the WST layer outputs. Thus it is possible to overlay the teletext display with an additional layer for user guidance.

The CPU memory contains RAM, program ROM and character ROM. The character ROM holds the font data and is separated from the program ROM to save CPU time. The CPU can still access the character ROM via a DMA interface including wait cycles. The WST layer and the additional OSD layer can also access the CPU memory via the same DMA interface.

The CPU is supported by some glue logic such as timer, watchdog and interrupt controller and communicates with the outside world via the I^2C-Bus.

2.2. Teletext Acquisition

The only task of the slicer circuit is to extract teletext lines from the incoming composite video signal and to store them into the acquisition scratch buffer of the external DRAM. No page selection is done at this hardware level.

Two analog sources can be connected, thus it is possible to receive text from one channel while watching another on the screen. After clamping and AGC amplifier the analog video signal is converted into binary data. Sync separation is done by a sync slicer and a horizontal PLL, which generate the horizontal and vertical timing. By these means no external sync signals are needed and any available signal source can be used for teletext reception.

The teletext information itself is acquired using adaptive slicers on bit and byte level with soft error detection to decrease the bit error rate under bad reception conditions. The slicer can be programmed to different bit rates for reception of PAL, NTSC or MAC world system teletext as well as VPS,WSS, or CAPTION signals.

2.3. Teletext Page Management

As a state-of-the-art teletext decoder the TPU 3040 is able to store and manage a sufficient number of teletext pages to absorb the annoying transmission cycle times. The number of available pages is only limited by the memory size. With an intelligent software and a 16 Mbit DRAM it is possible to store and to control more than 2000 teletext pages.

The management of such a data base is a typical software task and is therefore performed by the 65C02. Using a fixed length page table with one entry for every possible page, the software distributes the content of the acquisition scratch buffer among the page memory. The page size is fixed to 1 KByte, only ghost rows are chained in 128-byte segments to avoid unused memory space.

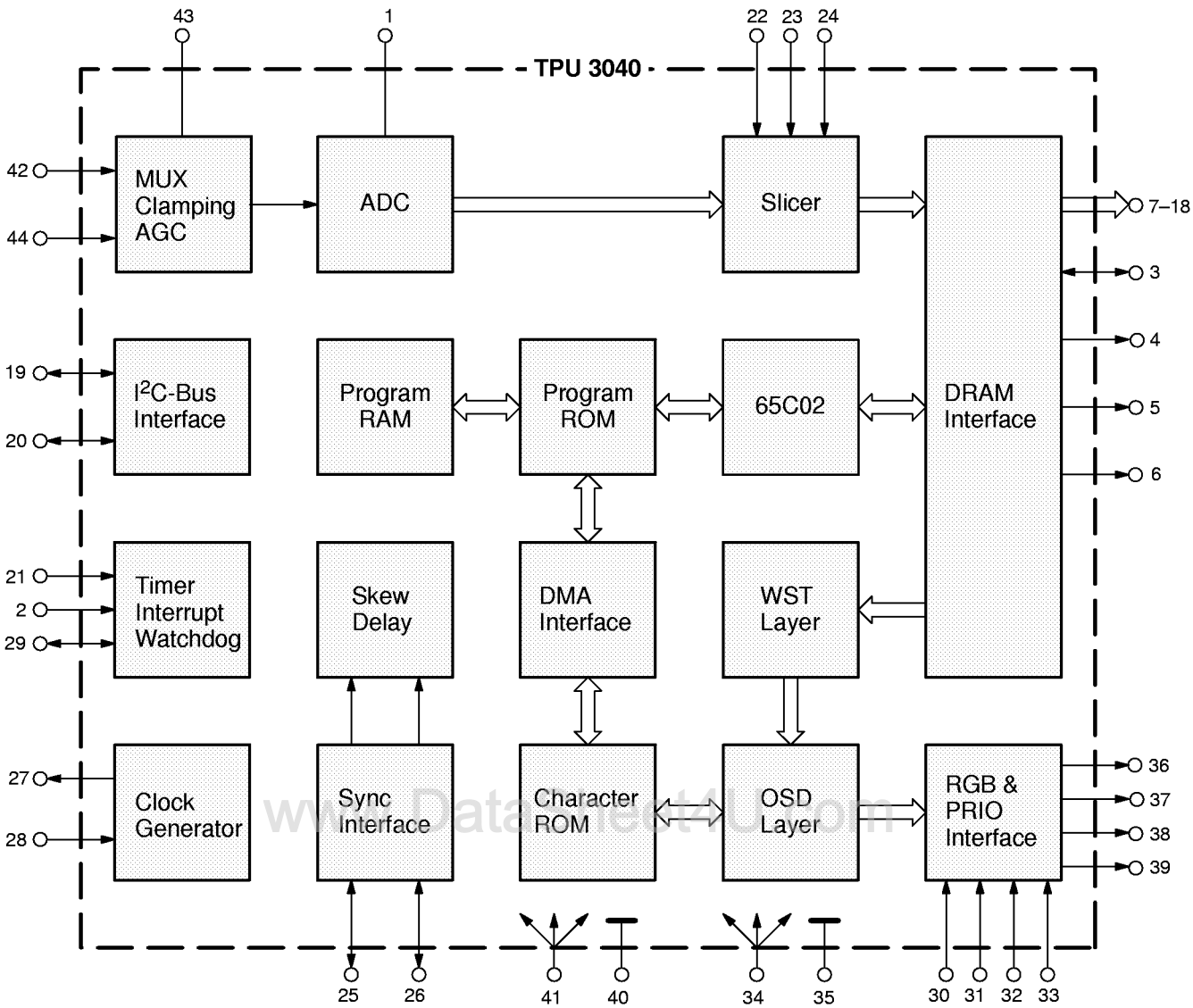


Fig. 2–1: Functional block diagram of the TPU 3040

2.4. Display Page Generation

A stored teletext page cannot be displayed directly, because of the row-adaptive transmission and the level 2 enhancements (row 26–29). Therefore the CPU has to generate a display page buffer, separated into level 1 data such as character codes and spacing attributes and into level 2 data, such as character set extension and non-spacing attributes. This is done by using a slightly modified stack model, in which one pointer bit for every character location indicates the presence of additional parallel attributes. Fig. 2–2 shows the organization of the stack row buffer. In this stack model the number of non-spacing attributes per row is limited to 40, which agrees with the WST and CEPT specification.

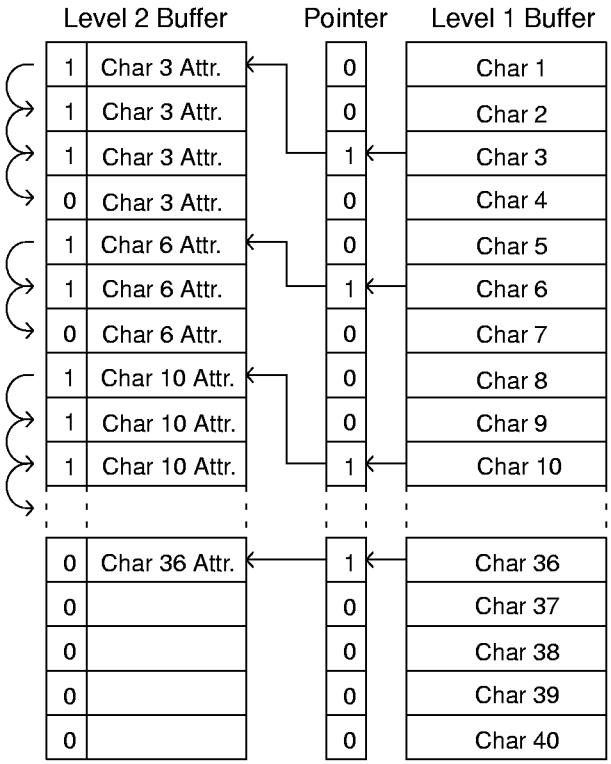


Fig. 2–2: Stack Row Buffer

2.5. WST Display Controller

The display controller includes two row buffers. The first row buffer holds a copy of a teletext row from the display page buffer. This decreases the data rate through the DRAM interface by a factor of 10 or 8, because new teletext row data is needed only after 10 lines in PAL or 8 lines in NTSC mode. The second row buffer stores all display attributes in parallel, to allow level 2 display without additional decoding.

To present a WST level 2 display, the teletext display controller has to evaluate the following attributes in parallel, that is for every character location:

– 10-bit character code

– 5-bit foreground color

– 5-bit background color

– 2-bit size

– 5-bit flash

– 1-bit invert

– 1-bit separated

– 1-bit conceal

– 1-bit underline

– 1-bit boxing/window

Additional attributes are defined to improve the display of CAPTION and OSD text:

– 1-bit italics

– 1-bit shadow

The display controller delivers 5-bit digital color information, a shadow signal for contrast reduction and a fast blank signal. The color bus can be used to address external color-look-up-tables (CLUT) which are part of modern digital TV systems, such as the DIGIT 3000. By this means, the full level 2 color spectrum can be displayed. For simple level 1 applications only 3 bits of the color bus are converted into analog RGB signals on chip.

2.6. Character Generator

Characters are displayed with a 10x10 pixel resolution in PAL and 10x8 pixel resolution in NTSC mode. Pixel clock is 10.125 MHz, derived from the main clock of 20.25 MHz. To get 10-bit pixel information two memory cycles are needed. The character font is part of the mask-programmable ROM, but supplied with its own bus structure (see Fig. 4–1). By this means the data transfer between character ROM and teletext display controller does not stop the CPU, which is important in the case of doubled line frequency.

Both bus structures are connected via a memory interface which allows cross-connections using DMA or wait cycles. As the number of addressable characters is 1024, the maximum character font size is 12800 byte. In this case part of the character font can be shifted into the program ROM which causes DMA cycles. Therefore only less frequently used characters should be placed into the program ROM. Vice versa seldom used CPU code can be put into the character ROM.

The WST specification defines a number of 7-bit code tables, which are filled with 96 characters only. In the G0 code table some characters have several language dependent variations. Additionally characters from the G0 code table can be combined with diacritical marks from the G2 code table (row 26). Thus it is not possible to simply transform the code tables into a continuous font ROM without getting unused ROM space and multiple defined character fonts.

The character ROM is optimized by reorganizing the code table structure of the WST specification. The whole character font is subdivided into blocks of 32 characters which are mapped to the WST character sets via a mask programmable mapping ROM (see Fig. 4–5). The character set selection is done via software.

2.7. OSD Layer

Apart from the WST layer, there is also one additional OSD layer on chip. The OSD layer accesses the CPU memory via DMA to read text and character font information. The RGB outputs of the OSD layer can have higher priority than the WST layer outputs. Thus it is possible to overlay the teletext display with an additional layer for user guidance (see Fig. 2–3).

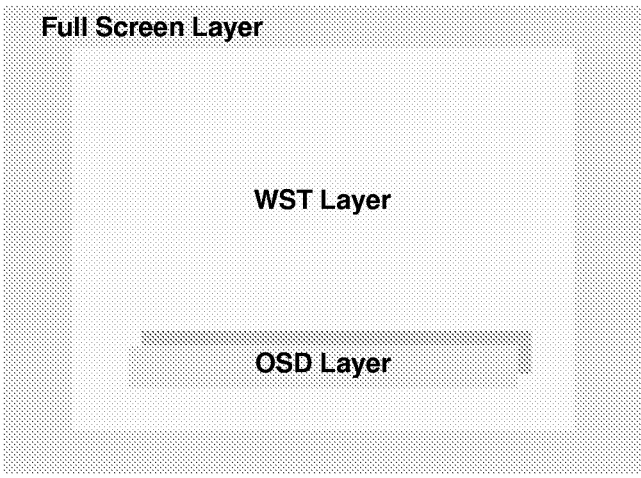


Fig. 2–3: Display Layer

2.8. DRAM Interface

The DRAM interface connects a standard DRAM to the internal bus structure. The address bus is 12 bit wide, addressing DRAMs up to 16 Mbit. Smaller DRAMs can also be connected. The maximum data throughput of the DRAM interface is 8.82 Mbit/s. This fast mode timing is adapted to DRAMS with page mode cycle time faster than 85 ns. In slow mode the data rate is 6.1 Mbit/s and the timing is adapted to DRAMS with a page mode cycle time faster than 120 ns. The data rate calculation already takes into account the required refresh cycles.

The DRAM interface has to handle 3 asynchronous data streams. The CPU needs access to every memory location of the DRAM. During VBI the slicer writes up to 22 teletext lines of 43 bytes into the acquisition scratch memory. Alternatively the slicer can store MAC packets of 90 bytes into the acquisition scratch. During text display the display controller copies teletext rows from display memory into its internal row buffer.

The lower data rate of the slow mode makes some restrictions necessary. With 6.1 Mbit/s it is no longer possible to run slicer and display in parallel. Only MAC packet teletext can still be acquired asynchronously because of the lower bit rate. VBI teletext can only be acquired while the display controller is inactive (synchronous acquisition and display).

2.9. SRAM Interface

The TPU 3050 is able to address either DRAM or SRAM memories. The DRAM interface can be switched into SRAM mode via I²C-Bus. The SRAM interface is inserted between the DRAM interface and the actual memory and demultiplexes the DRAM addresses into a single SRAM address and arranges the serial DRAM data into parallel data. Therefore, there is no gain in speed when SRAM is connected and slow SRAM types (100 ns) can be used. The internal, as well as the external controller software, does not see any difference between DRAM and SRAM mode.

2.10. Applications

The field of applications covers analog and digital TV sets, set-top satellite decoders, video recorders and home computers. For example, Fig. 2–4 shows how the TPU 3040 fits into an analog environment. Two analog sources are connected and the output is analog RGB, synchronized with an external sync signal or self-timed. Page selection and other user actions are sent to the TPU 3040 via I²C-Bus using a high level command language.

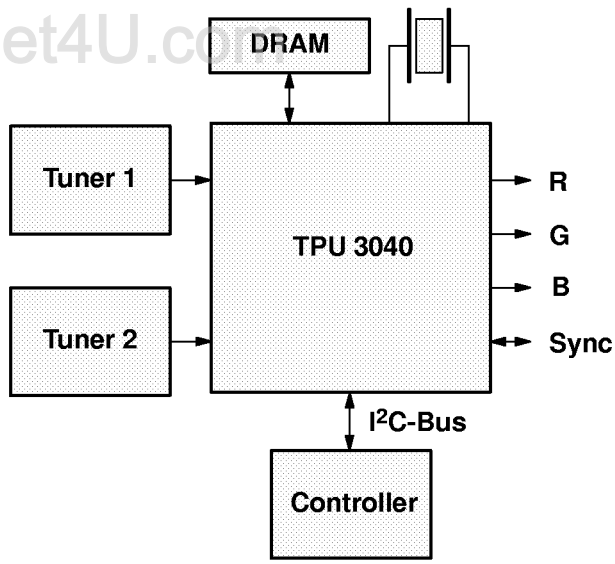


Fig. 2–4: Stand-Alone Application

3. Specifications

3.1. Outline Dimensions

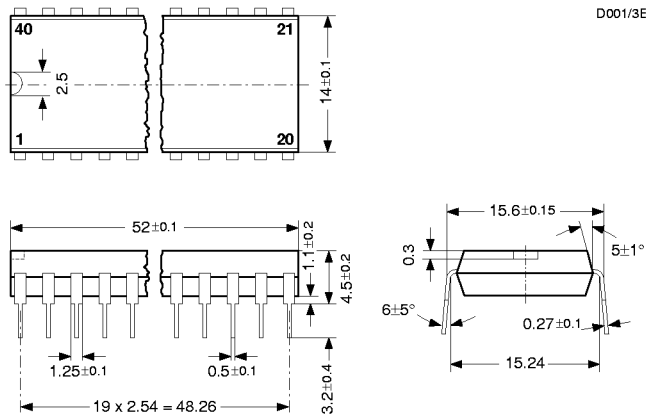


Fig. 3–1:
40-pin Plastic Dual-Inline Package
(PDIP40)
Weight approx. 6 g
Dimensions in mm

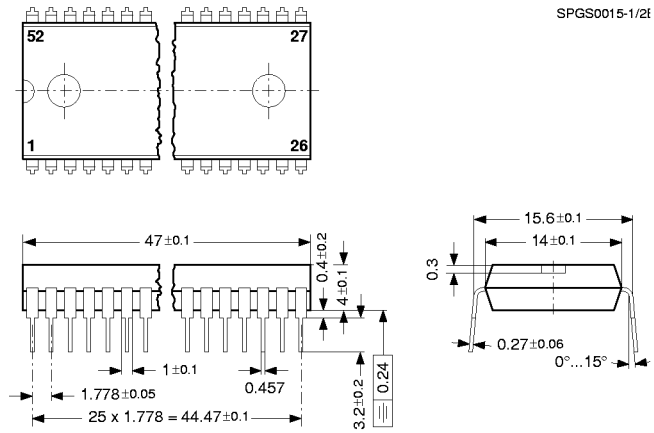


Fig. 3–2:
52-Pin Plastic Shrink Dual-Inline Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

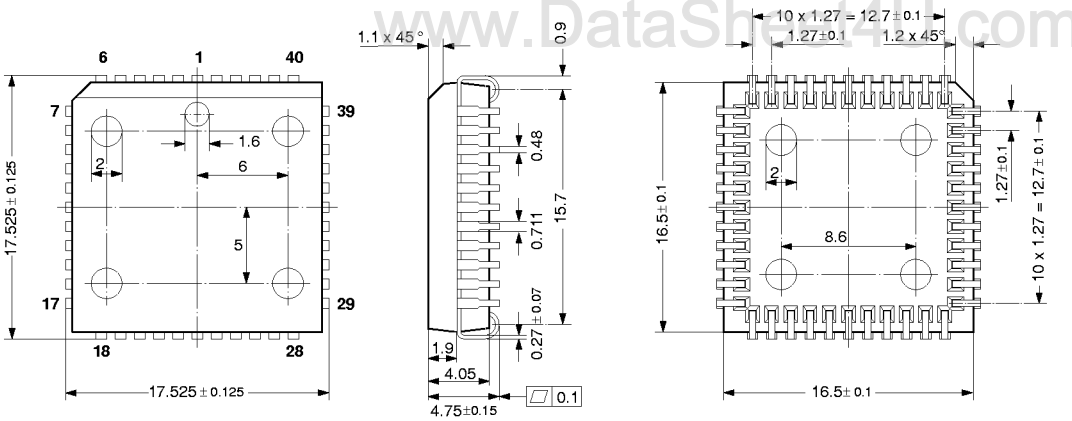


Fig. 3–3:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

Pin No. PLCC44	Pin No. PDIP40	Pin No. PSDIP52	Signal Name	Type	Symbol
TPU 3040	TPU 3035 TPU 3040	TPU 3040 TPU 3050			
1	1	3	Reference Voltage Top	Supply	VRT
–	–	2	SRAM Data 0	Input/Output	D0
–	–	1	SRAM Data 1	Input/Output	D1
–	–	52	SRAM Data 2	Input/Output	D2
2	40	51	Test Mode	Input	TEST
3	39	50	DRAM Data / SRAM Data 3	Input/Output	DATA / D3
4	38	49	DRAM/SRAM Write Enable	Output	$\overline{WE}$
5	37	48	DRAM Row Address Strobe / SRAM Data 4	Output	$\overline{RAS}$ / D4
6	36	47	DRAM Column Address Strobe / SRAM Data 5	Output	$\overline{CAS}$ / D5
–	–	46	SRAM Data 6	Input/Output	D6
–	–	45	SRAM Data 7	Input/Output	D7
7	35	44	DRAM/SRAM Address 0	Output	A0
8	34	43	DRAM/SRAM Address 1	Output	A1
9	33	42	DRAM/SRAM Address 2	Output	A2
10	32	41	DRAM/SRAM Address 3	Output	A3
11	31	40	DRAM/SRAM Address 4	Output	A4
12	30	39	DRAM/SRAM Address 5	Output	A5
13	29	38	DRAM/SRAM Address 6	Output	A6
14	28	37	DRAM/SRAM Address 7	Output	A7
15	27	36	DRAM/SRAM Address 8	Output	A8
16	26	35	DRAM/SRAM Address 9	Output	A9
17	25	34	DRAM/SRAM Address 10	Output	A10
–	–	33	Pad Supply Voltage	Supply	PVSUP
–	–	32	Pad Ground	Supply	PGND
18	24	31	DRAM/SRAM Address 11	Output	A11
–	–	30	SRAM Address 12	Output	A12
–	–	29	SRAM Address 13	Output	A13
–	–	28	SRAM Address 14	Output	A14
–	–	27	SRAM Address 15	Output	A15
19	23	26	IIC Bus Clock	Input/Output	SCL
20	22	25	IIC Bus Data	Input/Output	SDA
–	–	–	SRAM Address 16	Output	A16
–	–	–	SRAM Address 17	Output	A17
–	–	–	SRAM Address 18	Output	A18
–	–	–	SRAM Address 19	Output	A19

Pin Connections and Short Descriptions, continued

Pin No. PLCC44	Pin No. PDIP40	Pin No. PSDIP52	Signal Name	Type	Symbol
TPU 3040	TPU 3035 TPU 3040	TPU 3040 TPU 3050			
–	–	–	SRAM Address 20	Output	A20
21	21	–	Infrared	Input	IR
22	–	–	MAC Paket Data	Input	MAC_PAK
23	–	–	MAC VBI Data	Input	MAC_VBI
24	–	–	MAC Sync	Input	MAC_SYNC
25	20	23	Horizontal Sync Composite Sync 1 Main Sync	Input/Output Output Input	HSYNC CSYNC1 MSYNC
26	19	22	Vertical Sync Composite Sync 2	Input/Output Output	VSYNC CSYNC2
27	18	21	Crystal Oscillator Output	Output	XTAL2
28	17	20	Crystal Oscillator Input Main Clock	Input Input	XTAL1 CLK20
29	16	19	Reset	Input/Output	$\overline{\text{RESET}}$
30	15	18	Fast Blank Input Shadow Priority Bus 0	Input Output Input/Output	FBIN SHADOW PRIO0
31	14	17	Analog Blue Input Priority Bus 1	Input Input/Output	BIN PRIO1
32	13	16	Analog Green Input Priority Bus 2	Input Input/Output	GIN PRIO2
33	12	15	Analog Red Input Color Address Bus 4	Input Output	RIN COLOR4
34	11	14	Digital Supply Voltage	Supply	DVSUP
35	10	13	Digital Ground	Supply	DGND
36	9	12	Fast Blank Output Color Address Bus 3	Output Output	FBOUT COLOR3
37	8	11	Analog Blue Output Color Address Bus 2	Output Output	BOUT COLOR2
38	7	10	Analog Green Output Color Address Bus 1	Output Output	GOUT COLOR1
39	6	9	Analog Red Output Color Address Bus 0	Output Output	ROUT COLOR0
40	5	8	Analog Ground	Supply	AGND
41	4	7	Analog Supply Voltage	Supply	AVSUP
42	3	6	Analog Composite Video 1	Input	VIN1
43	2	5	Analog Signal Ground	Supply	SGND
44	–	4	Analog Composite Video 2	Input	VIN2

3.3. Pin Descriptions

Pin 1 – **VRT** Reference Voltage Top (Fig. 3–7)
This pin is connected to the internally-stabilized reference voltage of the A/D converter which is derived from the V_{ASUP} supply. Pin 1 must be decoupled externally to prevent high and low frequency noise.

Pin 2 – **TEST** Test Input (Fig. 3–8)
This pin is used for switching the TPU 3040 into test mode. For normal operation this pin has to be connected to ground.

Pin 3 – **DATA** DRAM Data Input/Output (Fig. 3–9)
This pin serves as an output for writing data into the external DRAM and as an input for reading data from the external DRAM.

Pin 4 – $\overline{\textbf{WE}}$ DRAM Write Enable Output (Fig. 3–9)
This pin supplies the Write Enable signal to the external DRAM.

Pin 5 – $\overline{\textbf{RAS}}$ DRAM Row Address Strobe Output (Fig. 3–9)
This pin supplies the Row Address Strobe signal to the external DRAM.

Pin 6 – $\overline{\textbf{CAS}}$ DRAM Column Address Strobe Output (Fig. 3–9)
This pin supplies the Column Address Strobe signal to the external DRAM.

Pins 7 to 18 – **A0** to **A11** DRAM Address Outputs (Figs. 3–9 and 3–10)
These pins are used for addressing the external DRAM. The addressing is compatible to all DRAM sizes from 64K to 16M, therefore the correct connection of pins A8 to A11 to the corresponding DRAM pins is necessary.

Pins 19 and 20 – **SCL and SDA** IIC Bus (Fig. 3–11)
Via these pins, the TPU 3040 communicates with external devices.

Pin 21 – **IR** Infrared (Fig. 3–12)
This pin has to be connected to ground.

Pin 22 – **MAC_PAK** MAC Paket Data (Fig. 3–12)
Via this pin, the TPU 3040 receives MAC packets from the DMA 2381 or from the DMA 2386.

Pin 23 – **MAC_VBI** MAC VBI Data (Fig. 3–12)
By means of this input, the TPU 3040 receives MAC VBI data from the DMA 2381 or from the DMA 2386.

Pin 24 – **MAC_SYNC** MAC Synchronization (Fig. 3–12)
By means of this input, the TPU 3040 receives the required MAC synchronization pulse from the DMA 2381. This sync pulse is used both as line sync and frame sync for the MAC teletext acquisition.

Pin 25 – **HSYNC** Horizontal Synchronization (Fig. 3–9)
Via this input, the TPU 3040 receives the horizontal synchronization signal. Either the falling or the rising edge of this signal will start the internal horizontal timing generation.

Pin 26 – **VSYNC** Vertical Synchronization (Fig. 3–9)
Via this input, the TPU 3040 receives the vertical synchronization signal. Either the falling or the rising edge of this signal will start the internal vertical timing generation.

Pin 27 and 28 – **XTAL1** and **XTAL2** (Fig. 3–13)
These oscillator pins are used to connect a 20.25MHz crystal, which determines the internal clock signal. Alternatively, an 20.25MHz clock signal may be fed to pin 28.

Pin 29 – $\overline{\textbf{RESET}}$ Reset Input/Output (Fig. 3–11)
This pin is used for hardware reset. The TPU 3040 watchdog generates a reset pulse which can be used to reset external circuits.

Pin 30 – **FBIN** Fast Blanking Input (Fig. 3–14)
This pin serves for enabling the analog RGB inputs.

Pin 31 to 33 – **RIN, GIN, BIN** RGB Inputs (Fig. 3–15)
Via these inputs, the TPU 3040 receives analog RBG signals, e.g. OSD or video recorder (SCART), which are fed to the analog RBG outputs. The specified level of these signals is 0 V to 0.7 V. For other DC levels, an AC coupling has to be used and the internal clamping circuit will adjust the DC level.

Pin 34 – **DVSUP** Digital Supply Voltage
This pin supplies all digital stages and has to be connected with the positive supply voltage.

Pin 35 – **DGND** Digital Ground
This pin is the common ground connection of all digital stages and has to be connected with the ground of the power supply.

Pin 36 – **FBOUT** Fast Blanking Output (Fig. 3–10)
This output supplies a fast switching signal, indicating the presence of RBG output signals.

Pin 37 to 39 – **ROUT, GOUT, BOUT** RGB Outputs (Fig. 3–15)
These outputs either supply the analog RGB signals, which have been received via the analog RGB input pins 31 to 33, or the internally generated RGB signals.

Pin 40 – **AGND** Analog Ground
This pin is the common ground connection of all analog stages and has to be connected with the ground of the power supply.

Pin 41 – **AVSUP** Analog Supply Voltage
This pin supplies all analog stages and has to be connected with the positive supply voltage.

Pin 42 and 44 – **VIN1** and **VIN2** Analog Video Inputs (Fig. 3–16)
The analog input signals carrying text data are fed to the TPU 3040 via a clamping capacitor of 33 nF to these pins.

Pin 43 – **SGND** Signal Ground
The lower end of the internal reference chain of the A/D converter is internally connected to the pin 43.

3.3.1. Pin Descriptions TPU 3050 (pin numbers refer to 52-pin PSDIP package)

Pin 33 – **PVSUP** Pad Supply Voltage
This pin supplies all SRAM interface pads and has to be connected with the positive supply voltage.

Pin 32 – **PGND** Pad Ground
This pin is the common ground connection of all SRAM interface pads and has to be connected with the ground of the power supply.

Pin 1, 2, 45 to 48, 50, 52 – **D0 to D7** SRAM Data Input/ Output (Fig. 3–9)
These pins serve as output for writing data into the external SRAM and as input for reading data from the external SRAM.

Pins 7 to 18 – **A0** to **A16** SRAM Address Outputs (Figs. 3–9 and 3–10)
These pins are used for addressing the external SRAM. The addressing is compatible to all SRAM sizes from 64K to 1M. Therefore, the correct connection of pins A11 to A16 to the corresponding SRAM pins is necessary.

3.4. Pin Configuration

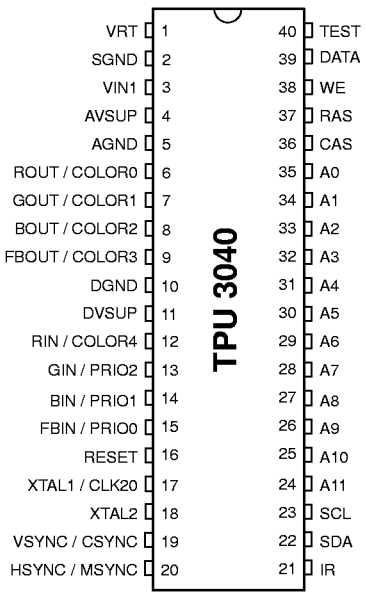


Fig. 3–4: TPU 3040 in 40-pin PDIP package

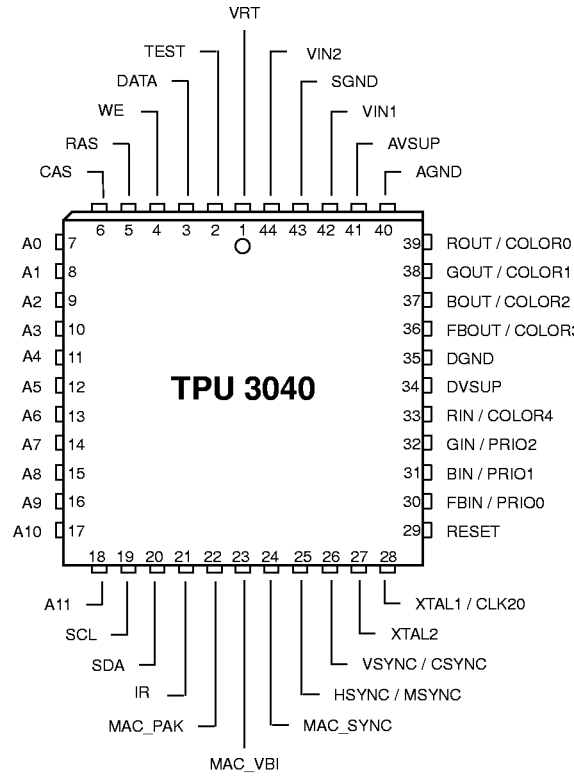


Fig. 3–6: TPU 3040 in 44-pin PLCC package

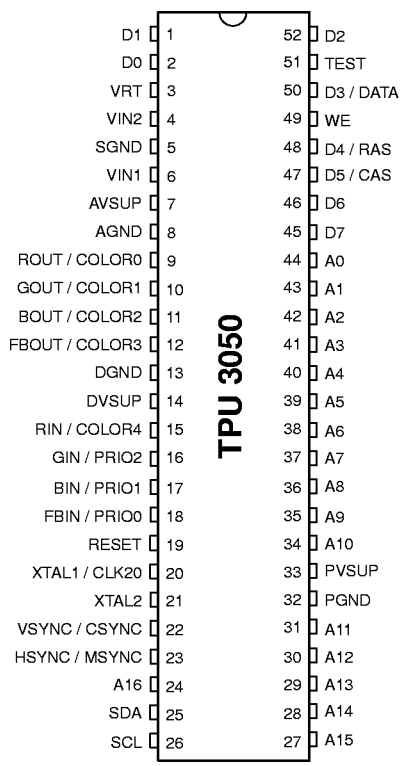


Fig. 3–5: TPU 3050 in 52-pin PSDIP package

3.5. Pin Circuits

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter “P” means P-channel, the letter “N” N-channel.

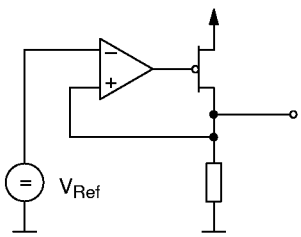


Fig. 3–7:
Supply Pin 1

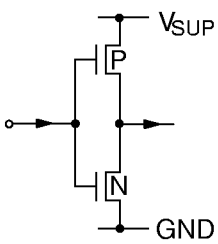


Fig. 3–8:
Input Pins 2 and 21

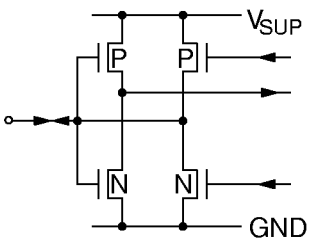


Fig. 3–9:
Input/Output Pins 3 to 14, 18, 25, 26

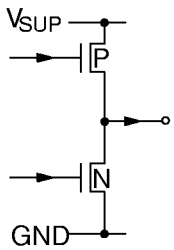


Fig. 3–10:
Output Pins 15 to 17 and 36

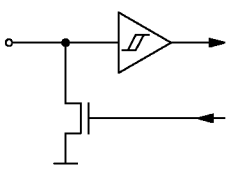


Fig. 3–11:
Input/Output Pins 19, 20 and 29

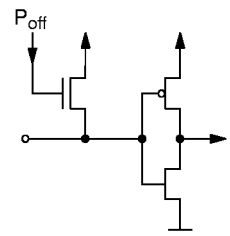


Fig. 3–12:
Input Pins 22 to 24

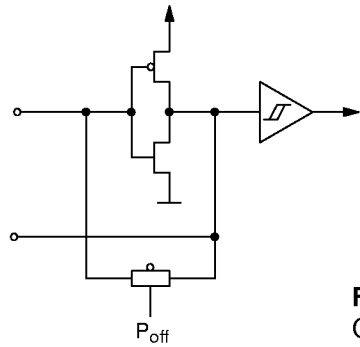


Fig. 3–13:
Output/Input Pins 27, 28

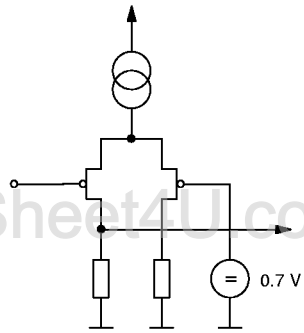


Fig. 3–14: Input Pin 30

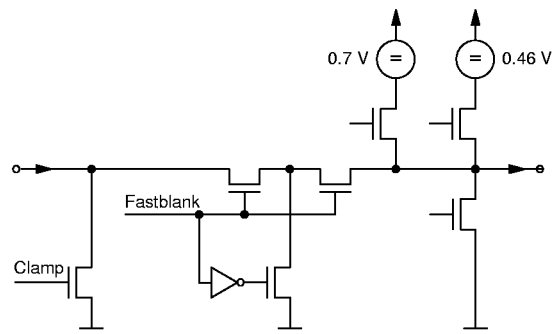


Fig. 3–15: Input/Output Pins 31 to 33 and 37 to 39

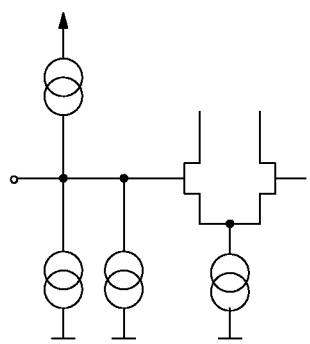


Fig. 3–16:
Input Pins 42 and 44

3.6. Electrical Characteristics

All voltages refer to ground.

3.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	−40	125	°C
V_{DSUP}	Digital Supply Voltage	34	−0.3	6	V
V_{ASUP}	Analog Supply Voltage	41	−0.3	6	V
V_{DI}	Digital Input Voltage		−0.3	V_{DSUP} +0.3	V
V_{AI}	Analog Input Voltage		−0.3	V_{ASUP} +0.3	V
I_O	Output Current		−10	10	mA

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Crystal Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Ambient Operating Temperature	27, 28	0	–	65	°C	
f_0	Parallel Resonance Frequency		–	20.25	–	MHz	C_L = 30 pF, T_A = 25 °C
$\frac{\Delta f}{f_0}$	Frequency Tolerance		–	–	± 50	ppm	T_A = 25 °C
$\frac{\Delta f}{f}$	Frequency Deviation versus Temperature		–	–	± 50	ppm	over operating temperature range with respect to frequency at 25 °C
R_r	Series Resistance		–	–	30	Ω	
C_0	Static Capacitance		–	–	8	pF	
C_1	Dynamic Capacitance		10	–	30	fF	
P_D	Rated Drive Level		–	0.2	–	mW	
$\frac{f_0}{f_H}$	Spurious Frequency Attenuation		3	–	–	dB	

3.6.3. General Operating Conditions

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Ambient Operating Temperature	all	0	20	65	°C	
V_{DSUP}	Digital Supply Voltage	34	4.75	5.0	5.25	V	
V_{ASUP}	Analog Supply Voltage	41	4.75	5.0	5.25	V	
f_{CLK}	Clock Frequency	27, 28	20.20	20.25	20.30	MHz	correct slicer operation

3.6.4. General Input Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_I	Input Leakage Current	all inputs			±1	µA	$V_{GND} \leq V_I \leq V_{SUP}$
C_I	Input Capacitance				20	pF	

3.6.5. Power Consumption

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{DSUP}	Digital Supply Current	34	–	40	60	mA	
I_{ASUP}	Analog Supply Current	41	–	20	30	mA	
P_T	Total Power Consumption	34,41	–	300	500	mW	

3.6.6. Timer, Interrupt, and Watchdog Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Reset Input Low Voltage	29	–	–	1.5	V	
V_{IH}	Reset Input High Voltage		3.0	–	–	V	
V_{OL}	Reset Output Low Voltage		–	–	0.4	V	I_L = 3mA
t_{OL}	Reset Output Pulse Width		–	1.618	–	ms	$2^{15} / f_{CLK}$
V_{IL}	Test Input Low Voltage	2	–	–	0.8	V	
V_{IH}	Test Input High Voltage		2.0	–	–	V	
V_{IL}	Infrared Input Low Voltage	21	–	–	0.8	V	
V_{IH}	Infrared Input High Voltage		2.0	–	–	V	

3.6.7. Clock Generator Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{CLK}	Clock Input Amplitude	28	1.0	–	3.0	V_{PP}	C_C = 10 nF
f_{CLK}	Clock Input Frequency		20.20	20.25	20.30	MHz	
f_{CLK}	Generated Clock Frequency	27,28	20.20	20.25	20.30	MHz	recommended crystal

3.6.8. Video Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{VRT}	Voltage Reference Top	1	2.6	2.8	3.0	V	C_L = 100 nF || 10 µF
V_{VRTN}	Voltage Reference Top Noise		–	–	100	mV_{PP}	C_L = 100 nF || 10 µF
V_I	Video Input Voltage	42, 44	0.7	1	1.3	V_{PP}	R_D= 75 Ω
I_{CLP}	Positive Clamping Current		–	235	–	µA	V_{IN} = 0V
I_{CLN}	Negative Clamping Current		–	6	–	µA	V_{IN} = V_{ASUP}
I_{CR}	Clamping Current Ratio		35	40	45		
C_C	Recommended Coupling Capacitance		–	33	–	nF	
R_D	Recommended Drive Impedance		–	75	100	Ω	

3.6.9. MAC Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	22, 23, 24	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	

3.6.10. RGB Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_I	RGB Input Voltage	31, 32, 33	0	0 to 0.7	1.5	V	R_L = 75 Ω
C_C	External Coupling Capacitance		100	-	1000	nF	R_L > 100k Ω
R_{CL}	RGB Input Resistance during Clamping		–	–	100	Ω	clamp window = 64 µs
V_{IL}	Fast Blank Input Low Voltage	30	–	–	0.5	V	R_L = 75 Ω
V_{IH}	Fast Blank Input High Voltage		0.9	–	–	V	R_L = 75 Ω
V_{OL}	RGB Output Low Voltage	37, 38, 39	0	–	50	mV	V_{ASUP} = 5.0 V, I_L = 0.5 mA
V_{OH100}	RGB Output High Voltage		630	700	770	mV	V_{ASUP} = 5.0 V, I_L = −0.5 mA
V_{OH66}	RGB Output High Voltage		420	467	513	mV	V_{ASUP} = 5.0 V, I_L = −0.5 mA
ΔV_O	Differential RGB Output Voltage		–	–	50	mV	V_{ASUP} = 5.0 V, ΔI_L < 10 µA
t_T	RGB Output Transition Time		–	–	10	ns	V_{ASUP} = 5.0 V, C_L = 20 pF
V_{OHO}	RGB Output Positive Overshoot				10	%	V_{ASUP} = 5.0 V, C_L = 20 pF
V_{OLO}	RGB Output Negative Over-shoot				10	%	V_{ASUP} = 5.0 V, C_L = 20 pF
R_{on}	Resistance from RGB Inputs to RGB Outputs	31, 32, 33, 37, 38, 39	–	–	150	Ω	ext. RGB on
V_{OL}	Fast Blank Output Low Voltage	36	–	–	0.4	V	I_L = 1.6 mA
V_{OH}	Fast Blank Output High Voltage		3.0	–	–	V	I_L = −0.5 mA
t_T	Fast Blank Output Transition Time		–	–	10	ns	C_L = 20 pF $V_{OL(max)} \leftrightarrow V_{OH(min)}$
t_D	Differential RGB & FB Timing	36 37,38,39			10	ns	C_L = 20 pF

3.6.11. Prio and Color Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Prio Input Low Voltage	30 to 32	–	–	0.8	V	
V_{IH}	Prio Input High Voltage		1.5	–	–	V	
V_{OL}	Prio & Color Output Low Voltage	30 to 33 36 to 39	–	0.25	0.5	V	I_L = 8mA, strength 3 I_L = 6mA, strength 2 I_L = 4mA, strength 1 I_L = 2mA, strength 0
V_{OH}	Prio & Color Output High Voltage		1.8	2.0	–	V	I_L = −0.01 mA
I_O	Prio & Color Output Pull-up Current		1.3	1.5	–	mA	V_{OL} = 0 V
t_T	Prio & Color Output Transition Time		–	–	10	ns	C_L = 20 pF
t_D	Differential Prio & Color Timing				10	ns	C_L = 20 pF

3.6.12. H and V Sync Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{ITF}	Input Trigger Level High → Low	25, 26	1.5	–	2.0	V	
V_{ITR}	Input Trigger Level Low → High		2.5	–	3.0	V	
V_{ITH}	Input Trigger Hysteresis		0.5	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4	V	I_L = 1.6 mA
V_{OH}	Output High Voltage		2.4	–	–	V	I_L = – 0.1 mA
t_T	Output Transition Time		–	–	10	ns	C_L = 20 pF

3.6.13. MSync Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	25	–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		10	–	–	ns	C_L = 20 pF
t_{IH}	Input Hold Time		0	–	–	ns	C_L = 20 pF

3.6.14. I²C-Bus Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{ITF}	Input Trigger Level High → Low	19, 20	1.5	–	2.0	V	
V_{ITR}	Input Trigger Level Low → High		2.5	–	3.0	V	
V_{ITH}	Input Trigger Hysteresis		0.5	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4	V	I_L = 3 mA
t_R	Input Rise Time		–	–	1000	ns	
t_F	Output Fall Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	19	0	–	400	kHz	

3.6.15. DRAM Interface Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	3	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
V_{OL}	Output Low Voltage	3 to 18	–	–	0.4	V	I_L = 1.6 mA
V_{OH}	Output High Voltage		2.4	–	–	V	I_L = −0.5 mA
t_T	Output Transition Time		–	5	10	ns	C_L = 15 pF $V_{OL(max)} \leftrightarrow V_{OH(min)}$

3.6.15.1. DRAM Fast Mode Timing at f_{CLK} = 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
t_{PC}	Page Mode Cycle Time	6		98.8		ns	DRAM: t_{PC} > 55
t_{CAS}	$\overline{CAS}$ Pulse Width		60			ns	DRAM: t_{CAS} > 25
t_{CP}	$\overline{CAS}$ Precharge Time		10			ns	DRAM: t_{CP} > 10
t_{RP}	$\overline{RAS}$ Precharge Time	5	90			ns	DRAM: t_{RP} > 80
t_{RSH}	$\overline{RAS}$ Hold Time	5, 6	40			ns	DRAM: t_{RSH} > 25
t_{CSH}	$\overline{CAS}$ Hold Time		110			ns	DRAM: t_{CSH} > 100
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time		45			ns	DRAM: t_{RCD} > 25
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		55			ns	DRAM: t_{CRP} > 10
t_{ASR}	Row Address Setup Time	5, 7 to 18	55			ns	DRAM: t_{ASR} > 0
t_{RAH}	Row Address Hold Time		15			ns	DRAM: t_{RAH} > 15
t_{AR}	Column Address Hold Time		105			ns	DRAM: t_{AR} > 75
t_{RAL}	Column Address Lead Time		55			ns	DRAM: t_{RAL} > 50
t_{ASC}	Column Address Setup Time	6, 7 to 18	5			ns	DRAM: t_{ASC} > 0
t_{CAH}	Column Address Hold Time		60			ns	DRAM: t_{CAH} > 20
t_{RRH}	Read Command Hold Time	4, 5	80			ns	DRAM: t_{RRH} > 0
t_{RCH}	Read Command Hold Time	4, 6	50			ns	DRAM: t_{RCH} > 0
t_{WCH}	Write Command Hold Time		90			ns	DRAM: t_{WCH} > 20
t_{WCS}	Write Command Setup Time		30			ns	DRAM: t_{WCS} > 0
t_{DOHR}	DATA Output Hold Time RAS	3, 5	105			ns	DRAM: t_{DHR} > 75
t_{DOS}	DATA Output Setup Time	3, 6	0			ns	DRAM: t_{DS} > 0
t_{DOH}	DATA Output Hold Time		60			ns	DRAM: t_{DH} > 20
t_{DIS}	DATA Input Setup Time		20			ns	DRAM: t_{CAC} < 25
t_{DIH}	DATA Input Hold Time		0			ns	DRAM: t_{OFF} < 30

3.6.15.2. DRAM Slow Mode Timing at f_{CLK} = 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
t_{PC}	Page Mode Cycle Time	6		148		ns	DRAM: t_{PC} > 120
t_{CAS}	$\overline{CAS}$ Pulse Width		60			ns	DRAM: t_{CAS} > 60
t_{CP}	$\overline{CAS}$ Precharge Time		60			ns	DRAM: t_{CP} > 25
t_{RP}	$\overline{RAS}$ Precharge Time	5	90			ns	DRAM: t_{RP} > 90
t_{RSH}	$\overline{RAS}$ Hold Time	5, 6	60			ns	DRAM: t_{RSH} > 60
t_{CSH}	$\overline{CAS}$ Hold Time		140			ns	DRAM: t_{CSH} > 120
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time		65			ns	DRAM: t_{RCD} > 25
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		85			ns	DRAM: t_{CRP} > 10
t_{ASR}	Row Address Setup Time	5, 7 to 18	55			ns	DRAM: t_{ASR} > 0
t_{RAH}	Row Address Hold Time		15			ns	DRAM: t_{RAH} > 15
t_{AR}	Column Address Hold Time		155			ns	DRAM: t_{AR} > 80
t_{RAL}	Column Address Lead Time		105			ns	DRAM: t_{RAL} > 80
t_{ASC}	Column Address Setup Time	6, 7 to 18	35			ns	DRAM: t_{ASC} > 0
t_{CAH}	Column Address Hold Time		60			ns	DRAM: t_{CAH} > 20
t_{RRH}	Read Command Hold Time	4, 5	80			ns	DRAM: t_{RRH} > 20
t_{RCH}	Read Command Hold Time	4, 6	50			ns	DRAM: t_{RCH} > 0
t_{WCH}	Write Command Hold Time		90			ns	DRAM: t_{WCH} > 30
t_{WCS}	Write Command Setup Time		50			ns	DRAM: t_{WCS} > 0
t_{DOHR}	DATA Output Hold Time RAS	3, 5	155			ns	DRAM: t_{DHR} > 90
t_{DOS}	DATA Output Setup Time	3, 6	30			ns	DRAM: t_{DS} > 0
t_{DOH}	DATA Output Hold Time		60			ns	DRAM: t_{DH} > 30
t_{DIS}	DATA Input Setup Time		20			ns	DRAM: t_{CAC} < 60
t_{DIH}	DATA Input Hold Time		0			ns	DRAM: t_{OFF} < 35

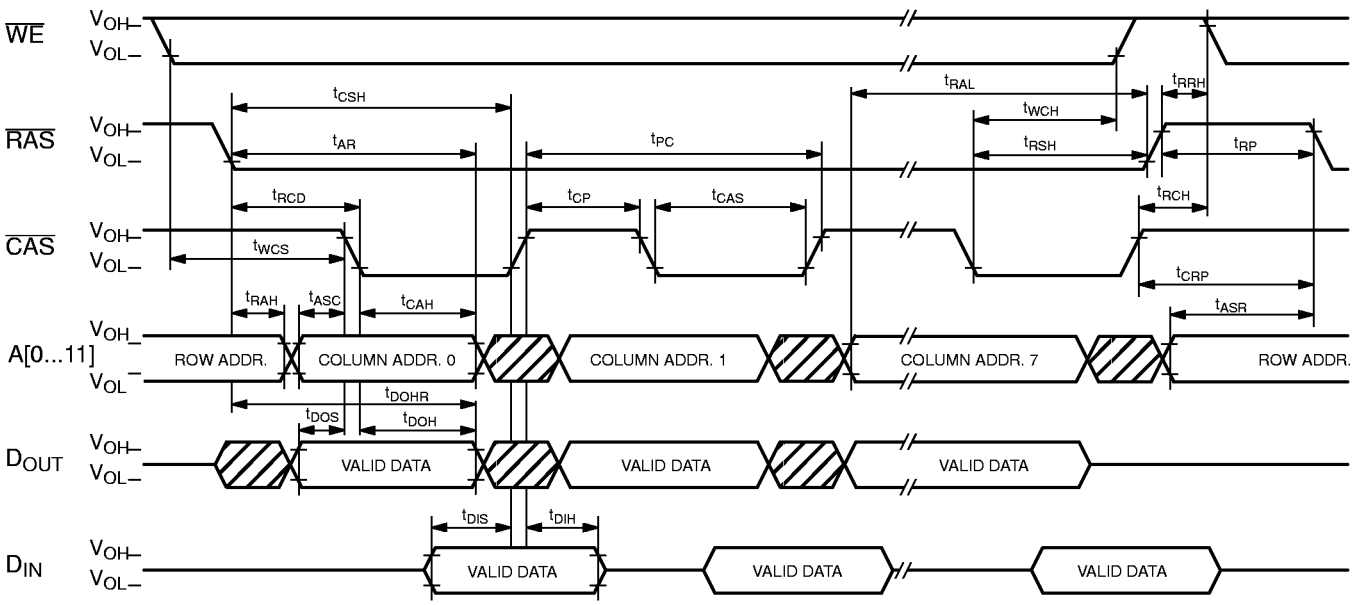


Fig. 3–17: DRAM page mode waveforms

3.6.16. SRAM Interface Characteristics (TPU 3050 only)

Symbol	Parameter	Pin No. PSDIP 52	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	1,2 45 to 48 50,52	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
V_{OL}	Output Low Voltage	1,2,24 27 to 31 34 to 50 52	–	–	0.4	V	I_L = 1.6 mA
V_{OH}	Output High Voltage		2.4	–	–	V	I_L = −0.5 mA
t_T	Output Transition Time		–	5	10	ns	C_L = 15 pF $V_{OL(max)} \leftrightarrow V_{OH(min)}$

3.6.16.1. SRAM Mode Timing at f_{CLK} = 20.25 MHz

Symbol	Parameter	Pin No. PSDIP 52	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC} t_{WC}	Read / Write Cycle Time	24 27 to 31 34 to 44		889		ns	SRAM: t_{RC} > 100 SRAM: t_{WC} > 100
t_{AS}	Address Setup Time	24 27 to 31 34 to 44 49	444			ns	SRAM: t_{AS} > 0
t_{AW}	Address Valid to End of Write		543			ns	SRAM: t_{AW} > 90
t_{WR}	Write Recovery Time		593			ns	SRAM: t_{WR} > 5
t_{WP}	Write Pulse Width Time	49	98.8			ns	SRAM: t_{WP} > 70
t_{WHZ}	Write to Output High–Z	1,2 45 to 50 52	0			ns	SRAM: t_{OW} > 10
t_{OW}	Write to Output Active		25			ns	SRAM: t_{WHZ} < 50
t_{DOS}	Data Output Setup Time		98.8			ns	SRAM: t_{DW} > 40
t_{DOH}	Data Output Hold Time		0			ns	SRAM: t_{DH} > 0
t_{DIS}	Data Input Setup Time	1,2,24 27 to 31 34 to 48 50,52	20			ns	SRAM: t_{AA} < 100
t_{DIH}	Data Input Hold Time		0			ns	SRAM: t_{OH} > 10
t_{DIL}	Data Input Latch Time			198		ns	

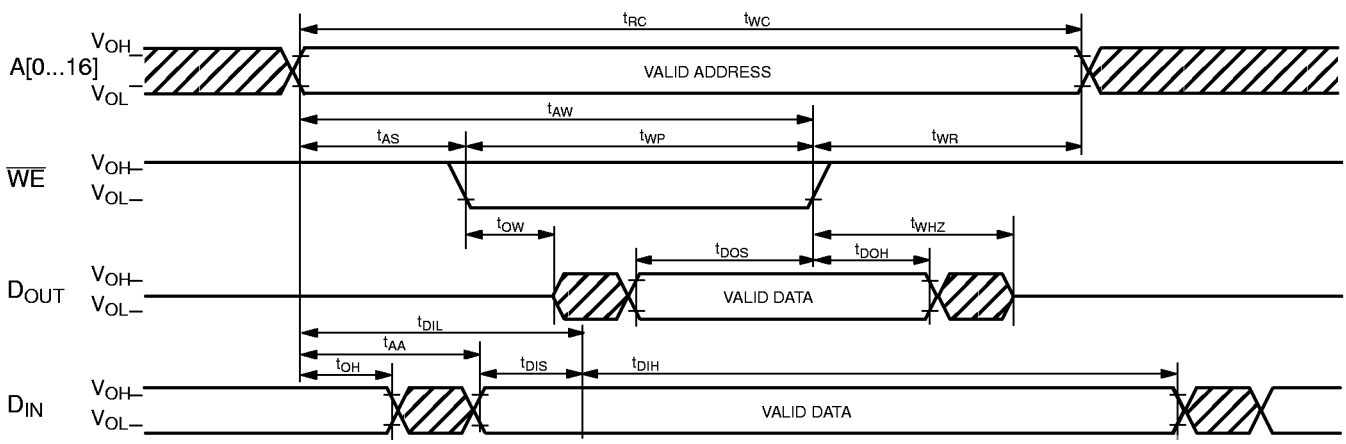


Fig. 3–18: SRAM mode waveforms

4. Definitions

4.1. CPU

4.1.1. Memory Mapping

Table 4–1: 65C02 memory map

Interrupt Vector	**Absolute Address (high byte, low byte)**
IRQ	FFFF, FFFE
Reset	FFFD, FFFC
NMI	FFFB, FFFA
Control Word	FFF9
Memory Segment	**Absolute Address**
Program RAM	0000 – 01FF
Zero Page	0000 – 00FF
Stack Page	0100 – 01FF
OSD Buffer	0100 – 019F
I/O Page	0200 – 02FF
Character ROM	6000 – 7FFF
Program ROM	E000 – FFFF

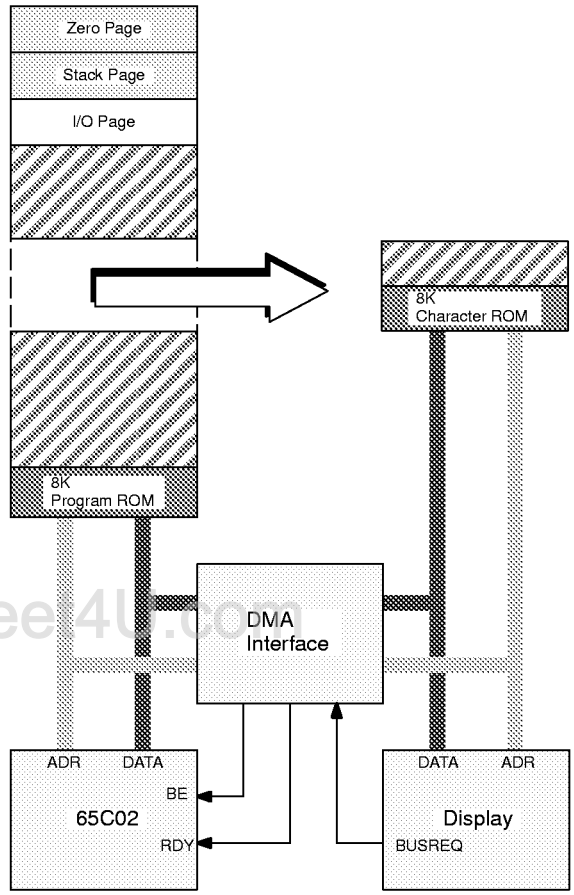


Fig. 4–1: 65C02 memory environment

4.2. I²C Bus Interface

Communication between TPU 3040 and host controller is done via I²C-bus. For detailed information on the I²C-bus please refer to the Philips manual 'I²C-bus Specification'.

The TPU 3040 acts as a slave transmitter/receiver and uses clock synchronization to slow down the data transfer if necessary. General call address will not be acknowledged.

Different memories and functions of TPU 3040 can be accessed by subaddressing. The byte following the slave address byte is defined as the subaddress byte.

Maximum length of an I²C telegram is 256 bytes following slave address and subaddress byte. The interface supports data transfer with autoincrement.

The I²C-bus interface is interrupt-driven and uses an internal 48-byte buffer to collect I²C data in real-time without disturbing internal processes. This is done to avoid clock synchronization as far as possible. When the TPU 3040 has to process the I²C buffer and the I²C telegram has not yet been stopped, the I²C clock line will be held down.

The time required to process the I²C buffer depends on other processes running inside the TPU 3040 firmware. Thus the following I²C telegram addressing the TPU can be held after the slave address byte until the old telegram is completely processed.

4.2.1. Subaddressing

Access to all memory locations and to the command interface is achieved by subaddressing. Both the external DRAM and the internal CPU memory can be addressed completely. The TPU 3040 acknowledges 6 different subaddresses following the slave address (see Table 4–2).

The following symbols are used to describe the I²C example telegrams:

```
<       start condition
>       stop condition
ab      address bank byte
ah      address high byte
al      address low byte
cc      command byte
dd      data byte
ss      status byte
..      0 - n continuation bytes
```


Table 4–2: I²C-bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
TPU	0010 001x	22, 23	W, R	TPU slave address
Sub 1	0111 1000	78	W	subaddressing CPU (static)
Sub 2	0111 1001	79	W	subaddressing CPU (autoincrement)
Sub 3	0111 1010	7A	W	subaddressing DRAM (autoincrement)
Sub 4	0111 1011	7B	W	subaddressing command language
Data	0111 1100	7C	R/W	subaddressing data register
Status	0111 1101	7D	R	status register bit 7 = command wait bit 6 = command invalid bit 5 = command found no data bit 4 = not used bit 3 = not used bit 2 = not used bit 1 = 0 bit 0 = 0

4.2.1.1. CPU Subaddressing

There are 2 CPU subaddresses to access CPU memory: either with static memory address or with autoincrementing memory address. The main purpose of CPU subaddressing is to write text into the OSD buffer and to access the I/O page (see chapter 4.15.). The static CPU subaddress can be used to write more than 1 byte into the same I/O page register.

The CPU subaddress has to be followed by 2 address bytes defining the CPU memory address. The following data byte is written into this address. In the case of autoincrement the continuation bytes are written into incrementing memory addresses.

The CPU telegram can be stopped after the 2 memory address bytes. The following I²C telegram subaddressing the data register will continue data transfer to or from the CPU memory. The data transfer will always start at the CPU memory address (autoincrement is not saved).

```
< 22 78 ah al dd .. >
< 22 79 ah al dd .. >
< 22 79 ah al  > <  22 7C dd .. >
```

Data is directly written into CPU memory without using the I²C buffer of TPU 3040 and without waiting for a stop condition.

4.2.1.2. DRAM Subaddressing

DRAM access is necessary to generate level 2 displays. The external DRAM can be addressed on byte level. The maximum DRAM size of 16 Mbit requires a 21-bit memory address pointer. The format of the DRAM address pointer is shown in Fig. 4–2.

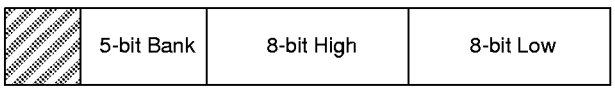


Fig. 4–2: DRAM Address Pointer

The DRAM subaddress has to be followed by 3 address bytes defining the DRAM address pointer. The following data byte is written into this address.

DRAM subaddressing always uses autoincrement. Separate read and write DRAM address pointers are saved for autoincrement.

The DRAM telegram can be stopped after the 3 address pointer bytes. The following I²C telegram subaddressing the data register will continue data transfer to or from the DRAM.

When reading the DRAM, the first data byte the TPU 3040 returns is a dummy byte, which has to be ignored.

```
< 22 7A ab ah al dd .. >
< 22 7A ab ah al  > < 22 7C dd .. >
< 22 7A ab ah al  > < 22 7C <  23 dd ..>
```

Data written to the DRAM subaddress is collected first in the I²C buffer of TPU 3040 and is copied to DRAM when the buffer is full (48 bytes) or after stop condition. During the time the buffer is copied to DRAM the TPU 3040 will hold the I²C clock line down.

Reading data from the DRAM subaddress is also buffered internally. Reading the first byte will only empty the I²C buffer. Every time the buffer is empty, the TPU 3040 will copy 48 bytes from DRAM into the I²C buffer. During this time the TPU 3040 will hold the I²C clock line down.

4.2.1.3. Command Subaddressing

TPU 3040 supports a command language, allowing the host controller to start complex processing inside the TPU 3040 with simple commands (see chapter 4.9.). Commands have to be sent to the command subaddress.

The command subaddress has to be followed by the command code. The following data bytes are taken as command parameters.

The execution time for commands depends on other processes running inside the TPU 3040 firmware, therefore the host controller has to read the status register to get information about the running command before reading command parameter or starting other commands.

The status register returns information about the command interface. The ‘command wait’ bit is set during execution of a command and is reset when a command is executed completely and read parameters are available. If a non-existing command is sent to the TPU 3040, the ‘command invalid’ bit is set. If a command could not be executed successfully, the ‘command found no data’ bit is set. In this case the read parameters of this command are not valid.

Reading status from TPU 3040 is done by subaddressing the status register followed by repeated start condition and slave read address (see Fig. 4–3).

```
< 22 7B cc dd ..  >
< 22 7D <  23 ss .. >
< 22 7C <  23 dd .. >
```

Telegrams subaddressing the command interface are buffered and processed after receiving the stop condition. Therefore the command code and all necessary command parameters have to be included in a single telegram.

4.2.1.4. Data Subaddressing

Writing data to TPU 3040 memory is possible by subaddressing the data register directly. The data is then written into memory addressed by the foregoing telegram.

```
< 22 7C dd .. >
```

Reading data from TPU 3040 is done by subaddressing the data register followed by a repeated start condition and slave read address (see Fig. 4–3). The returned data depend on the subaddress selected in the preceding TPU telegram.

```
< 22 7C <  23 dd .. >
```

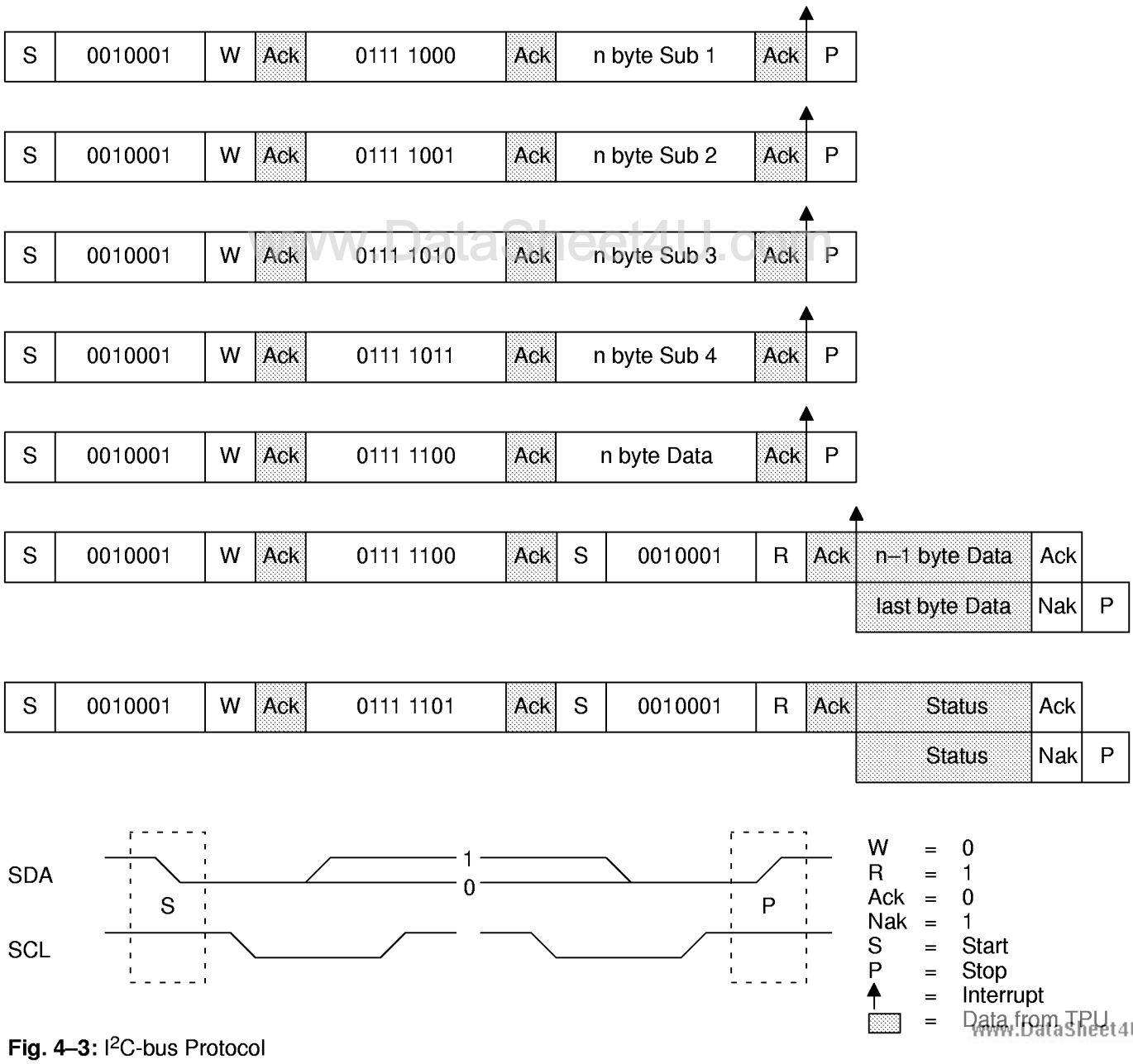


Fig. 4–3: I²C-bus Protocol

4.3. Display Memory

The TPU 3040 supports a variable number of display memories, each 4 KByte large. One bank is used to store the display information of the selected teletext page. The bank location can be defined with the command DISPLAY_TTX_POINTER. Other banks can be used to store any kind of display data in level 1 or level 2 format. Switching between these banks is fast and can be programmed with the command DISPLAY_POINTER. Bank switching allows generation of OSD menus without affecting the teletext display.

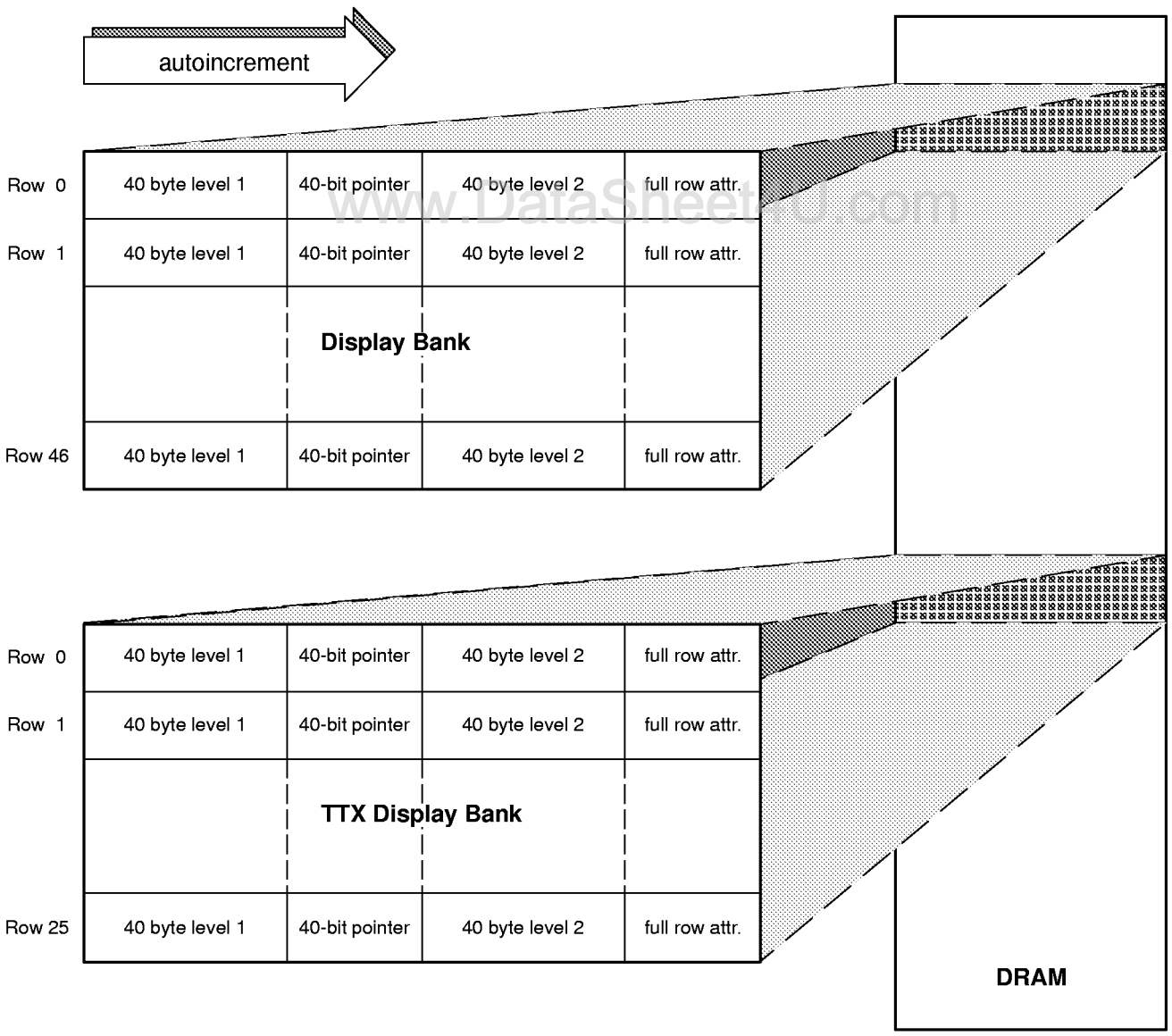


Fig. 4–4: Display Memory Organization

Table 4–3: Full Row Attribute

+ 55H	R/W	Full Row Attribute
Bit	Reset	Function
7	–	1 = row is displayed blank 0 = row is displayed using row data
6	–	1 = row is displayed in double height 0 = row is displayed in normal height
5	–	1 = row is displayed in level 2 mode 0 = row is displayed in level 1 mode
4 to 0	–	5-bit value defining full row background color

Table 4–4: Level 1 Spacing Attributes

Code	Function	Action	Notes
00	Alpha Black		set alpha mode and foreground color of following alpha characters select G0 character set
01	Alpha Red		
02	Alpha Green		
03	Alpha Yellow		
04	Alpha Blue		
05	Alpha Magenta		
06	Alpha Cyan		
07	Alpha White		
08	Flash Normal		
09	Flash Off	set at	
0A	Boxing Off	set at double	
0B	Boxing On	set at double	
0C	Size Normal	set at	
0D	Size Double Height		
0E	Size Double Width		
0F	Size Double		
10	Mosaic Black		set mosaic mode and foreground color of following mosaic characters select G1 character set
11	Mosaic Red		
12	Mosaic Green		
13	Mosaic Yellow		
14	Mosaic Blue		
15	Mosaic Magenta		
16	Mosaic Cyan		
17	Mosaic White		
18	Conceal	set at	
19	Contiguous Mosaic	set at	
1A	Separated Mosaic	set at	
1B	ESC		
1C	Black Background	set at	
1D	New Background	set at	
1E	Hold Mosaic	set at	
1F	Release Mosaic		
Shaded attributes are default at start of each display row.			

Table 4–5: Level 2 Parallel Attributes

7	6	5	4	3	2	1	0	Function
P	0	0	Color					Foreground Color
P	0	1	Color					Background Color
P	1	0	Flash					Flash Mode
P	1	1	0	0	L	Set		Character Set
P	1	1	0	1	0	DH	DW	Size
P	1	1	0	1	1	0	U	Underline/Separated
P	1	1	0	1	1	1	I	Inverted
P	1	1	1	0	0	0	C	Conceal
P	1	1	1	0	0	1	W	Window/Boxing
P	1	1	1	0	1	0	S	Shadow
P	1	1	1	0	1	1	IT	Italic

Table 4–6: Flash Modes

4	3	2	1	0	Function
0	0	0	0	0	Off
0	0	0	0	1	Normal
0	0	1	0	1	Normal Fast Phase 1
0	1	0	0	1	Normal Fast Phase 2
0	1	1	0	1	Normal Fast Phase 3
0	0	0	1	0	Inverted
0	0	1	1	0	Inverted Fast Phase 1
0	1	0	1	0	Inverted Fast Phase 2
0	1	1	1	0	Inverted Fast Phase 3
0	0	0	1	1	Color Table
0	0	1	1	1	Color Table Phase 1
0	1	0	1	1	Color Table Phase 2
0	1	1	1	1	Color Table Phase 3
1	0	0	x	x	Incremental
1	0	1	x	x	Decremental

Table 4–7: Color Look-Up Table

4	3	2	1	0	Display Color
0	0	0	0	0	Black
0	0	0	0	1	Red
0	0	0	1	0	Green
0	0	0	1	1	Yellow
0	0	1	0	0	Blue
0	0	1	0	1	Magenta
0	0	1	1	0	Cyan
0	0	1	1	1	White
0	1	0	0	0	Transparent
0	1	0	0	1	Reduced Red
0	1	0	1	0	Reduced Green
0	1	0	1	1	Reduced Yellow
0	1	1	0	0	Reduced Blue
0	1	1	0	1	Reduced Magenta
0	1	1	1	0	Reduced Cyan
0	1	1	1	1	Reduced White
1	x	x	x	x	Programmable

4.4. OSD Layer

Table 4–8: OSD Layer Control Codes

Code	Function	Notes
01	Underline On	only for 13 scanlines/character
02	Underline Off	
03	Flash On	
04	Flash Off	
05	Italics On	
06	Italics Off	
07	Transparent	layer becomes transparent
08	Shadow	layer becomes transparent and contrast is reduced to 66%
0C	END	end of layer
0D	CR	end of text line
0E – 7F	ASCII Character	using font 1 or font 2
80 – FF	Color Control	only one control code per character is allowed bit 0 = foreground color blue bit 1 = foreground color green bit 2 = foreground color red bit 3 = background color blue bit 4 = background color green bit 5 = background color red bit 6 = replace white by transparent bit 7 = 1
Shaded attributes are default at start of each text line.		

4.5. Character Set

10-bit Character Code = 2–bit Character Set (level 2) + 8–bit Character Value (level 1)

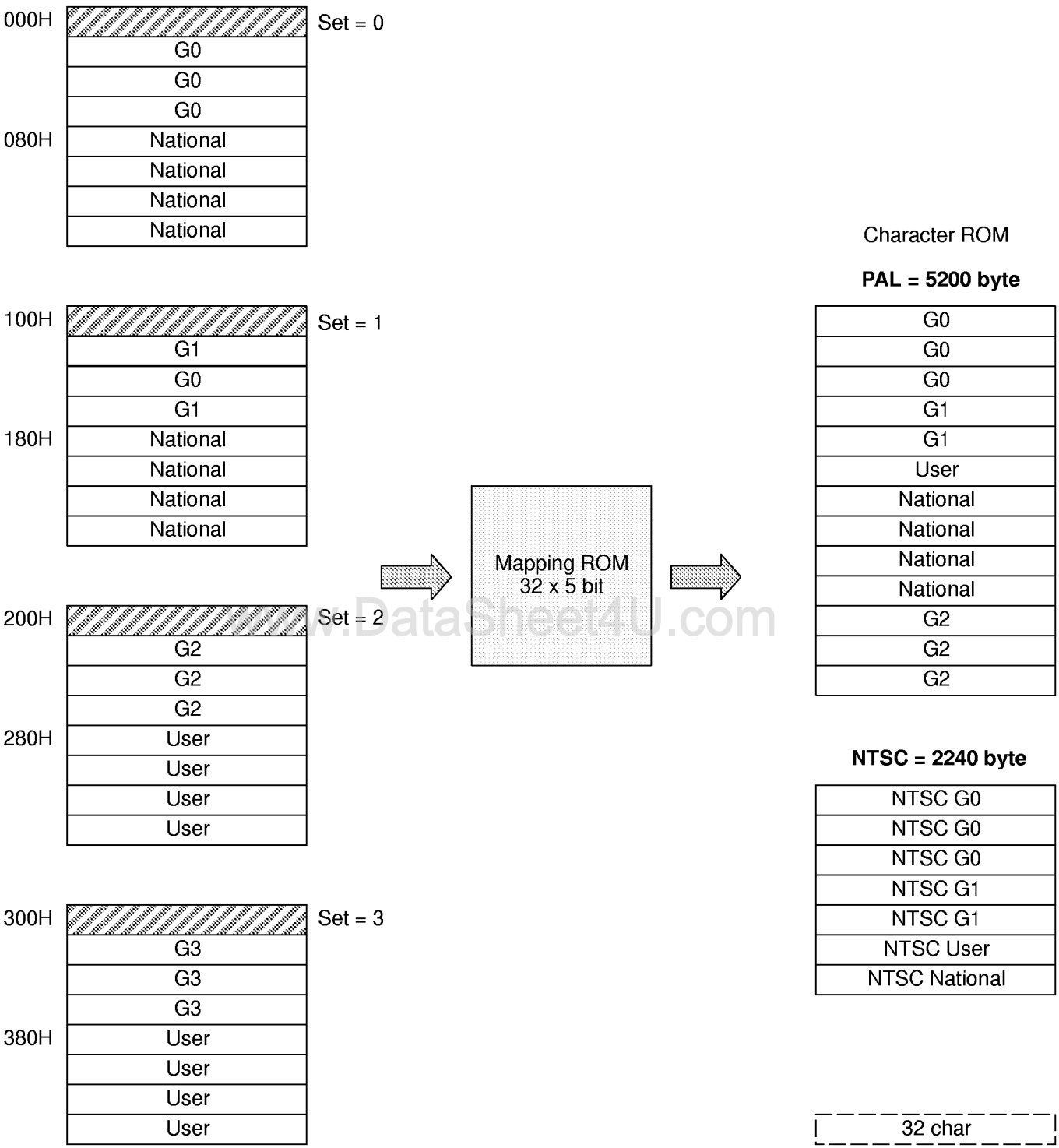


Fig. 4–5: Character Set Organization

4.6. Font Structure

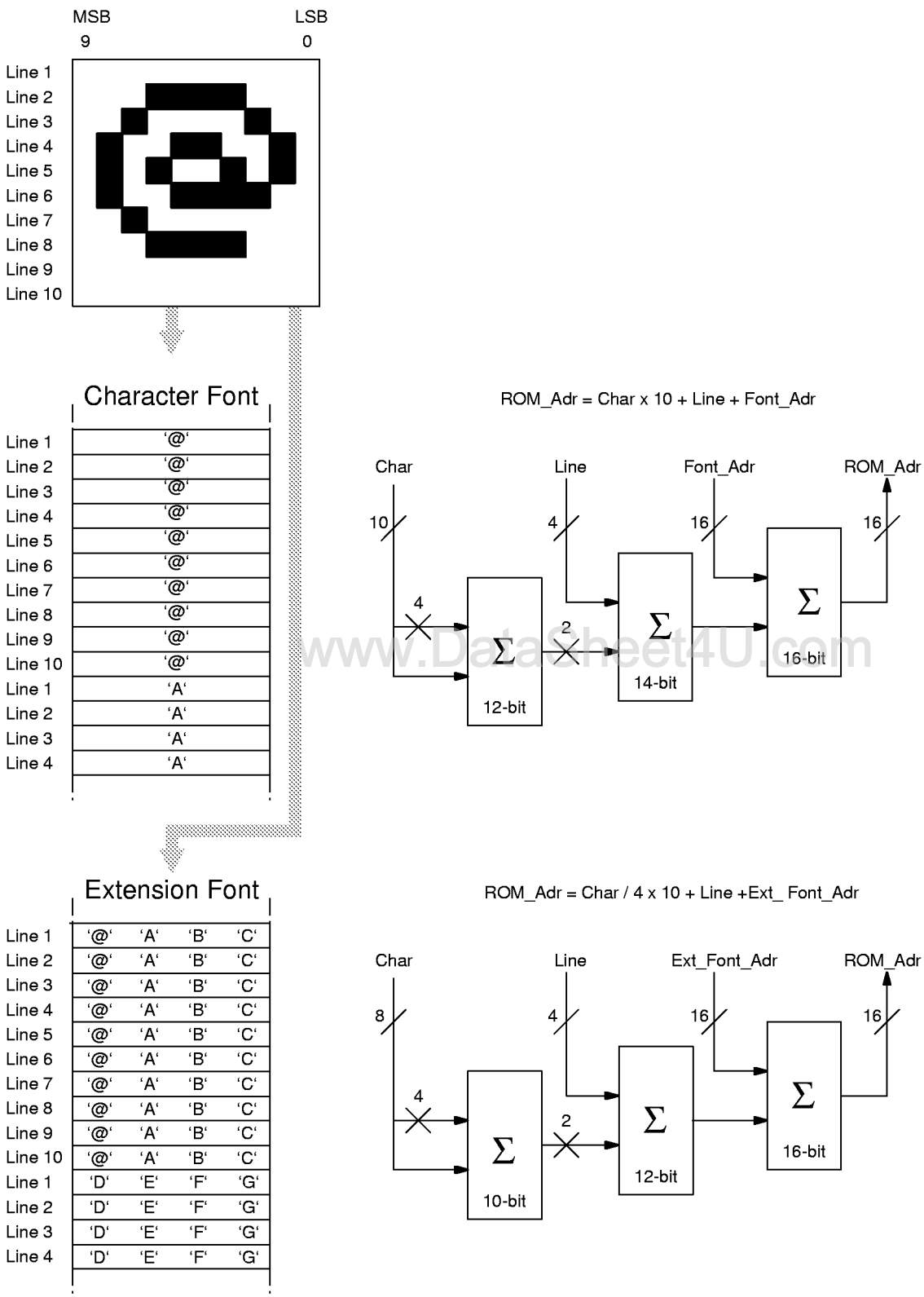


Fig. 4–6: Character Font Structure

4.7. Character Font

4.7.1. Character Set 0

Table 4–9: G0 font

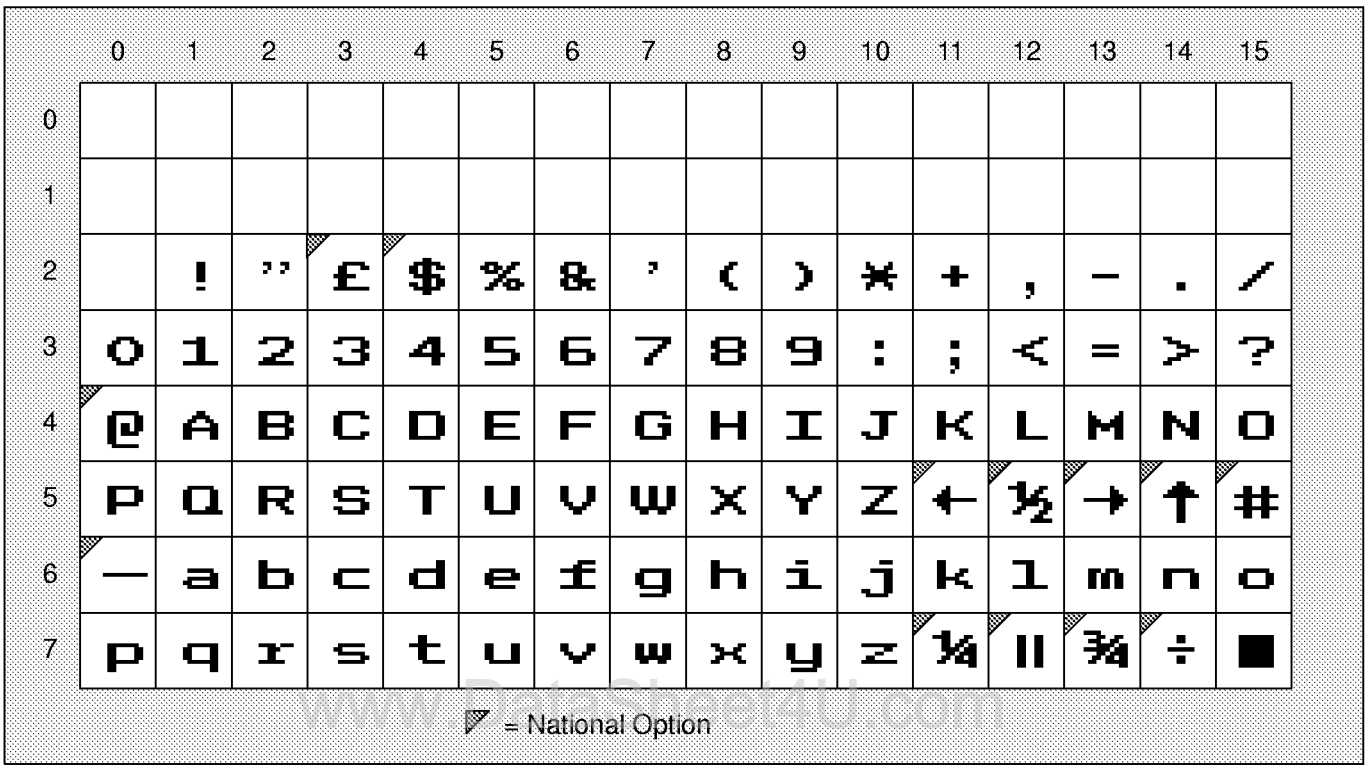
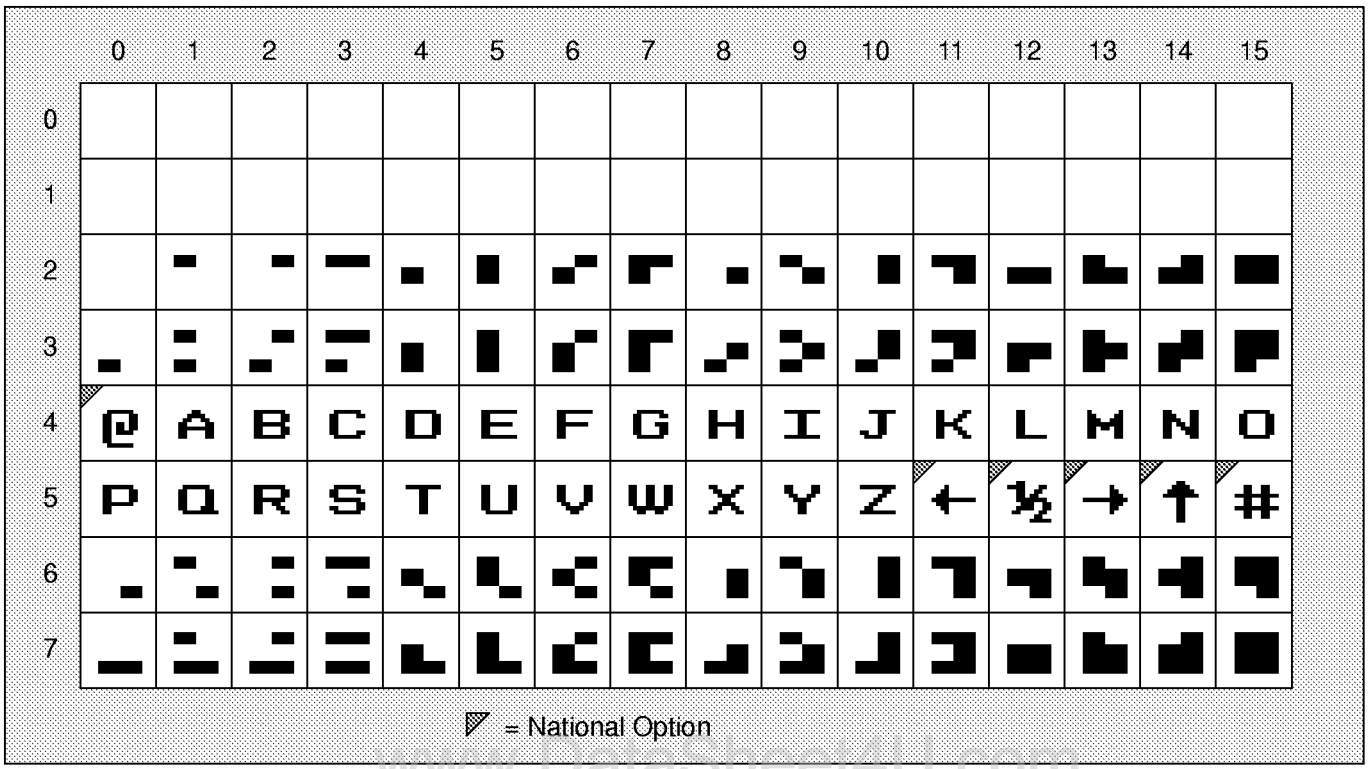


Table 4–10: National font

4.7.2. Character Set 1

Table 4–11: G1 font



4.7.3. Character Set 2

Table 4–12: G2 font

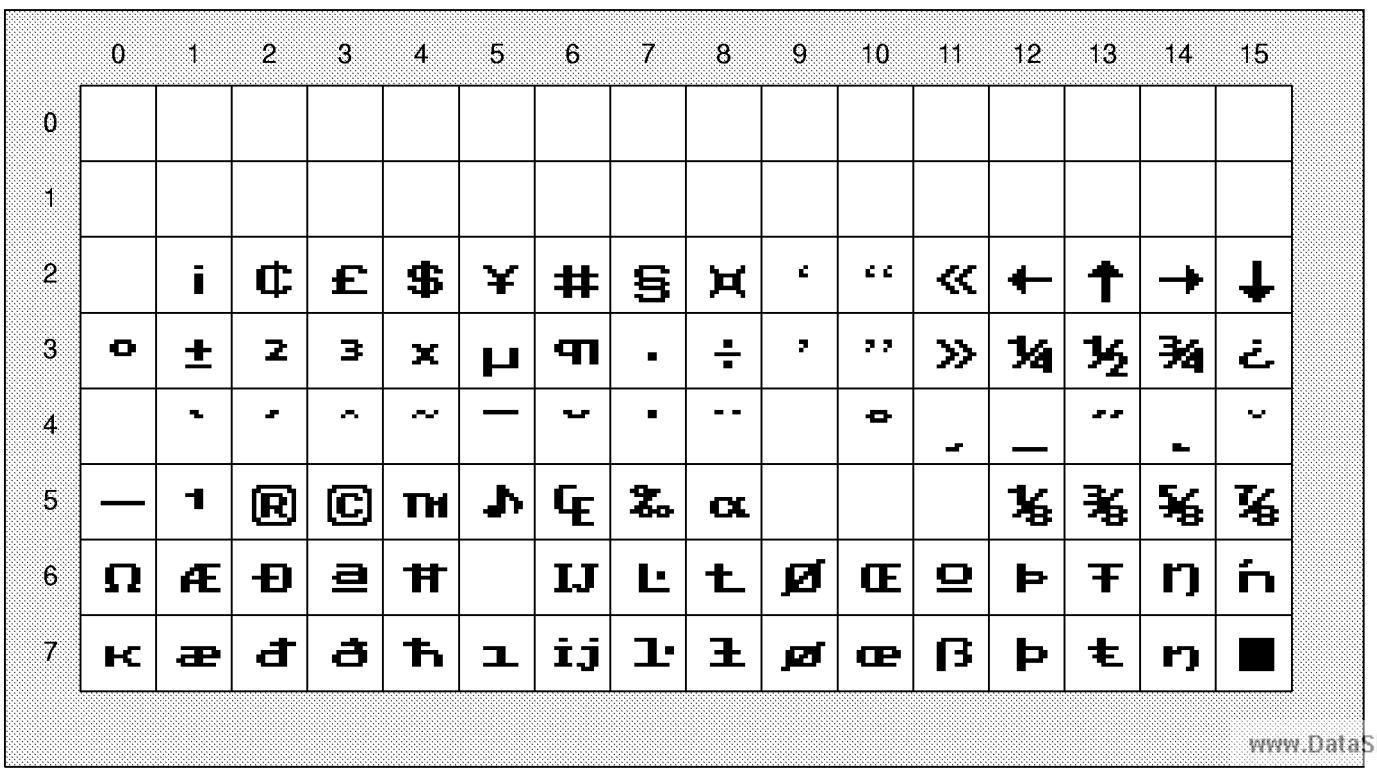


Table 4–13: User font TPU 3035/3040

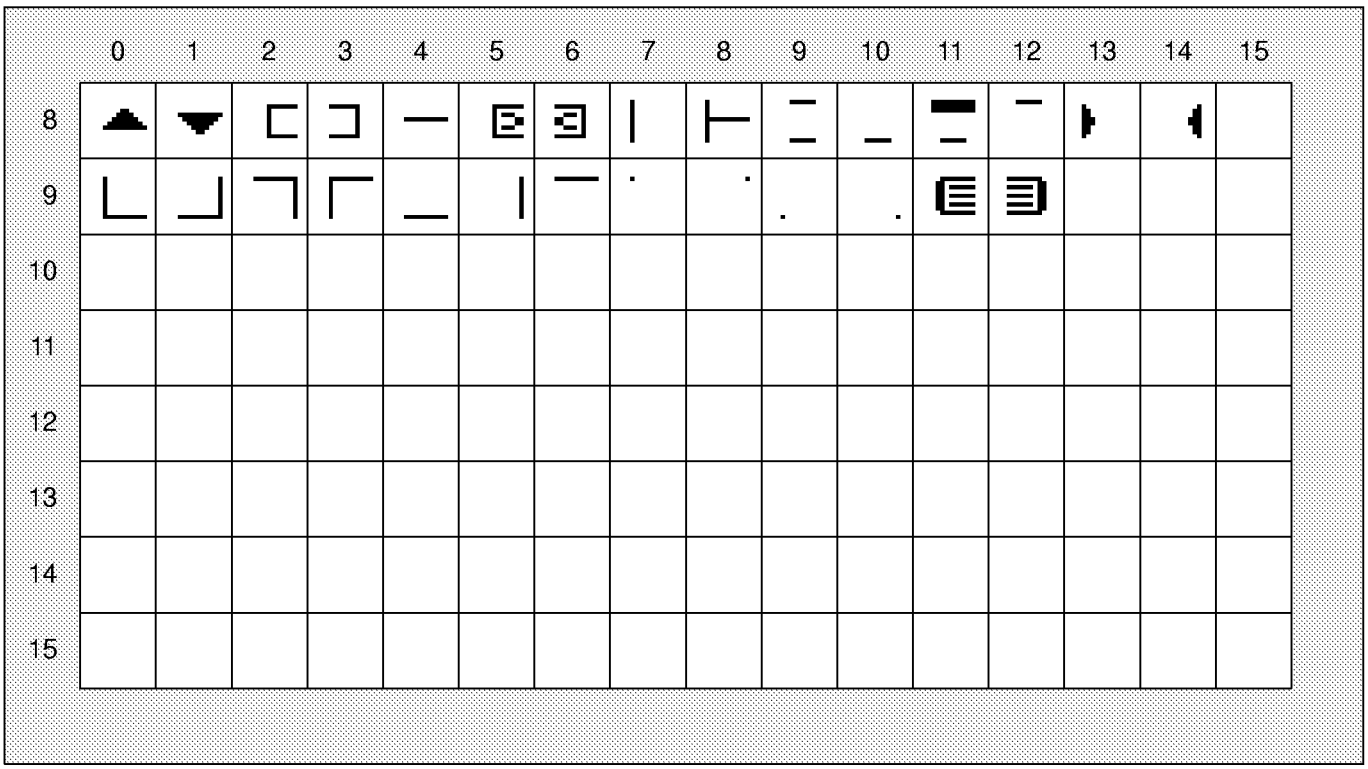
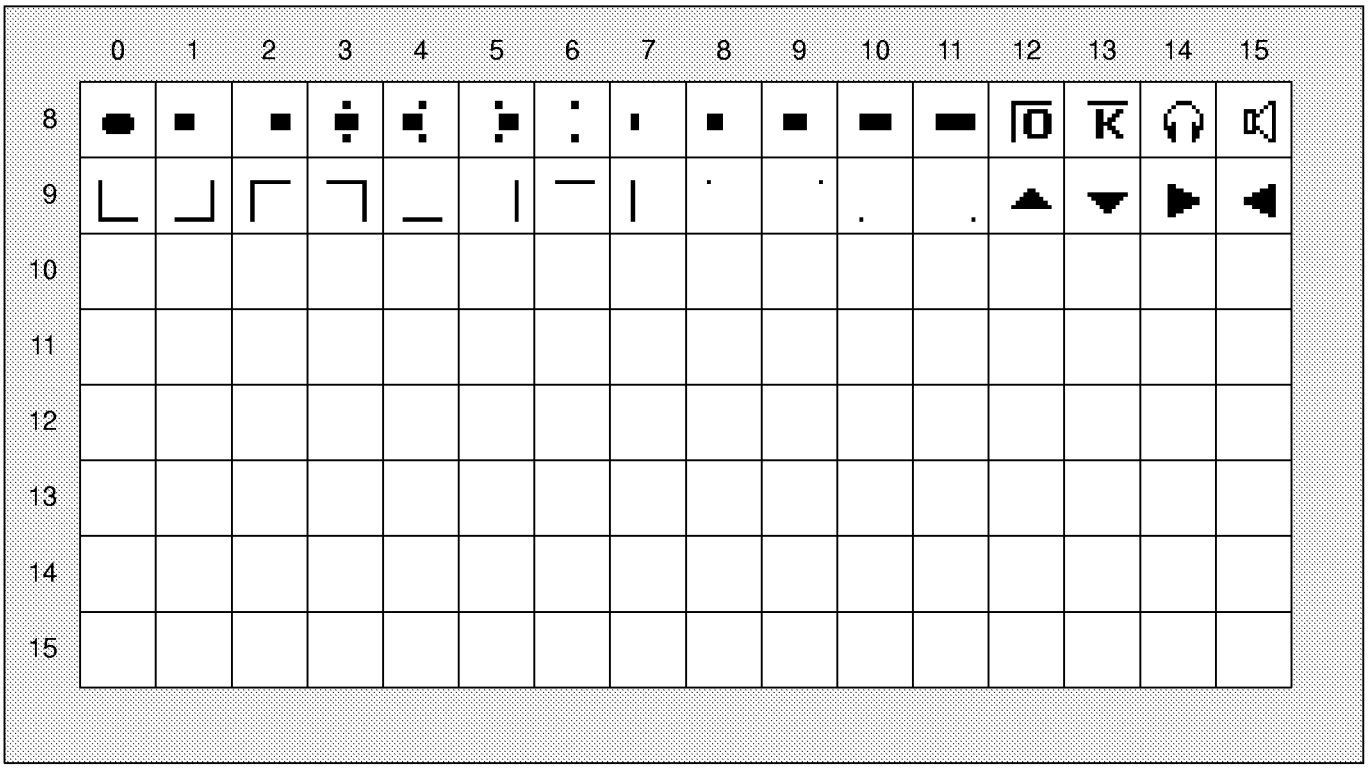


Table 4–14: User font TPU 3050



4.7.4. NTSC Character Sets

NTSC character sets G0 and G1 are identical to PAL character sets. There is no G2 character set for NTSC.

Table 4–15: NTSC national font

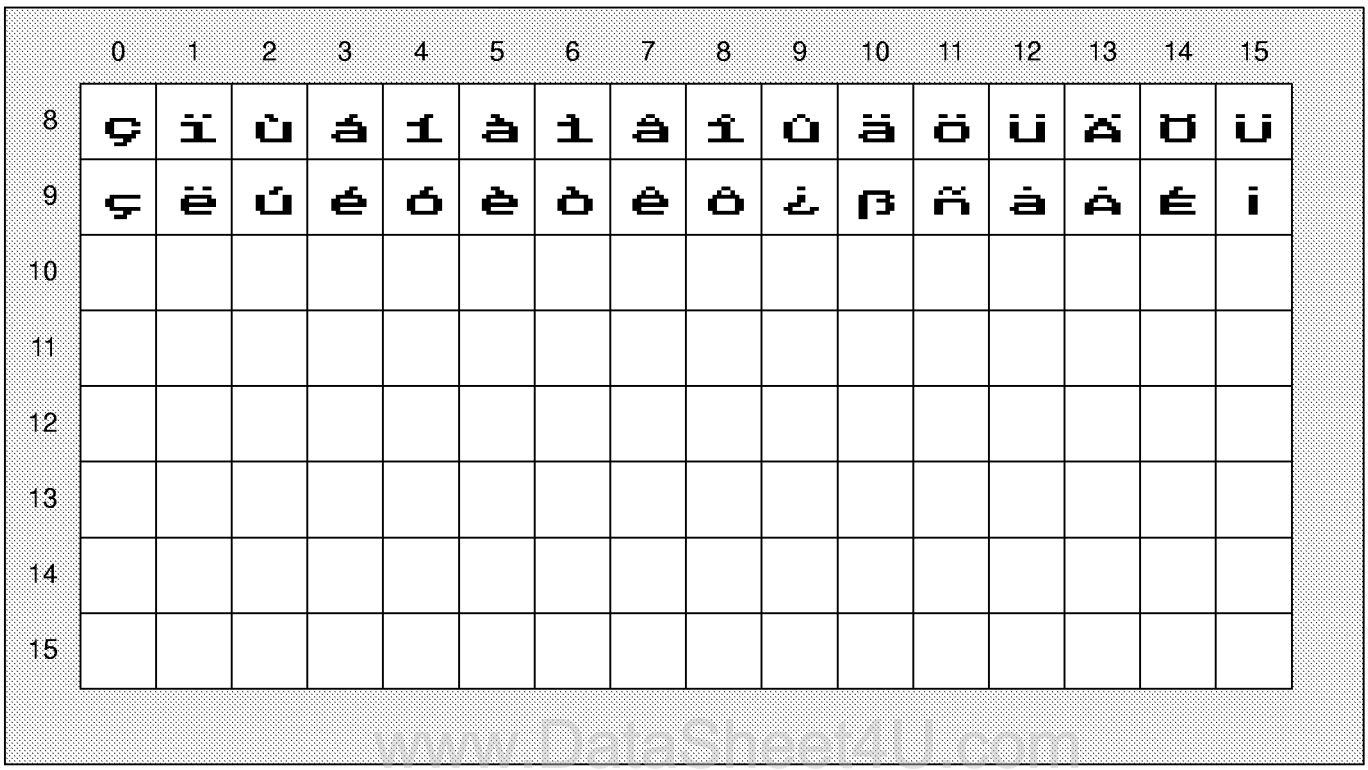
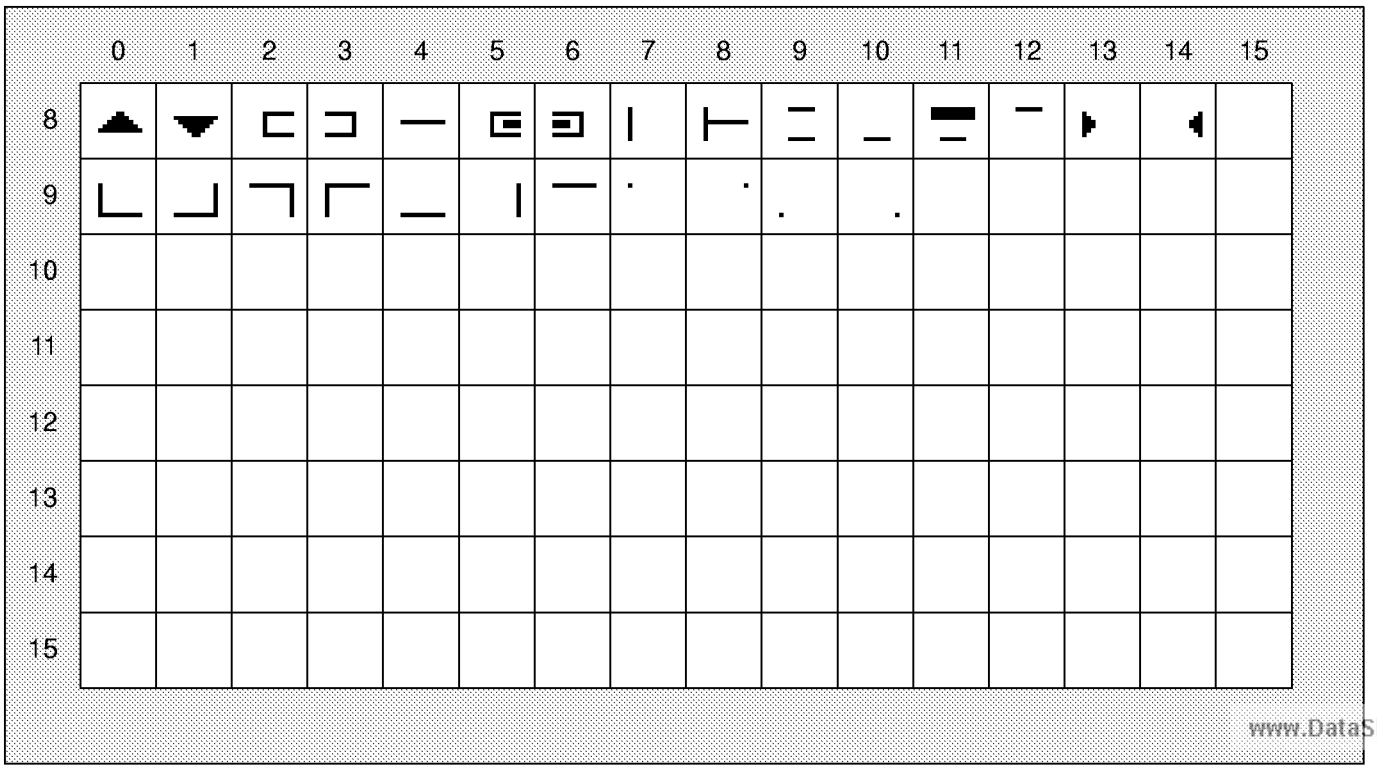


Table 4–16: NTSC user font



4.8. Character Mapping

Table 4–17: Character set options

Option Bits	Character Set				
C14,C13,C12	6	38	40	55	70
000	English	Polish	English (US)	English	English (US)
001	French	French	French	French	Slovakian
010	Swedish	Swedish	Swedish	Swedish	Hungarian
011	Czech	Czech	Czech	Turkish	Serbian
100	German	German	German	German	Albanian
101	Spanish	Serbian	Spanish	Spanish	Polish
110	Italian	Italian	Italian	Italian	Turkish
111	English	English	English	English	Rumanian

Table 4–18: National option mapping

Language	G0/G1 Table Position												
	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
Albanian	5/15	2/4	13/12	13/2	12/12	12/3	11/12	9/1	13/13	13/3	12/13	13/1	11/13
Czech	5/15	12/9	13/13	10/11	12/13	12/11	8/4	15/13	9/3	8/3	12/0	9/2	11/13
English	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
English (US)	5/15	2/4	4/0	14/4	13/5	15/4	14/6	13/0	14/7	14/5	15/6	15/5	15/7
French	9/3	8/1	8/5	9/1	9/7	8/2	8/8	5/15	9/5	8/7	9/8	8/9	9/0
German	5/15	2/4	15/0	8/13	8/14	8/15	14/6	13/0	14/0	8/10	8/11	8/12	9/10
Hungarian	5/15	9/2	9/14	8/4	8/14	10/1	12/15	11/15	9/3	9/4	8/11	8/3	8/12
Italian	2/3	2/4	9/3	14/0	9/0	5/13	5/14	5/15	8/2	8/5	9/6	9/5	8/6
Polish	5/15	14/3	13/15	13/8	12/7	15/8	13/3	9/4	10/9	13/9	13/7	15/9	13/11
Rumanian	5/15	14/1	10/14	10/5	14/14	14/11	10/6	15/1	10/15	8/7	14/15	12/5	8/8
Serbian	5/15	2/4	13/12	13/2	12/12	12/3	11/12	13/0	13/13	13/3	12/13	13/1	11/13
Slovakian	5/15	12/9	13/13	10/11	12/13	12/11	8/4	15/13	9/3	8/3	12/0	9/2	11/13
Spanish	9/0	2/4	9/15	8/3	9/3	8/4	9/4	9/2	9/9	8/12	9/11	9/5	8/5
Swedish	5/15	14/1	9/14	8/13	8/14	9/13	8/15	13/0	9/3	8/10	8/11	9/12	8/12
Turkish	13/6	10/13	10/8	14/14	8/14	8/0	8/15	10/12	15/1	14/15	8/11	9/0	8/12

4.9. Command Language

Table 4–19: Command Table

Code	Code	Command Name	No. Write Parameter	No. Read Parameter	Status Register
00	00	Dummy	0	0	x000 0000
01	01	Reset	0	0	x000 0000
02	02	Escape	0	0	x000 0000
03	03	Version	0	2	x000 0000
04	04	Test	0	0	x000 0000
05	05	Test	0	0	x000 0000
06	06	DRAM Mode	3	0	x000 0000
07	07	Acquisition Mode	5	2	x000 0000
08	08	Display Mode	3	0	x000 0000
09	09	Display TTX Pointer	2	0	x000 0000
10	0a	Display Pointer	3	0	x000 0000
11	0b	Display Clear	2	0	x000 0000
12	0c	Page Request	8	3	x0x0 0000
13	0d	Display Time Pointer	2	0	x000 0000
14	0e	Read DRAM Size	0	3	x000 0000
15	0f	Read VPS	0	15	x0x0 0000
16	10	Read Quality	0	4	x000 0000
17	11	Read Display Mode	0	3	x000 0000
18	12	Read Reset Source	0	1	x000 0000
19	13	Read Rolling Header	0	24	x000 0000
20	14	Read Page Info	2	7	x000 0000
21	15	Read Page Row	5	40	x0x0 0000
22	16	Change Page Info	3	0	x000 0000
23	17	Search MPET	0	1 + (n*4)	x0x0 0000
24	18	Read Display Page	0	4	x000 0000
25	19	Page Memory	2	0	x000 0000
26	1a	Display Page Request	5	0	x000 0000
27	1b	Page Table Reset	0	0	x000 0000
28	1c	Search Next Page	3	6	x0x0 0000
29	1d	Read Page Cycle	0	9	x000 0000
30	1e	Read TOP Code	2	2	x000 0000
31	1f	Read Rolling Time	0	8	x000 0000
32	20	Copy Page Row	8	0	x0x0 0000
33	21	Copy Data	7	0	x000 0000
34	22	Search Next TOP Code	3	4	x0x0 0000
35	23	Read Ghost Row	6	40	x0x0 0000
36	24	Read 8/30 Row	1	40	x0x0 0000
37	25	Read Priority	0	5	x000 0000
38	26	Page Priority	2	0	x000 0000
39	27	Search AIT	0	1 + (n*4)	x0x0 0000
40	28	Read TOP Status	0	2	x000 0000
41	29	Search AIT Title	2	17	x0x0 0000
42	2a	Reset Ghost Row Status	0	0	x000 0000
43	2b	Search MPT	0	1 + (n*4)	x0x0 0000
44	2c	Copy AIT Title	5	17	x0x0 0000
45	2d	Search Direct Choice	1	1 + (n*2)	x0x0 0000
46	2e	Read Hamming	1	1	x000 0000
47	2f	Read Hamming 2	3	3	x000 0000
48	30	Display Column	3+length	0	x000 0000
49	31	Display Fill	4	0	x000 0000
50	32	Read BTTL	0	9	x0x0 0000
51	33	Read Next Page	2	2	x000 0000
52	34	Change BTT magazine	1	0	x000 0000
53	35	Read WSS	0	15	x0x0 0000
54	36	Read CAPTION 1	0	7	x0x0 0000
55	37	Read CAPTION 2	0	7	x0x0 0000
56	38	OSD Font Pointer	5	0	x000 0000

Note:
If not otherwise designated, all parameters in the following table are specified as single bytes. As write parameter magazine numbers 8 and 0 have the same meaning, as read parameter the magazine number is a true 4-bit number (e.g. magazine 8 = 00001000). For write parameters the values in parentheses indicate default values after reset (in hex notation). For compatibility reasons every undefined bit in a write parameter should be set to '0'. Undefined bits in a read parameter should be treated as "don't care".

Table 4–20: Command Codes

Code	Function	Write Parameter	Read Parameter	Notes
		Operational & Test Commands		
00	Dummy			no action
01	Reset			software reset of 65C02
02	Escape			escape to other codes
03	Version		CPU pointer high CPU pointer low	show version in OSD layer CPU pointer to text in ROM
04	Test			reserved for testing
05	Test			reserved for testing
06	DRAM Mode	dram mode (06) flash inc (05) control enable (FF)		dram mode = I/O page register 028EH flash freq = flash inc / (256 * 0.00324) control enable: bit0 = C4 erase page bit1 = C5 news flash bit2 = C6 subtitle bit3 = C7 suppress header bit4 = C8 update indicator bit5 = C9 interrupted sequence bit6 = C10 inhibit display bit7 = $\overline{C11}$ magazine parallel
07	Acquisition Mode	acquisition mode (00) init subcode high (FF) init subcode low (FF) gain max (1F) filter max (1F)	gain filter	acquisition mode: bit0 = no slicer adaption bit1 = no bit error in framing code bit2 = limit slicer adaption init subcode: automatic subcode request after page table reset gain max: only used if bit2 = 1 filter max: only used if bit2 = 1
		Memory Management Commands		
14	Read DRAM Size		dram size high dram size low dram mode	dram size: 0080H = 256Kbit (slow mode) 0200H = 1Mbit (fast mode) 0800H = 4Mbit (fast mode) 2000H = 16Mbit (fast mode) dram mode: (only in TPU 3050) see I/O page register 028EH
25	Page Memory	dram bank (00) dram high (40)		start of page memory execute page table reset
27	Page Table Reset			reset page table reset ghost row status reset data service status reset cycle count reset memory count reset ghost count reset priorities clear rolling header clear VPS data clear WSS data
42	Reset Ghost Row Status			ghost row status: bit0 = row 24 in cycle bit1 = row 25 in cycle bit2 = row 26 in cycle bit3 = row 27 in cycle bit4 = row 28 in cycle bit5 = row 29 in cycle bit6 = row 30 in cycle bit7 = row 31 in cycle

Command Codes, continued

Code	Function	Write Parameter	Read Parameter	Notes
29	Read Page Cycle		ghost row status 2 byte cycle count 2 byte memory count 2 byte ghost count data service status memory status	= number of pages in cycle = number of pages in memory = number of ghost blocks in memory data service status: bit0 = 8/30 format 1 updated bit1 = 8/30 format 2 updated bit2 = VPS updated bit3 = WSS updated bit4 = CAPTION 1st field updated bit5 = CAPTION 2nd field updated memory status: bit0 = memory full
38	Page Priority	enable (00) border (FF)		enable: bit0 = enable priority manager border: min/max border for page priorities
37	Read Priority		highest priority lowest priority border priority magazine number page number	= max priority in page memory = min priority in page memory = min/max border for page priorities = page with lowest priority
	Page Related Commands			
12	Page Request	magazine number page number page subcode high page subcode low priority quantity start magazine number start page number	number of open requests removed magazine number removed page number	remove pages from memory beginning at start page if page priority is disabled, ignores start page if page priority is enabled magazine number: bit0–3= magazine number bit4 = not used bit5 = hex request bit6 = backward request bit7 = forced request = ignore cycle flag
20	Read Page Info	magazine number page number	page pointer high page pointer low subpage count ghost row count ring buffer index page subcode high page subcode low	= pointer from page table = number of subpages in chain = number of ghost rows in chain if page request with subcode F1xx
22	Change Page Info	magazine number page number page table flags		page table flags: bit0 = protection bit1 = update bit2 = not used bit3 = not used bit4 = not used bit5 = subpage bit6 = memory bit7 = cycle
28	Search Next Page	magazine number page number search code	magazine number page number page pointer high page pointer low subpage count ghost row count	search in page table for cycle flag magazine number: bit0–3= magazine number bit4 = take search code bit5 = hex search bit6 = backward search bit7 = include start page search code: bit0 = search protection flag bit1 = search update flag bit2–4= not used bit5 = search subpage flag bit6 = search memory flag bit7 = search cycle flag
51	Read Next Page	magazine number page number	magazine number page number	calculate next page number magazine number: bit0–3= magazine number bit4 = not used bit5 = hex calculation bit6 = backward calculation bit7 = not used

Command Codes, continued

Code	Function	Write Parameter	Read Parameter	Notes
21	Read Page Row	magazine number page number subpage number high subpage number low row number	40 byte row data	row 0 – 24
32	Copy Page Row	magazine number page number subpage number high subpage number low row number destination dram bank destination dram high destination dram low		copy 40byte text row from page memory into DRAM
35	Read Ghost Row	magazine number page number subpage number high subpage number low row number designation code	40 byte row data	row 25 – 28
		TOP Commands		
40	Read TOP Status		TOP status 1 TOP status 2	TOP status 1: bit0 = not used bit1 = MPT link in PLT bit2 = MPET link in PLT bit3 = AIT link in PLT bit4 = BTT in memory bit5 = MPT in memory bit6 = MPET in memory bit7 = AIT in memory TOP status 2: bit0–5 = not used bit6 = all MPET in memory bit7 = all AIT in memory
30	Read TOP Code	magazine number page number	BTT code MPT code	code: bit0–3 = data bit6 = hamming error
50	Read BTTL		BTTL error 8 byte BTTL data	BTTL error: bit6 = hamming error in BTTL BTTL data: bit0–3 = data bit6 = hamming error
52	Change BTT magazine	magazine number (01)		all TOP commands then refer to this magazine
43	Search MPT		number of MPTs magazine number page number subpage number high subpage number low ...	search in PLT
23	Search MPET		number of MPETs magazine number page number subpage number high subpage number low ...	search in PLT
39	Search AIT		number of AITs magazine number page number subpage number high subpage number low ...	search in PLT
41	Search AIT Title	magazine number page number	5 byte data 12 byte title	search in AIT magazine number: bit0–3 = magazine number (0#8) bit4–6 = not used bit7 = ignore title language data: bit0–3 = data bit6 = hamming error

Command Codes, continued

Code	Function	Write Parameter	Read Parameter	Notes
44	Copy AIT Title	magazine number page number destination dram bank destination dram high destination dram low	5 byte data 12 byte title	search in AIT and copy title into dram magazine number: bit0–3 = magazine number (0#8) bit4–6 = not used bit7 = ignore title language data: bit0–3 = data bit6 = hamming error
34	Search Next TOP Code	magazine number page number code condition	magazine number page number code code flag	search in BTT magazine number: bit0–3 = magazine number bit4–5 = not used bit6 = backward search bit7 = include start page code condition: low nibble = BTT code high nibble = search condition 0 = BTT code in low nibble 1 = BTT code # 0 2 = block page 3 = group page 4 = normal page 5 = subtitle page 6 = TV page 7 = block/TV page 8 = group/block/TV page 9 = subpage a = block/TV subpage b = group/block/TV subpage c = title page d = future page e = future page f = future page code: bit0–3 = BTT code bit6 = hamming error code flag: bit0 = subtitle page found bit1 = TV page found bit2 = block page found bit3 = group page found bit4 = normal page found bit5 = future page found bit6 = title page found bit7 = subpage found
45	Search Direct Choice	direct choice code	number of AIT entries magazine number page number ...	search in AIT

Command Codes, continued

Code	Function	Write Parameter	Read Parameter	Notes
		Miscellaneous Data Commands		
36	Read 8/30 Row	designation code	40 byte row data	only format 1 and 2 are supported 1st byte of row data is already hamming decoded
15	Read VPS		framing code counter 13 byte VPS data	= 51H = incremented every VPS reception = biphase decoded VPS bytes 3–15
53	Read WSS		framing code counter 13 byte WSS data	= 78H = incremented every WSS reception = 102 WSS elements from group 1 on
54	Read CAPTION 1		counter 6 byte CAPTION data	= incremented every reception in field 1 = 3x oversampling
55	Read CAPTION 2		counter 6 byte CAPTION data	= incremented every reception in field 2 = 3x oversampling
19	Read Rolling Header		24 byte rolling header	every row 0 in cycle
31	Read Rolling Time		8 byte rolling time	using time pointer
16	Read Quality		text lines hamming errors parity errors soft errors	updated every VBI
18	Read Reset Source		reset source	reset source: bit0 = clock supervision bit1 = voltage supervision bit2 = watchdog all bits in reset source are reset after read
46	Read Hamming	hamming (8,4) byte	data	hamming byte: bit0–3 = data bit6 = hamming error
47	Read Hamming 2	hamming (24,18) 1st byte hamming (24,18) 2nd byte hamming (24,18) 3rd byte	address mode data	address: bit0–5 = address bit7 = hamming error mode: bit0–4 = mode data: bit0–6 = data
33	Copy Data	source dram bank source dram high source dram low length destination dram bank destination dram high destination dram low		copy data from DRAM to DRAM

Command Codes, continued

Code	Function	Write Parameter	Read Parameter	Notes
		Display Commands		
17	Read Display Mode		display mode character set font	display mode: bit0 = forced boxing bit1 = reveal bit2 = box bit3 = time hold bit4 = page hold bit5 = row 24 hold bit6 = row 25 hold bit7 = row 26 hold
08	Display Mode	display mode (00) character set (06) font (00)		display mode: see above character set: 6,38,40,55,70 font: 0=PAL 1=NTSC
09	Display TTX Pointer	dram high (20) dram low (00)		page memory is copied to TTX pointer
10	Display Pointer	dram high (20) dram low (00) scroll counter (00)		display starts at pointer using scroll counter as line offset
11	Display Clear	dram high dram low		clear display bank beginning at pointer (26 rows * 86 bytes)
13	Display Time Pointer	dram high (20) dram low (20)		8byte time string from packet x/00 is copied to time pointer
26	Display Page Request	magazine number page number subpage number high subpage number low display delay (1E)		magazine number: bit0–3 = magazine number bit4 = change display delay bit5 = display clear (on update) bit6–7 = not used subpage number: F0xx for rolling subpages display delay: delay after row 0 reception in steps of 3.24ms (255 = no update) only used if bit4 = 1
24	Read Display Page		magazine number page number subpage number high subpage number low	current page in display
48	Display Column	dram high dram low length byte list ...		write to dram with increment of 86 byte = number of bytes in list
49	Display Fill	dram high dram low length character		repeated write of 1 character to dram = number of repeated writes
56	OSD Font Pointer	font mode (00) font pointer high font pointer low extension font pointer high extension font pointer low		font mode: bit0 = 0 = reset OSD font 2 pointer bit0 = 1 = load OSD font 2 pointer with following parameters

4.10. Memory Manager

The Memory manager is the core of the internal TPU 3040 software. Most of the acquisition and display related functions are controlled by this management.

4.11. Memory Organization

The upper end of the memory is defined by the DRAM size, the lower end can be defined with the *PAGE_MEMORY* command. Default memory organization is shown in Fig. 4–8.

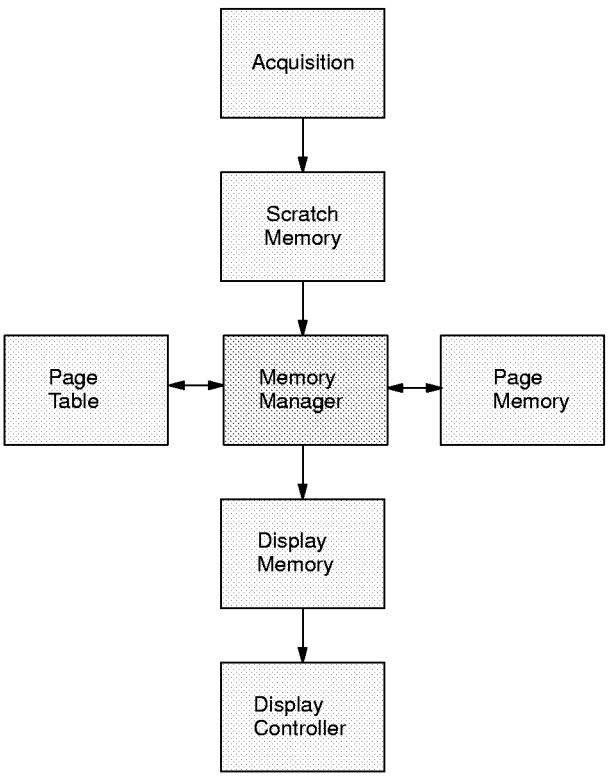


Fig. 4–7: Memory Manager

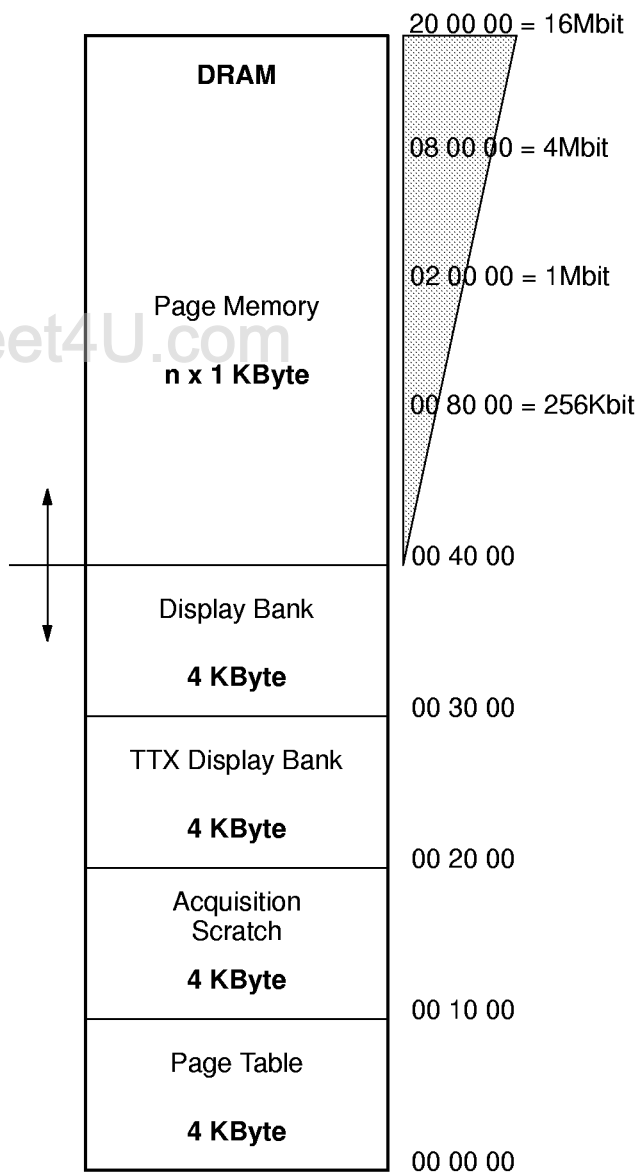


Fig. 4–8: Memory Organization

4.12. Page Table

The memory management is based on a fixed size page table, which has entries for every hexadecimal page number from 100 to 8FF. The page table starts with page 800 and contains a 2-byte page pointer for every page.

The page table can be read with the command *READ_PAGE_INFO* sending the page number and reading the 2-byte page pointer containing:

– DRAM pointer

– cycle flag

– memory flag

– subpage flag

– update flag

– protection flag

The DRAM pointer gives the location where the page is stored in memory. The page size is fixed to 1 KByte, only ghost rows are allocated dynamically.

The cycle flag will be set as soon as this page is detected in the transmission cycle even if it cannot be stored in memory. Only if the page is really stored in memory, the memory flag will be set. The subpage flag will be set for every page in cycle if the page subcode is different from 0000H or 3F7FH. The update flag is set every time a page is stored and will be reset only for the display page after updating the display memory. A page with protection flag set will never be removed from memory.

The memory manager uses page priorities to decide which pages should be stored or removed from memory. If no more memory is available, pages with lowest priority are removed automatically and the higher priority pages are stored at their place. By setting the page priority the programmer has control over the memory management.

The page table is fully controlled by the memory manager and should never be written by external software. To change the page table flags the command *CHANGE_PAGE_INFO* can be used.

Table 4–21: Page Table Format

Index	2-byte Page Pointer					
000	*start magazine 8*					
001						
...						
100	Cycle Flag	Memory Flag	Subpage Flag	11-bit DRAM Pointer	Update Flag	Protect Flag
...						
1F0	*hexadecimal pages (e.g. TOP)*					
...						
7FE						
7FF	*end magazine 7*					

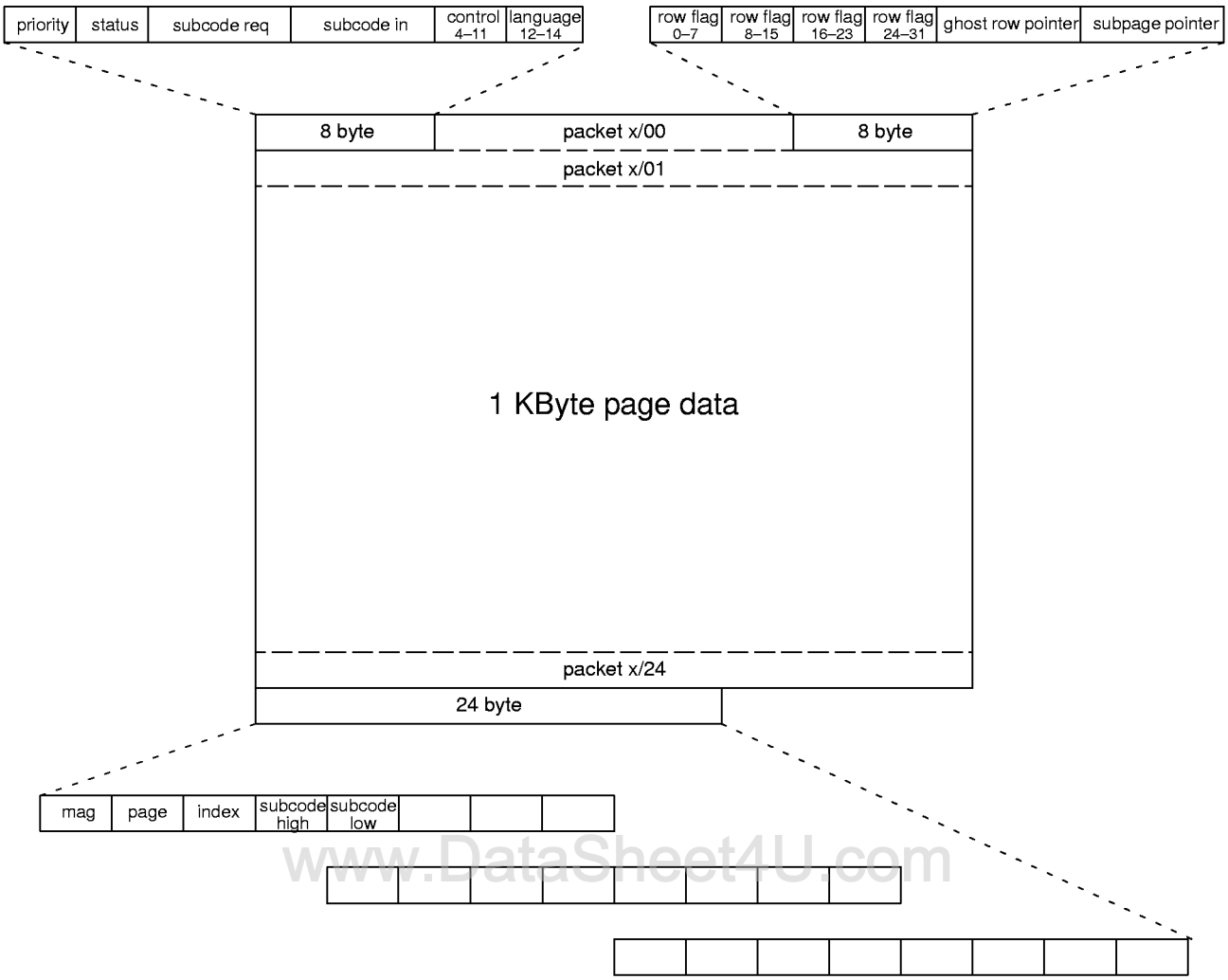


Fig. 4–9: Page Format

4.13. Ghost Row Organization

Page-related ghost rows are stored in blocks of 128 byte. These ghost blocks are linked together using 2 byte ghost row pointers. The first pointer can be found in the basic page, all following pointers are part of the block header. A zero pointer indicates the end of the chain.

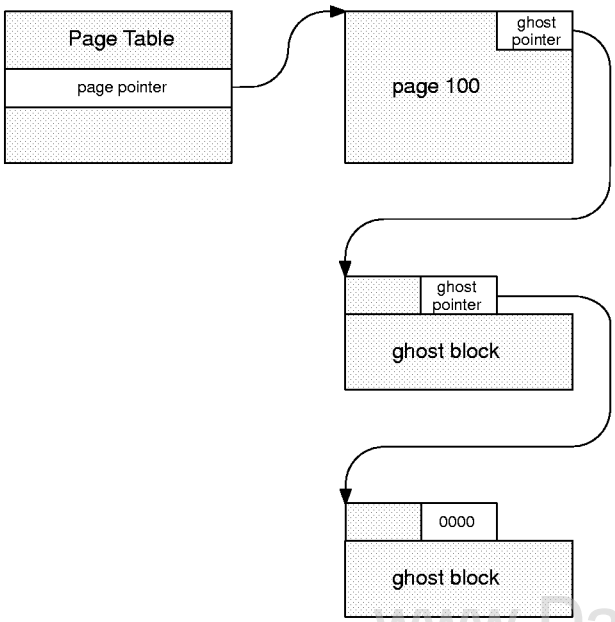


Fig. 4–10: Ghost Row Organization

Every ghost block contains 3 ghost rows which can be identified by 3 row identification bytes in the block header. The row identification contains designation code and row number. The row number is reduced to a 3-bit tag. All ghost rows in one block belong to the same page. If the memory manager removes a page from memory, the linked ghost blocks will also be removed.

Table 4–22: Ghost Row Identification

Row Number Tag	Row
000	empty
001	row 25
010	row 26
011	row 27
100	row 28
101	row 29
110	row 30
111	row 31

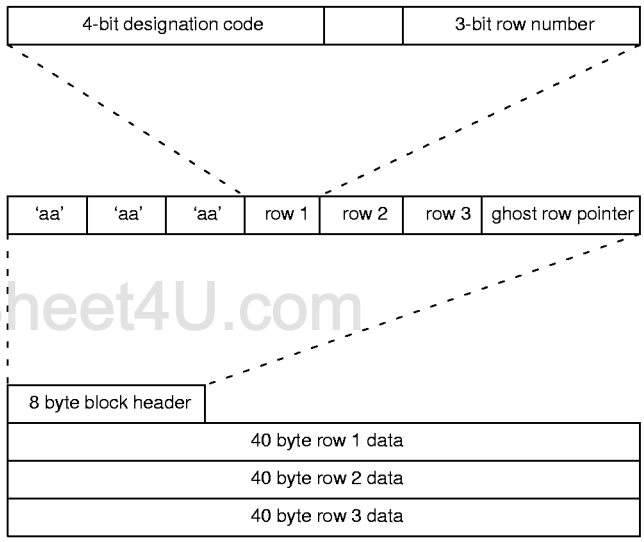


Fig. 4–11: Ghost Block Structure

4.14. Subpage Manager

Any page in cycle can have a number of subpages, identified by subcode. In normal mode the subpage manager will acquire only one subpage of every requested page. This subpage can be any if subcode FFFF is requested or it will be selected according to the requested subcode.

After a *PAGE_REQUEST* command with subcode F0xx, the subpage manager will acquire all subpages of the requested page. The subpages will be chained in the same order as they are transmitted, i.e. every new subcode will be added at the end of chain. The page table entry points to the subpage which was transmitted first after the page request. The *READ_PAGE_INFO* command will reply the page table pointer and the actual number of subpages in chain.

After a *PAGE_REQUEST* command with subcode F1xx, the subpage manager will acquire all subpages of the requested page but will allocate only a limited amount of memory to store these subpages. The parameter “page subcode low” will define the length (in number of subpages) of a ring buffer in page memory which will hold the recently received subpages. In this case, the *READ_PAGE_INFO* command will return an index pointing to the most recently updated subpage in chain, together with the subcode of this page.

The *DISPLAY_PAGE_REQUEST* command searches and displays a page according to the requested display subcode. The search starts from page table and continues through the subpage chain if there is any. A rolling header will be displayed if the requested subpage cannot be found in memory.

A requested display subcode FFFF (don’t care subcode) will only search and display the first subpage in chain, thus there is no rolling subpage anymore. A *DISPLAY_PAGE_REQUEST* command with subcode F0xx (follow subcode) will search and display the last received subpage in chain, thus it is possible to request all subpages in background while still showing rolling subpages in display.

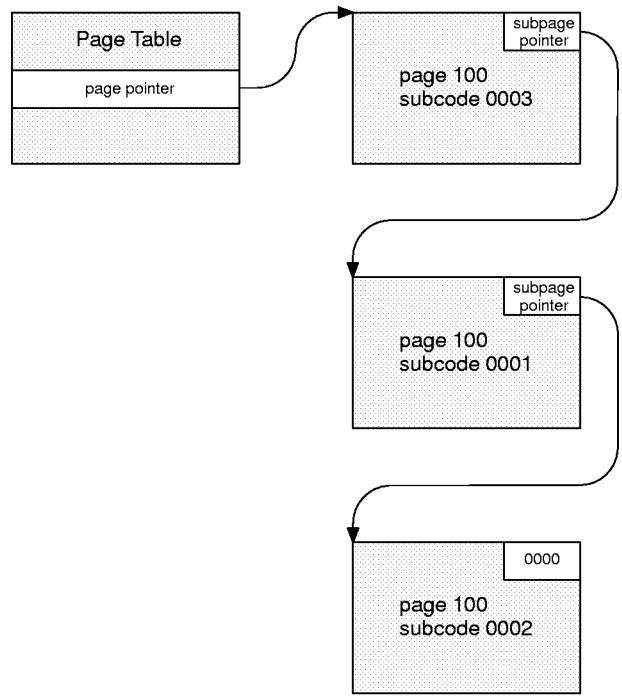


Fig. 4–12: Subpage Organization

4.15. I/O Page Definition

Most hardware related functions of the TPU 3040 are controlled by memory mapped I/O of the 65C02. The following table lists all available registers. For a more detailed description of the I/O page registers see next section.

The application software has access to the I/O page registers via I²C-bus using the CPU subaddresses SUB1 and SUB 2.

Reset values are written by TPU during initialization. Application software should only write into registers with user label 'Appl'!

Most of the I/O page registers are only write registers and will not return useful data when read by application software.

Table 4–23: I/O Page Register

Addr.	Mode	User	Reset	Name
0200 H	R/W	Test	00 H	Control Register
0201 H	W	Test	00 H	Test Mode
0202 H	W	Appl	00 H	Standby
0203 H	W	TPU	6C H	Watchdog
0204 H	R/W	Test	07 H	Supervision
0210 H	R/W	TPU	–	Interface Data
0211 H	R/W	TPU	00 H	Interface Status
0212 H	R	TPU	–	Interface Address
0213 H	W	Appl	01 H	Interface Mode
0220 H	R/W	TPU	FF H	Interrupt Source
0221 H	W	TPU	3B H	Interrupt Enable
0222 H	W	Appl	0F H	Interrupt & Timer Mode
0223 H	R	Appl	–	Timer Latch Low
0224 H	R	Appl	–	Timer Latch High
0225 H	R	Appl	–	Timer Count Low
0226 H	R	Appl	–	Timer Count High
0250 H	W	Appl	04 H	Clamping Start
0251 H	W	Appl	07 H	Blanking Stop
0252 H	W	Appl	00 H	Blanking Start
0253 H	W	Appl	37 H	Halfline Code
0254 H	W	Appl	60 H	Display Mode 1
0255 H	W	Appl	4D H	Display Mode 2
0256 H	W	Appl	07 H	Clamping Stop
025A H	W	Appl	35 H	PRIO Mode
025B H	R/W	Appl	00 H	FB Mode
0260 H	W	Appl	0060 H	OSD Layer Vertical Start
0261 H	W	Appl	0128 H	OSD Layer Vertical Stop
0262 H	W	Appl	16 H	OSD Layer Horizontal Start
0264 H	W	Appl	version	OSD Layer Text Pointer
0265 H	W	Appl	0138 H	OSD Layer 2nd Color Start
0266 H	W	Appl	0C H	OSD Layer 2nd Color
0267 H	W	Appl	0024 H	WST Layer Vertical Start
0268 H	W	Appl	0F H	WST Layer Horizontal Start
0269 H	W	Test	00 H	OSD Test
026A H	W	Appl	0128 H	WST Layer Vertical Stop
026B H	W	Appl	011E H	WST Layer Last Row
026C H	W	Appl	00 H	RGB Mode
026D H	W	Appl	00 H	Sync Mode
026E H	W	TPU	pal font	Display Font Pointer
026F H	W	Appl	8F H	Display Mode 3
0270 H	W	TPU	00 H	Display Mode 4
0271 H	W	Test	00 H	Display Test 1
0272 H	W	Test	00 H	Display Test 2
0273 H	W	TPU	00 H	Display Mode 5
0274 H	W	Test	00 H	Display Test 4
0280 H	R/W	TPU	00 H	DRAM Display Pointer Low
0281 H	R/W	TPU	20 H	DRAM Display Pointer Medium
0282 H	R/W	TPU	00 H	DRAM Display Pointer High
0283 H	R/W	TPU	00 H	DRAM Slicer Pointer Low
0284 H	R/W	TPU	10 H	DRAM Slicer Pointer Medium
0285 H	R/W	TPU	00 H	DRAM Slicer Pointer High
0286 H	R/W	TPU	–	DRAM CPU Write Pointer Low
0287 H	R/W	TPU	–	DRAM CPU Write Pointer Medium
0288 H	R/W	TPU	–	DRAM CPU Write Pointer High
0289 H	R/W	TPU	–	DRAM CPU Read Pointer Low
028A H	R/W	TPU	–	DRAM CPU Read Pointer Medium
028B H	R/W	TPU	–	DRAM CPU Read Pointer High
028C H	R/W	TPU	–	DRAM Data
028D H	R/W	TPU	–	DRAM Hamming Data
028E H	W	TPU	06 H	DRAM Mode
0290 H	W	TPU	01 H	ACQ Soft Slicer
0291 H	W	Appl	BE H	ACQ TTX Bitslicer Frequency Low
0292 H	W	Appl	0A H	ACQ TTX Bitslicer Frequency High
0293 H	W	Appl	FA H	ACQ VPS Bitslicer Frequency Low
0294 H	W	Appl	09 H	ACQ VPS Bitslicer Frequency High
0295 H	W	TPU	07 H	ACQ Filter Coefficient
0296 H	W	TPU	0D H	ACQ Data Slicer
0297 H	W	TPU	04 H	ACQ Accumulator Mode
0298 H	R	TPU	–	ACQ AC Accumulator
0299 H	R	TPU	–	ACQ FLT Accumulator
029A H	W	Test	00 H	ACQ Packet Header Low
029B H	W	Test	00 H	ACQ Packet Header High
029C H	R	TPU	–	ACQ Soft Error Counter
029D H	W	TPU	0F H	ACQ Sync Slicer
029E H	R	Appl	–	ACQ Sync Status
029F H	W	Appl	18 H	ACQ Standard
02A0 H	W	TPU	50 H	ACQ Analog Mode
02A1 H	W	Test	00 H	ACQ Test Mode
02A2 H	W	Test	00 H	ACQ Test Observe
02A3 H	W	Appl	00 H	ACQ Video Input
02A4 H	R	Appl	–	ACQ HSync Counter

4.16. I/O Page Register

Note:
For compatibility reasons, every undefined bit of a write register should be set to '0'. Undefined bits of a read register should be treated as "don't care".

0200 H	R/W	CONTROL REGISTER
Bit	Reset	Function
all	00 H	During reset the control register is loaded with the contents of the address FFF9H, but it can be read and written via software.
7	0	1 = CPU disable 0 = CPU enable
6	0	1 = program RAM disable 0 = program RAM enable
5	0	1 = program ROM disable 0 = program ROM enable
4	0	1 = character ROM disable 0 = character ROM enable
3	0	1 = DMA interface disable 0 = DMA interface enable
2	0	1 = I/O page disable 0 = I/O page enable
1	0	1 = test mode on 0 = test mode off
0	0	write: 1 = burnin test mode (only if test pin high) 0 = normal test mode read: 1 = burnin test mode 0 = normal test mode

0202 H	Write	STANDBY
Bit	Reset	Function
2	0	1 = digital circuitry power off (CPU still active with slow clock) 0 = digital circuitry power on
1	0	1 = analog circuitry power off 0 = analog circuitry power on
0	0	1 = character ROM power off 0 = character ROM power on

0203 H	Write	WATCHDOG
Bit	Reset	Function
all	6C H	reset watchdog if 8-bit value= 0x6c is written into this register all other values or time out will reset the chip

0204 H	R/W	SUPERVISION	
Bit	Reset	Function	
4	0	write enable only if test pin high write: 1 = short reset pulse 0 = long reset pulse	(15-bit FOSC)
3	0	write enable only if test pin high write: 1 = short watchdog period 0 = long watchdog period	(19-bit PH2)
2	1	write enabled per mask option write: 1 = watchdog enable 0 = watchdog disable	reset after read read: 1 = watchdog alarm 0 = watchdog sleeping
1	1	write disabled per mask option write: 1 = voltage supervision enable 0 = voltage supervision disable	reset after read read: 1 = voltage supervision alarm 0 = voltage supervision sleeping
0	1	write disabled per mask option write: 1 = clock supervision enable 0 = clock supervision disable	reset after read read: 1 = clock supervision alarm 0 = clock supervision sleeping

0210 H	R/W	INTERFACE DATA
Bit	Reset	Function
all	–	8-bit value

0211 H	R/W	INTERFACE STATUS	
Bit	Reset	Function	
7	–	write:	read: 1 = stop condition
6	–	write:	read: 1 = write data telegram
5	–	write:	read: 1 = read data telegram
4	–	write:	read: 1 = sub 4 telegram
3	–	write:	read: 1 = sub 3 telegram
2	–	write:	read: 1 = sub 2 telegram
1	–	write: 1 = reset interface (static)	read: 1 = sub 1 telegram
0	–	write: 0 = clear status	read: 1 = start condition

0212 H	Read	INTERFACE ADDRESS
Bit	Reset	Function
all	–	8-bit value

0213 H	Write	INTERFACE MODE
Bit	Reset	Function
2	0	1 = IIM Bus test enable (if normal test mode) 0 = IIM Bus test disable
1	0	1 = standby enable (if bit 2 of register 0202H = 1) 0 = standby disable
0	1	1 = IIC Bus 0 = IIM Bus

0220 H	R/W	INTERRUPT SOURCE
Bit	Reset	Function
all	FF H	write: 1 = reset interrupt source 0 = no action read: 1 = pending interrupt 0 = no pending interrupt
7	1	IR input falling edge
6	1	IR input rising edge
5	1	timer (bit 2^{12} from timer = every 3.24ms)
4	1	vertical sync display
3	1	slave interface (bus write of address or read/write of data register)
2	1	master interface
1	1	TTX acquisition start
0	1	TTX acquisition stop

0221 H	Write	INTERRUPT ENABLE
Bit	Reset	Function
all	3B H	for bit mapping see register 0220 H 1 = interrupt enable 0 = interrupt disable

0222 H	Write	INTERRUPT & TIMER MODE
Bit	Reset	Function
3	1	1 = timer not latched by falling edge of IR input (see Fig. 2–5) 0 = timer latched by falling edge of IR input
2	1	1 = timer not latched by rising edge of IR input (see Fig. 2–5) 0 = timer latched by rising edge of IR input
1	1	1 = IRQ generated by falling edge of IR input 0 = NMI generated by falling edge of IR input
0	1	1 = IRQ generated by rising edge of IR input 0 = NMI generated by rising edge of IR input

0223 H 0224 H 0225 H 0226 H	Read	TIMER LATCH LOW TIMER LATCH HIGH TIMER COUNT LOW TIMER COUNT HIGH
Bit	Reset	Function
all	–	8-bit value (see Fig. 2–5)

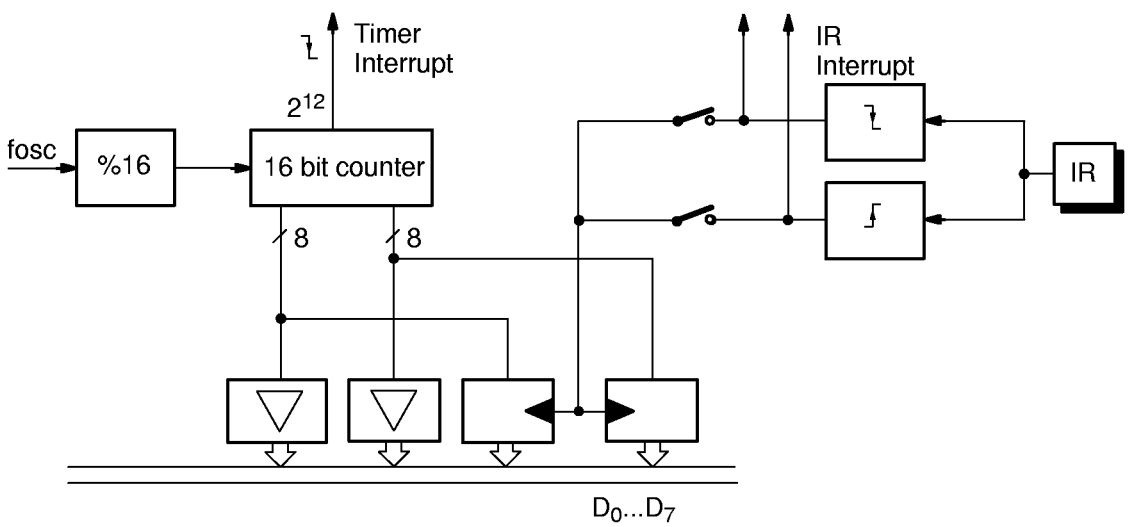


Fig. 2–5: Timer Structure

0250 H	Write	CLAMPING START
Bit	Reset	Function
all	04 H	horizontal start of clamping pulse in character increments (see Fig. 2–6) correct clamping pulse cannot be guaranteed if clamping start = clamping stop

0251 H	Write	BLANKING STOP
Bit	Reset	Function
all	07 H	horizontal stop of blanking pulse in character increments (see Fig. 2–6) correct blanking pulse cannot be guaranteed if blanking start = blanking stop

0252 H	Write	BLANKING START
Bit	Reset	Function
all	00 H	horizontal start of blanking pulse or self-timed HSYNC in character increments (see Fig. 2–6) correct blanking pulse cannot be guaranteed if blanking start = blanking stop

0256 H	Write	CLAMPING STOP
Bit	Reset	Function
all	07 H	horizontal stop of clamping pulse in character increments (see Fig. 2–6) correct clamping pulse cannot be guaranteed if clamping start = clamping stop

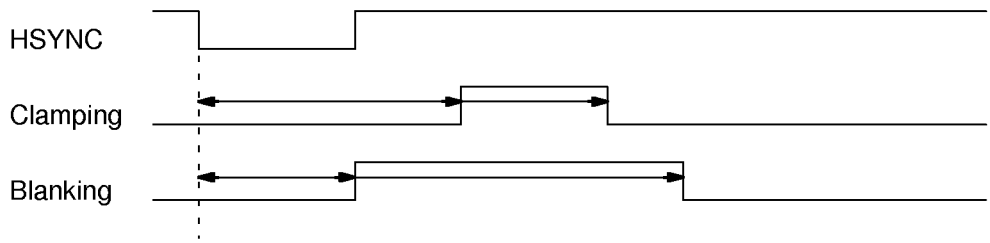


Fig. 2–6: Internal Timing

0253 H	Write	HALFLINE CODE
Bit	Reset	Function
all	37 H	horizontal position to reset HSYNC flip-flop in normal sync mode (in character) horizontal position of halfline HSYNC in self-timed interlaced mode (in character)

0254 H	Write	DISPLAY MODE 1
Bit	Reset	Function
7	0	1 = OSD layer always uses FONT 1 0 = OSD layer changes from FONT 1 to FONT 2 if ASCII≥20H
6	1	1 = enable OSD layer 0 = disable OSD layer
5	1	1 = active flash phase of OSD layer 0 = inactive flash phase of OSD layer
4	0	1 = 13 scanlines/character 0 = 8 scanlines/character
3 to 0	0	With this scan line the OSD layer starts display of the first text line. By slow incrementing of this value soft scroll begins.

0255 H	Write	DISPLAY MODE 2
Bit	Reset	Function
6	1	1 = skew delay enable 0 = skew delay disable
5	0	1 = VSYNC active high 0 = VSYNC active low
4	0	1 = HSYNC active high 0 = HSYNC active low
3	1	1 = 10.125MHz display clock 0 = 20.25MHz display clock
2	1	1 = font pointer offset 10 scanlines/character 0 = font pointer offset 8 or 16 scanlines/character (depending on bit 1)
1	0	1 = font pointer offset 16 scanlines/character 0 = font pointer offset 8 scanlines/character
0	1	1 = 10 scanlines/character 0 = 8 or 13 scanlines/character (depending on bit 4 in register 0254 H)

025A H	Write	PRIO MODE
Bit	Reset	Function
7 to 6	00	prio output strength: 3 = 8 mA output pull-down current 2 = 6 mA output pull-down current 1 = 4 mA output pull-down current 0 = 2 mA output pull-down current
5 to 3	110	prio code for shadow pixel
2 to 0	101	prio code for normal pixel

025B H	R/W	FB Mode
Bit	Reset	Function
all	00 H	write: read: every read resets status
7	0	color bit 4 (color output of OSD layer)
6	0	color bit 3 (color output of OSD layer)
5	0	1 = inverted shadow output / enable fastblank input 0 = normal shadow output / disable fastblank input
4	0	1 = inverted color output 0 = normal color output
3	0	1 = inverted fastblank output 0 = normal fastblank output
2	0	1 = shadow output on pin 30 0 = fastblank input on pin 30
1	0	1 = invert fastblank input read: dynamic fastblank status 0 = normal fastblank input
0	0	1 = fastblank input with high priority read: static fastblank status 0 = fastblank input with low priority

0260 H	Write	OSD LAYER VERTICAL START
Bit	Reset	Function
all	00 H 60 H	9-bit value defining vertical position (in scanline) 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

0261 H	Write	OSD LAYER VERTICAL STOP
Bit	Reset	Function
all	01 H 28 H	9-bit value defining vertical position (in scanline) 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

0262 H	Write	OSD LAYER HORIZONTAL START
Bit	Reset	Function
all	16 H	8-bit value defining horizontal start position (in character)

0264 H	Write	OSD LAYER TEXTPOINTER
Bit	Reset	Function
all	–	16-bit value defining memory address of text 1st write: bit7 to 0 = 8 MSBs 2nd write: bit7 to 0 = 8 LSBs

0265 H	Write	OSD LAYER 2nd COLOR START
Bit	Reset	Function
all	01 H 38 H	9-bit value defining vertical start for 2nd color (in scanline) 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

0266 H	Write	OSD LAYER 2nd COLOR
Bit	Reset	Function
6 to 0	0C H	7-bit value defining 2nd color 2nd color is used during 1 text row (8, 10 or 13 scanlines) after 2nd color start

0267 H	Write	WST LAYER VERTICAL START
Bit	Reset	Function
all	00 H 24 H	9-bit value defining vertical position (in scanline) 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

0268 H	Write	WST LAYER HORIZONTAL START
Bit	Reset	Function
all	0F H	8-bit value defining horizontal start position (in character)

026A H	Write	WST LAYER VERTICAL STOP
Bit	Reset	Function
all	01 H 28 H	9-bit value defining vertical position (in scanline) 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

026B H	Write	WST LAYER LAST ROW
Bit	Reset	Function
all	01 H 1E H	9-bit value defining last scanline of the last row to display level 1 double height after this scanline the level 1 double height attribute will not be decoded anymore 1st write: bit 0 = MSB 2nd write: bit7 to 0 = 8 LSBs

026C H	Write	RGB MODE
Bit	Reset	Function
6	0	1 = inverted CLK20 input 0 = normal CLK20 input
5	0	1 = WST layer mixed mode 0 = WST layer normal mode
4 to 3	0	11 = WST layer top 10 = WST layer opaque bottom 01 = WST layer transparent bottom 00 = WST layer disable
2	0	1 = OSD layer mixed mode 0 = OSD layer normal mode
1 to 0	0	11 = OSD layer top 10 = OSD layer opaque bottom 01 = OSD layer transparent bottom 00 = OSD layer disable

026D H	Write	SYNC MODE
Bit	Reset	Function
7	0	1 = MSYNC enable 0 = HSYNC & VSYNC enable
6	0	1 = CSYNC enable (for self-timed mode only) 0 = CSYNC disable
5	0	1 = double scan enable 0 = double scan disable
4	0	1 = blanking disable 0 = blanking enable
3	0	1 = NTSC self-timed mode 0 = PAL self-timed mode
2	0	1 = digital color mode enable 0 = digital color mode disable
1	0	1 = self-timed mode enable 0 = self-timed mode disable
0	0	1 = interlace enable = 312/313 (for self-timed mode only) 0 = interlace disable = 312/312

026E H	Write	DISPLAY FONT POINTER
Bit	Reset	Function
all	–	4 x 16 value defining memory address of related font WST layer always uses font 1 order of loading: extension font 1 extension font 2 font 1 font 2 for every fontpointer: 1st write: bit7 to 0 = 8 MSBs 2nd write: bit7 to 0 = 8 LSBs

026F H	Write	DISPLAY MODE 3
Bit	Reset	Function
7	1	1 = 10 pixel/character 0 = 8 pixel/character
6	0	1 = double dot size in vertical direction (OSD layer only) 0 = normal dot size in vertical direction
5	0	1 = double dot size in horizontal direction (OSD layer only) 0 = normal dot size in horizontal direction
4	0	1 = black colors replaced by transparent & shadow (OSD layer only) 0 = black colors displayed black
3 to 0	F H	4-bit value defining delay of horizontal start for both layers (in pixel) delay = mod_{16} (character_width – 2 – value) (leftmost position should not be used!)

0270 H	Write	DISPLAY MODE 4
Bit	Reset	Function
2	0	1 = boxing enable 0 = boxing disable
1	0	1 = reveal enable 0 = reveal disable
0	0	This bit is taken as flash clock for the WST layer, the frequency should be around 6 Hz.

0273 H	Write	DISPLAY MODE 5
Bit	Reset	Function
4	0	WST layer scan line counter preset (LSB for zoom mode)
3 to 0	0	WST layer scan line counter preset

0280 H 0283 H 0286 H 0289 H	R/W	DRAM DISPLAY POINTER LOW DRAM SLICER POINTER LOW DRAM CPU WRITE POINTER LOW DRAM CPU READ POINTER LOW
Bit	Reset	Function
7 to 0	–	8 least significant bits of 21 bit address pointer 12 LSBs of 21 bit address pointer are running with autoincrement read value is only specified when pointer is not incrementing

0281 H 0284 H 0287 H 028A H	R/W	DRAM DISPLAY POINTER MEDIUM DRAM SLICER POINTER MEDIUM DRAM CPU WRITE POINTER MEDIUM DRAM CPU READ POINTER MEDIUM
Bit	Reset	Function
all	–	8 medium bits of 21 bit address pointer 12 LSBs of 21 bit address pointer are running with autoincrement read value is only specified when pointer is not incrementing writing this register clears all lower bits of related pointer

0282 H 0285 H 0288 H 028B H	R/W	DRAM DISPLAY POINTER HIGH DRAM SLICER POINTER HIGH DRAM CPU WRITE POINTER HIGH DRAM CPU READ POINTER HIGH
Bit	Reset	Function
4 to 0	–	5 most significant bits of 21 bit address pointer static (no autoincrement) writing this register clears all lower bits of related pointer

028C H	R/W	DRAM DATA
Bit	Reset	Function
all	–	8 bit value

028D H	R/W	DRAM HAMMING DATA
Bit	Reset	Function
all	–	8 bit value writing this register resets hamming decoder

028E H	Write	DRAM MODE
Bit	Reset	Function
5	0	1 = SRAM mode enable (only available in TPU 3050) 0 =DRAM mode enable
4	0	1 = next CPU write without WEQ but with address increment 0 = normal CPU write mode
3	0	1 = reset address pointer and switch off refresh during standby 0 = keep address pointer and refresh during standby
2	1	1 = display channel enable 0 = display channel disable
1	1	1 = slicer channel enable 0 = slicer channel disable
0	0	1 = slow mode timing 0 =fast mode timing

0290 H	Write	ACQ SOFT SLICER
Bit	Reset	Function
4 to 0	01 H	5 bit binary soft slicer level is compared with ABS[data] ($-32 \leq data \leq +31$)

0291 H 0293 H	Write	ACQ TTX BITSLICER FREQUENCY LOW ACQ VPS BITSLICER FREQUENCY LOW
Bit	Reset	Function
all	–	8 LSBs of bitslicer frequency

0292 H 0294 H	Write	ACQ TTX BITSLICER FREQUENCY HIGH ACQ VPS BITSLICER FREQUENCY HIGH	
Bit	Reset	Function	
3	1	1 = PHINC enable 0 = PHINC disable	phase inc = Freq*(1 + 1/8) before framing code phase inc = Freq*(1 + 1/16) after framing code phase inc = Freq
2 to 0	–	3 MSBs of bitslicer frequency	Freq = 2^{11} * Bitfreq / 20.25MHz = 702 for PAL = 579 for NTSC = 506 for VPS or WSS = 153 for CAPTION

0295 H	Write	ACQ FILTER COEFFICIENT
Bit	Reset	Function
5 to 0	07 H	high pass filter coefficient in 2's complement 100000 = not allowed 100001 = −31 000000 = 0 011111 = +31

0296 H	Write	ACQ DATA SLICER	
Bit	Reset	Function	
5 to 0	0D H	6-bit binary data slicer level is compared with ABS[data]	(−32≤data≤ +31)

0297 H	Write	ACQ ACCUMULATOR MODE	
Bit	Reset	Function	
3	0	1 = soft error correction disable 0 = soft error correction enable	
2	1	1 = AC & FLT accu disable 0 = AC & FLT accu enable	(only during VPS&CAPTION line)
1	0	1 = DC accu disable 0 = DC accu enable	
0	0	1 = reset DC & AC & FLT accu 0 = no action	(one shot)

0298 H 0299 H	Read	ACQ AC ACCUMULATOR ACQ FLT ACCUMULATOR	
Bit	Reset	Function	
all	–	8 MSBs of 16bit accu accu increment is 6-bit binary ABS[data-slicer_level] these 8 MSBs are reset after read read must occur when accu is not active	(−32≤data≤ +31)

029A H	Write	ACQ PACKET HEADER LOW
Bit	Reset	Function
all	00 H	8 LSBs of MAC packet address

029B H	Write	ACQ PACKET HEADER HIGH
Bit	Reset	Function
7 to 4	6	4-bit framing code window every detected clock-runin loads window counter with 4-bit value * 2 (e.g. 6 → 12-bit window) window counter is clocked down to 0 with teletext bit rate slicer will ignore text line if no framing code is found inside framing code window 0000 = disable framing code window
3	0	1 = subframe 2 MAC packet acquisition enable 0 = subframe 2 MAC packet acquisition disable
2	0	1 = subframe 1 MAC packet acquisition enable 0 = subframe 1 MAC packet acquisition disable
1 to 0	0	2 MSBs of MAC packet address

029C H	Read	ACQ SOFT ERROR COUNTER
Bit	Reset	Function
5 to 0	–	6-bit soft error counter counts number of soft error corrected bytes counter stops at 63 reset after read

029D H	Write	ACQ SYNC SLICER
Bit	Reset	Function
7	0	1 = vertical sync window disable 0 = vertical sync window enable
6 to 0	00 H	7-bit binary sync slicer level is compared with binary data (0≤data≤127)

029E H	Read	ACQ SYNC STATUS	
Bit	Reset	Function	
7	–	1 = field 1 0 = field 2	set at line 624 (PAL) or line 524 (NTSC) reset at line 313 (PAL) or line 263 (NTSC)
6	–	1 = vertical retrace 0 = vertical window	set at line 628 (PAL) or line 528 (NTSC) reset at line 624 (PAL) or line 524 (NTSC)

029F H	Write	ACQ STANDARD
Bit	Reset	Function
7	0	1 = CAPTION enable in field 2 0 = CAPTION disable in field 2
6	0	1 = CAPTION enable in field 1 0 = CAPTION disable in field 1
5	0	1 = VPS enable 0 = VPS disable
7 to 5	0	VPS and CAPTION cannot be used at the same time, therefore these combinations are used to enable WSS reception on a PAL+ signal 0 = 1 = VPS 2 = CAPTION field 1 3 = WSS & VPS 4 = CAPTION field 2 5 = WSS & VPS 6 = CAPTION field 1&2 7 = WSS
4	1	1 = TTX enable 0 = TTX disable
3	1	1 = MAC VBI channel A 0 = MAC VBI channel B
2	0	1 = MAC packet acquisition enable 0 = MAC VBI acquisition enable
1	0	1 = NTSC mode 0 = PAL mode
0	0	1 = MAC mode 0 = composite video mode
1 to 0	0	MAC and NTSC cannot be used at the same time, therefore this combination is used to enable full VBI data reception in Caption mode

02A0 H	Write	ACQ ANALOG MODE
Bit	Reset	Function
7	0	1 = full N clamping (−150 µA) 0 = half N clamping (− 75 µA)
6	1	1 = N clamping disable 0 = N clamping enable (−150 µA if data < sync slicer level)
5	0	1 = clamping disable 0 = clamping enable (+225 µA if data = 0, −6 µA static)
4 to 0	10 H	5 bit analog gain of AGC 31 = 12dB 16 = 6dB 00 = 0dB

02A3 H	Write	ACQ VIDEO INPUT
Bit	Reset	Function
0	0	1 = video input 2 (pin 44) 0 = video input 1 (pin 42)

02A4 H	Read	ACQ HSYNC COUNTER
Bit	Reset	Function
7 to 0	0	number of detected horizontal sync pulses per frame divided by 4 sync pulse is detected if within horizontal window of HPLL counter is latched with vertical sync, the register can be read at any time

5. Application

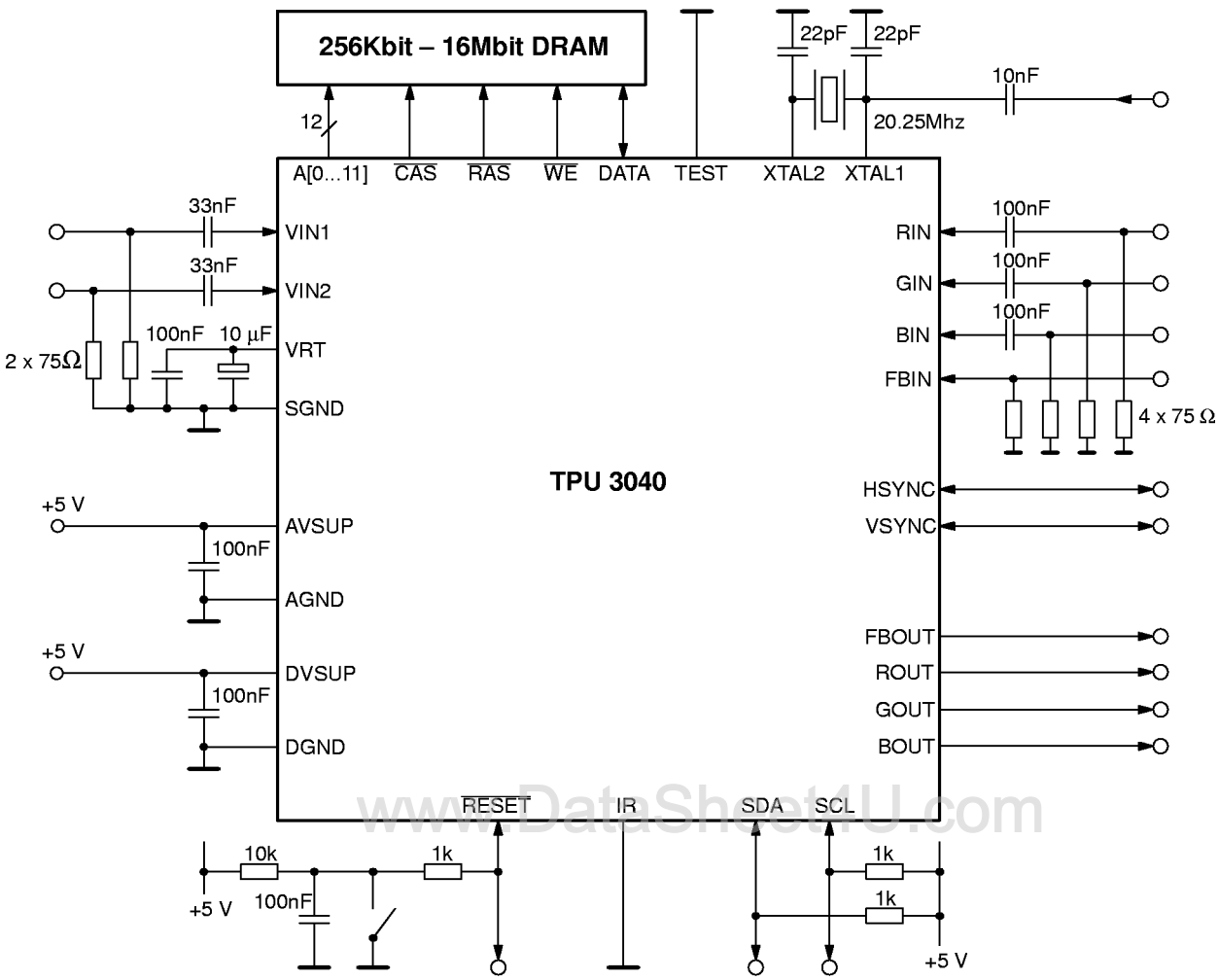


Fig. 5–1: TPU 3040 Application with DRAM

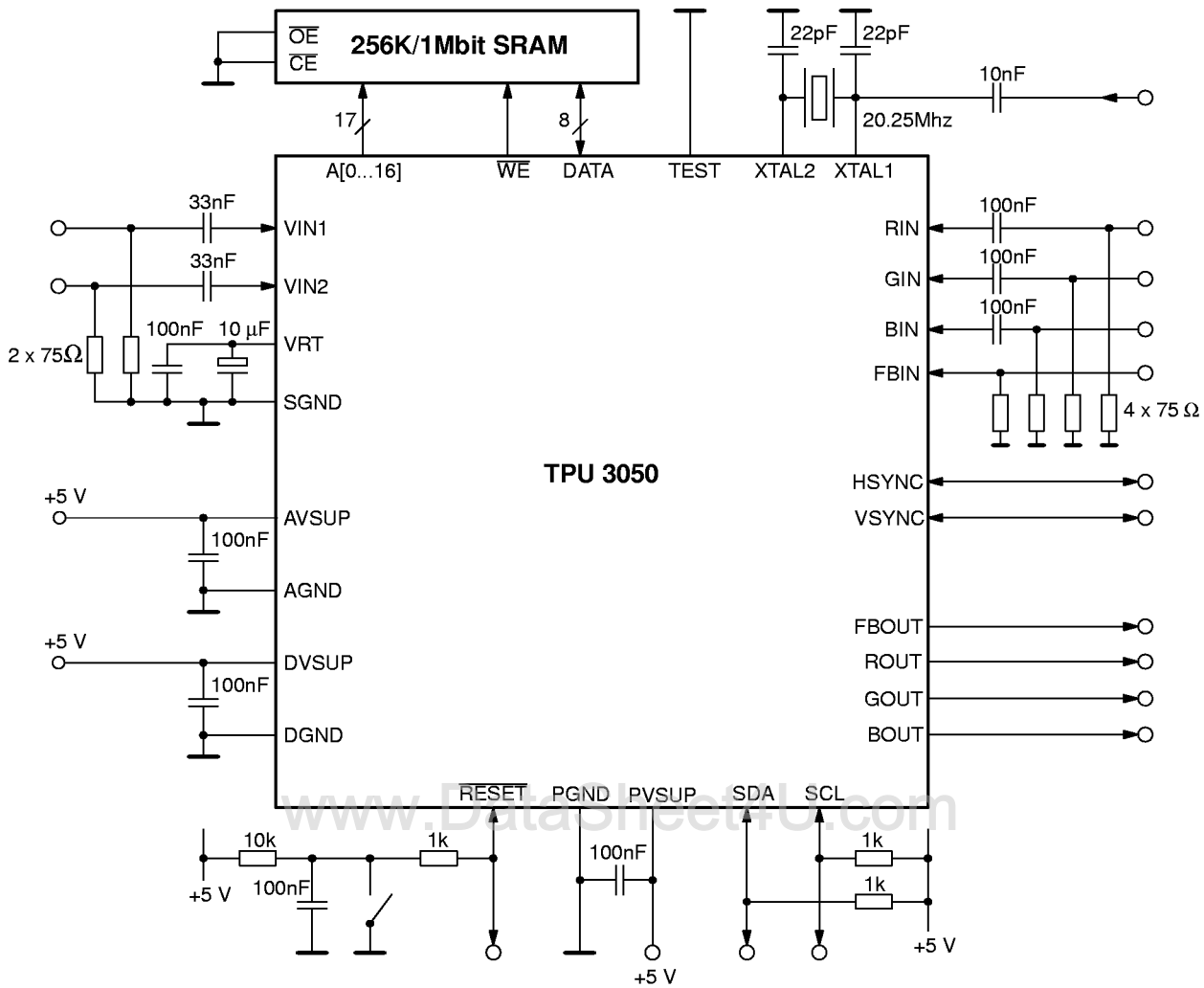


Fig. 5–2: TPU 3050 Application with SRAM

6. Glossary of Abbreviations

AIT	Additional Information Table
BTT	Basic TOP Table
BTTL	Basic TOP Table List
CEPT	Conférence Européene des Administrations des Postes et Télécommunication
CLUT	Color Look Up Table
CPU	Central Processing Unit
CRI	Clock Runin
DRAM	Dynamic Random Access Memory
DRCS	Dynamically Redefinable Character Set
FLOF	Full Level One Features
FRC	Framing Code
MAC	Multiplexed Analogue Components
MPT	Multipage Table
MPET	Multipage Extension Table
OSD	On Screen Display
PDC	Programme Delivery Control
PLT	Page Linking Table
RAM	Random Access Memory
ROM	Read Only Memory
SRAM	Static Random Access Memory
TOP	Table Of Pages
TPU	Teletext Processing Unit
TTX	Teletext
VBI	Vertical Blanking Interval
VPS	Video-Programm-System
WSS	Wide Screen Signalling
WST	World System Teletext

7. References

1) “World System Teletext and Data Broadcasting System”. Technical Specification. February 1990.

2) “Teletext Specification”. Interim Technical Document SPB 492. European Broadcasting Union. December 1992.

3) “8R2 Video-Programm-System (VPS)”. Technische Richtlinie ARD/ZDF.

4) “8R4 Fernsehtext-Spezifikation”. Technische Richtlinie ARD/ZDF.

5) “8R5 TOP-Verfahren für Fernsehtext”. Technische Richtlinie ARD/ZDF.

6) “Specification of the domestic video Programme Delivery Control system (PDC)”. European Broadcasting Union. August 1990.

7) “Television systems; 625-Line television Wide Screen Signalling (WSS)”. ETSI. November 1993.

8) “Television Captioning for the Deaf”. Signal and Display Specifications. May 1980.