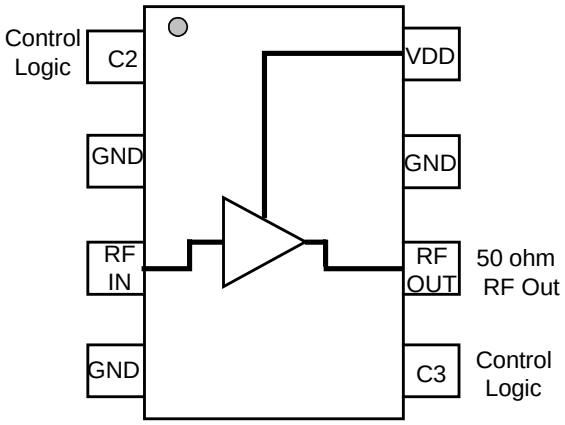
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ3131

DATA SHEET

3V Cellular Band CDMA/AMPS LNA IC



Features

- *Small size: SOT23-8*
- *Single 3V operation*
- *Low-current operation*
- *Gain Select*
- *Mode Select*
- *High IP3 performance*
- *Few external components*

Applications

- *IS-95 CDMA Mobile Phones*
- *AMPS Mobile Phones*
- *Dual Mode CDMA Cellular applications*
- *832-870MHz CDMA applications*

Product Description

The TQ3131 is a 3V, RF LNA IC designed specifically for Cellular band CDMA/AMPS applications. It's RF performance meets the requirements of products designed to the IS-95 and AMPS standards. The TQ3131 is designed to be used with the TQ5131 (CDMA/AMPS mixer) which provides a complete CDMA receiver for 800MHz dual-mode phones.

The LNA incorporates on-chip switches which determine CDMA, AMPS, and bypass mode select. When used with the TQ5131 (CDMA RFA/mixer), four gain states are available. The RF output port is internally matched to 50 Ω, greatly simplifying the design and keeping the number of external components to a minimum. The TQ3131 achieves good RF performance with low current consumption, supporting long standby times in portable applications. Coupled with the very small SOT23-8 package, the part is ideally suited for Cellular band mobile phones.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Frequency	832		894	MHz
Gain		13.0		dB
Noise Figure		1.4		dB
Input 3rd Order Intercept		10.0		dBm
DC supply Current		10.5		mA

Note 1: Test Conditions: Vdd=2.8V, Tc=25C, RF frequency=881MHz, CDMA High Gain state.

Electrical Characteristics

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency		832	881	894	MHz
CDMA Mode-High Gain					
Gain		11.5	13.0		dB
Noise Figure			1.4	2.0	dB
Input IP3		8.0	10.0		dBm
LNA IN Return Loss (with external matching)		10			dB
LNA OUT Return Loss		10			dB
Supply Current			10.5	13.5	mA
Bypass Mode					
Gain		-3.0	-2.0		dB
Noise Figure			2.0	3.0	dB
Input IP3		18.0	30.0		dBm
LNA IN Return Loss (with external matching)		10			dB
LNA OUT Return Loss		10			dB
Supply Current			1.2	2.5	mA
AMPS Mode					
Gain		8.5	11.0		dB
Noise Figure			1.6	2.2	dB
Input IP3		2.0	3.0		dBm
LNA IN Return Loss (with external matching)		10			dB
LNA OUT Return Loss		10			dB
Supply Current			4.0	5.5	mA
Supply Voltage		2.7	2.8	3.3	V

Note 1: Test Conditions: Vdd=2.8V, RF=881MHz, T_C = 25° C, unless otherwise specified.

Note 2: Min/Max limits are at +25°C case temperature, unless otherwise specified.

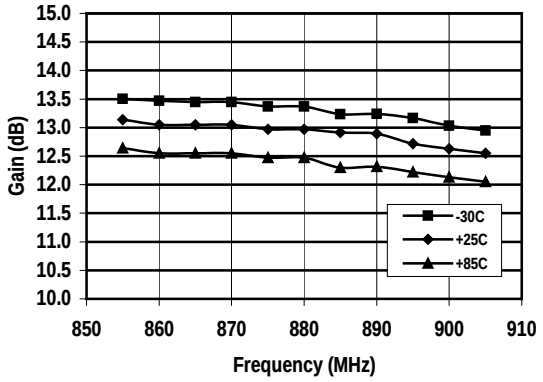
Absolute Maximum Ratings

Parameter	Value	Units
DC Power Supply	5.0	V
Power Dissipation	500	mW
Operating Temperature	-40 to 85	C
Storage Temperature	-60 to 150	C
Signal level on inputs/outputs	+20	dBm
Voltage to any non supply pin	+0.3	V

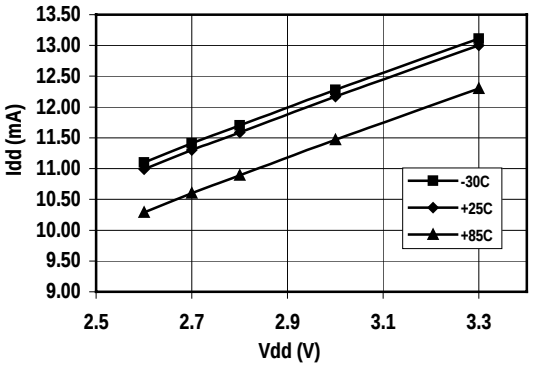
Typical Performance

Test Conditions, unless Otherwise Specified: Vdd=2.8V, Tc=+25C, RF=881MHz

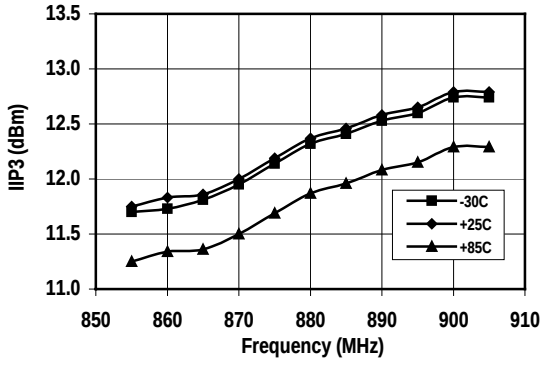
CDMA High Gain Mode
Gain v Freq v Temp



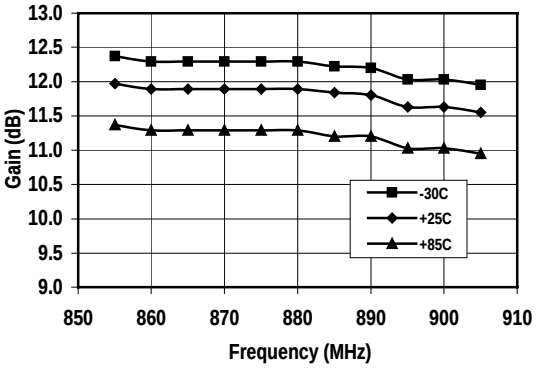
CDMA High Gain Mode
Idd v Vdd v Temp



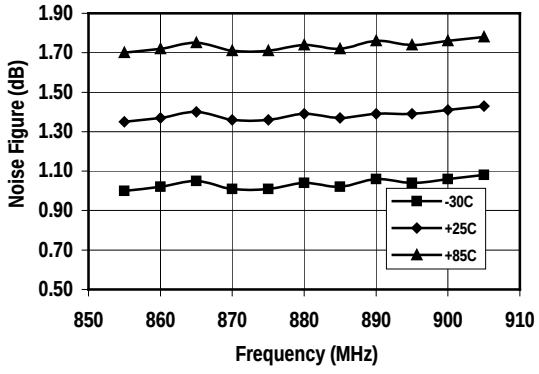
CDMA High Gain Mode
IIP3 v Freq v Temp



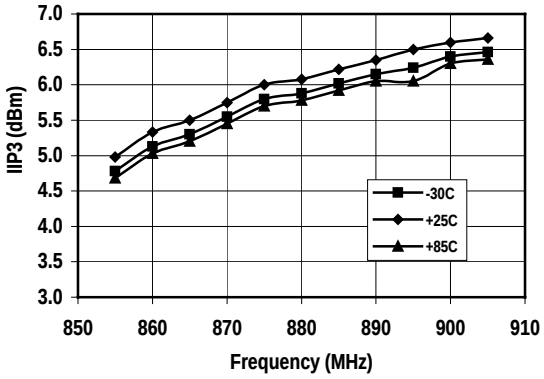
AMPS Mode
Gain v Freq v Temp



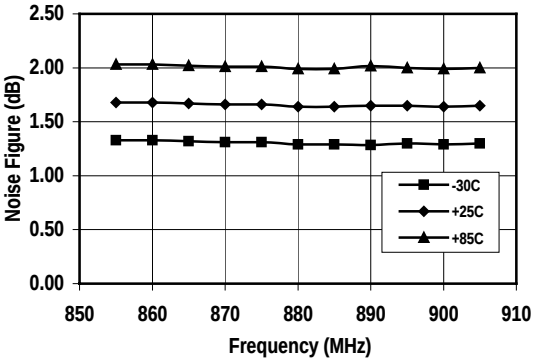
CDMA High Gain Mode
Noise Figure v Freq v Temp



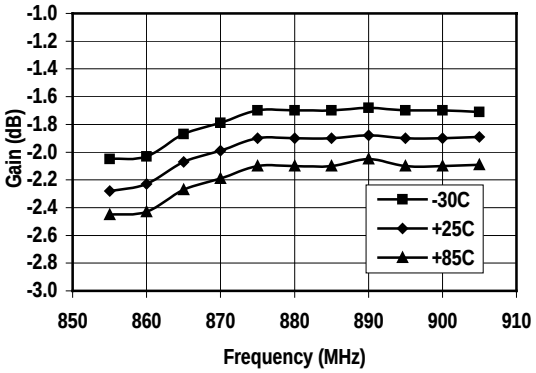
AMPS Mode
IIP3 v Freq v Temp



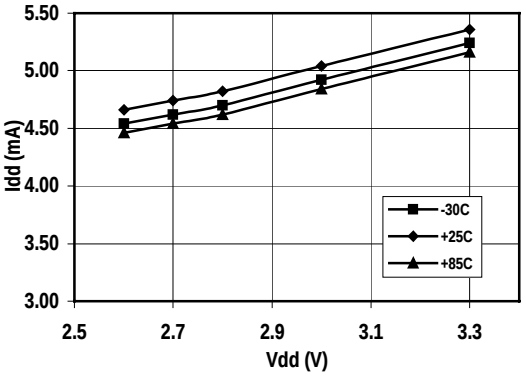
AMPS Mode
Noise Figure v Freq v Temp



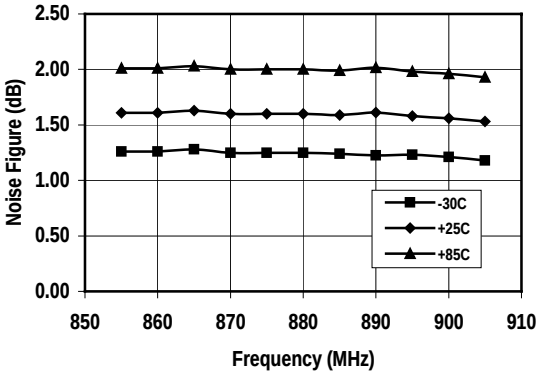
BYPASS Mode
Gain v Freq v Temp



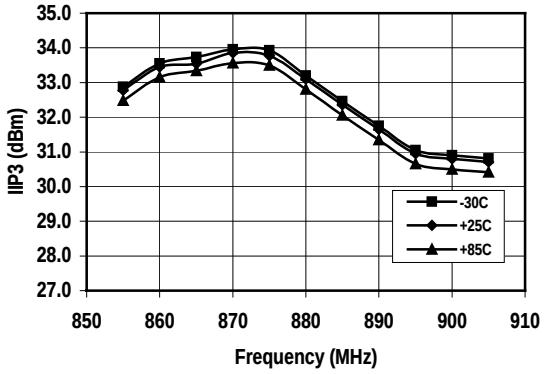
AMPS Mode
Idd v Vdd v Temp



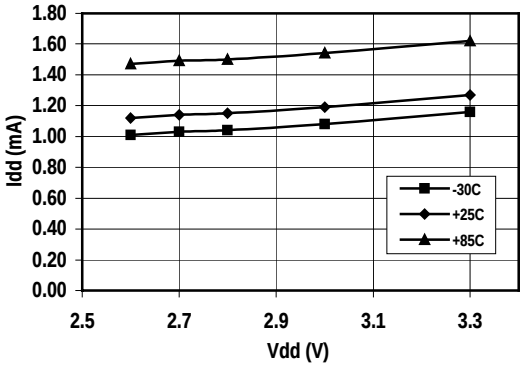
BYPASS Mode
Noise Figure v Freq v Temp



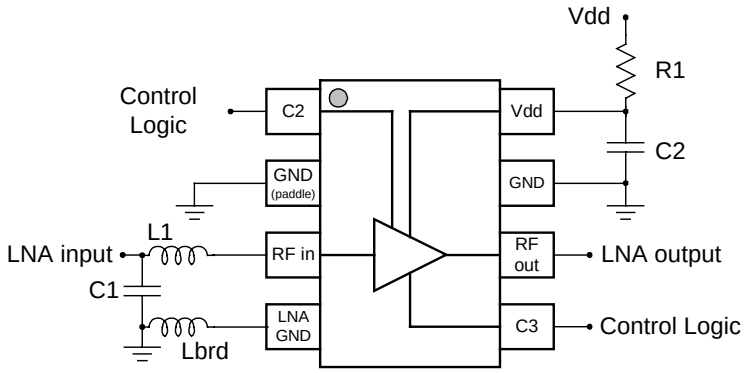
BYPASS Mode
IIP3 v Freq v Temp



BYPASS Mode
Idd v Vdd v Temp



Application/Test Circuit



Bill of Material for TQ3131 LNA Application/Test Circuit

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC	U1	TQ3131		SOT23-8	TriQuint Semiconductor
Capacitor	C1		3.3pFd	0402	
Capacitor	C2		8.2pF	0402	
Resistor	R1		3.3Ω	0402	
Inductor	L1		15nH	0402	
Inductor	Lbrd		See application note		

TQ3131 Product Description

The TQ3131 LNA uses a cascode low noise amplifier, along with signal path switching. A bias control circuit sets the quiescent current for each mode and ensures peak performance over process and temperature, (refer to Figure 1). In the application, CMOS level signals are applied to pins 1 and 5 and are decoded by internal logic in order to set the device to the desired mode. (see Table 1 for logic control states)

In the high gain mode, switches S1, S2, and S5 are closed, with switches S3 and S4 open. In the bypass mode, switches S1, S2, and S5 are open, with switches S3 and S4 closed. Having five switches ensures that there are no parasitic feedback paths for the signal. In the AMPS mode, control logic switches the LNA into a low current bias condition.

Only three external components are needed in an application. The chip uses an external cap and inductor for the input match to pin 3. The output is internally matched to 50 ohms at pin 6. A Vdd bypass cap is required close to pin 8.

External degeneration of the cascode is required between pin 4 and ground. However, a small amount of pc board trace can be used as the inductor (Lbrd). Alternatively, if an extra component can be tolerated, a small value chip inductor can be used. (see Figure 2)

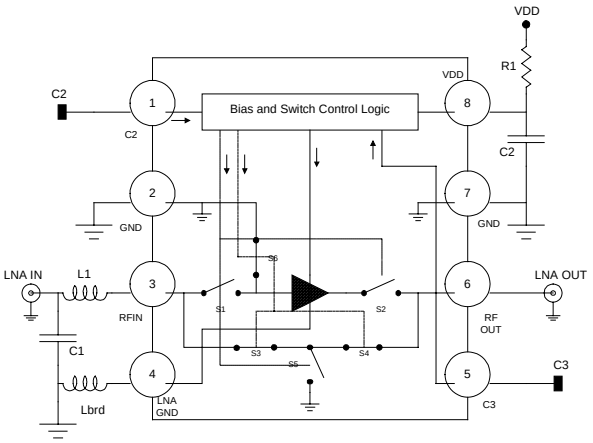


Figure 1 TQ3131 Simplified Schematic

Operation

MODE	C2	C3	Typical Gain
High Gain	0 1	0 0	13(dB)
AMPS	0	1	11(dB)
Bypass	1	1	-2(dB)

Table 1 LNA States and Control Bits

LNA Input Network Design

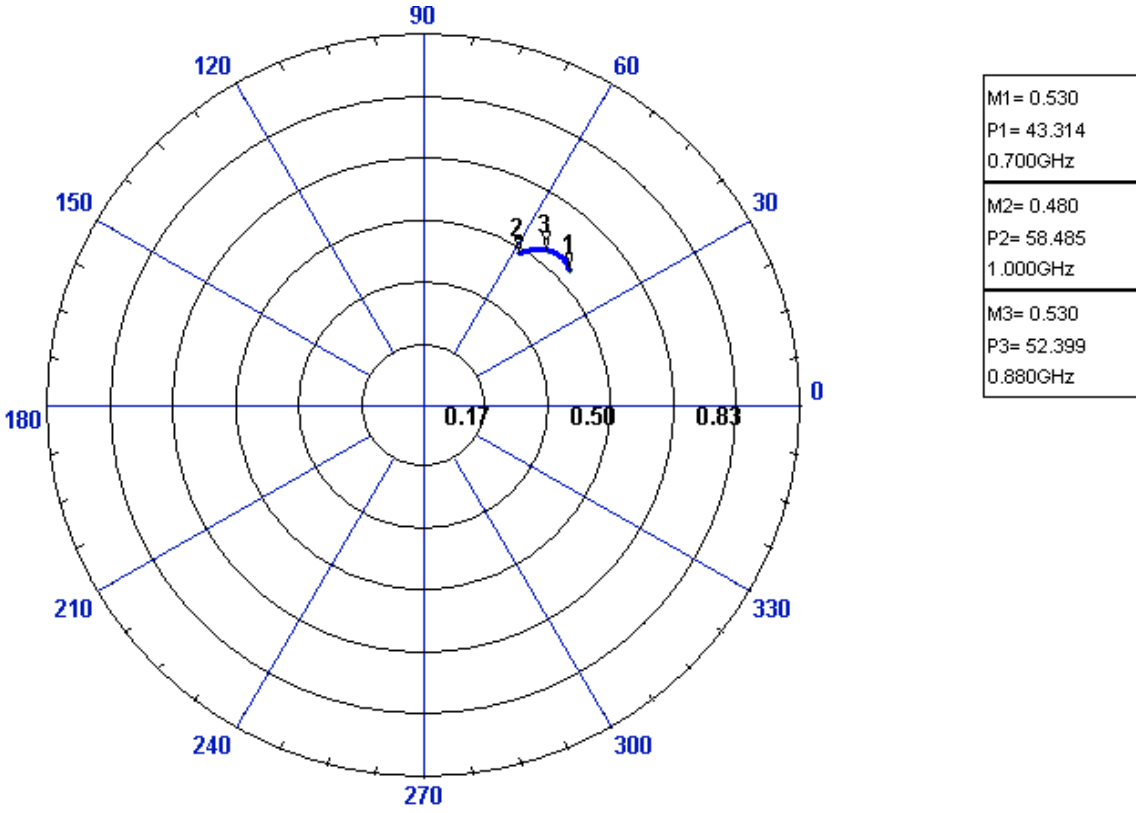
Input network design for most LNA's is a straightforward compromise between noise figure and gain. The TQ3131 is no exception, even though it has 3 different modes. The device was designed so that one only needs to optimize the input match in the high gain mode. As long as the proper grounding and source inductance are used, the other two modes will perform well with the same match.

It is probably wise to synthesize the matching network component values for some intermediate range of Gamma values, and then by experimentation, find the one which provides the best compromise between noise figure and gain. The quality of the chip ground will have some effect on the match, which is why some experimentation will likely be needed. The input match will affect the output match to some degree, so S22 should be monitored.

The values used on our evaluation board may be used as a starting point.

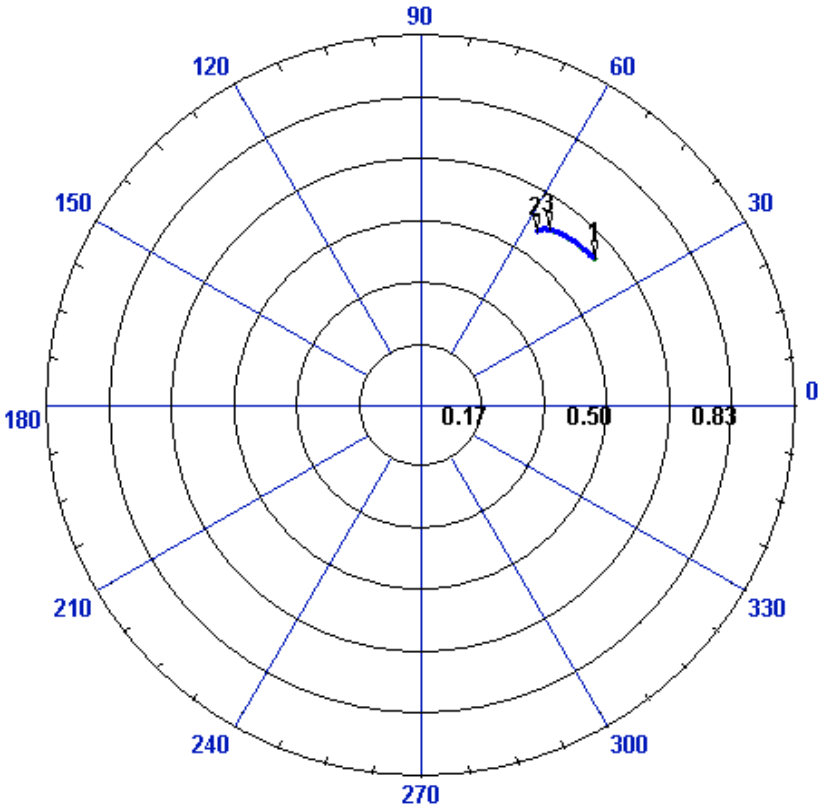
Noise Parameter Analysis

A noise parameter analysis is shown on the next page for both the high gain and AMPS modes. A "nominal" device was mounted directly on a solid copper ground plane with semi-rigid probes attached to the device input and output pins. A value of Lbrd was chosen so that 13.0dB of gain was attained at conjugate match. Then the tuner was removed and noise data was taken. Please note that although data was taken at 700MHz and 1000MHz, the device was designed to operate satisfactorily only over a much more limited range.



Gamma Opt analysis for TQ3131 High Gain Mode

Freq (MHz)	Γ Opt	Γ Angle	Fmin (dB)	R noise
700	0.53	43.3	0.90	18.5
880	0.53	52.4	0.92	16.5
1000	0.48	58.5	1.01	15.4



M1= 0.610
P1= 40.601
0.700GHz

M2= 0.560
P2= 56.602
1.000GHz

M3= 0.586
P3= 54.223
0.880GHz

Gamma Opt analysis for TQ3131 Amps Mode

Freq (MHz)	Γ Opt	Γ Angle	Fmin (dB)	R noise
700	0.61	40.6	1.22	33.0
880	0.70	54.2	1.09	27.4
1000	0.56	56.6	1.42	27.0

Gain Control via Pin 4 Inductance

The source connection of the LNA cascode is brought out separately through pin 4. That allows the designer to make some range of gain adjustment. The total amount of inductance present at the source of the cascode is equal to the bond wire plus package plus external inductance. One should generally use an external inductance such that gain in the high gain CDMA mode = 13.0. Although it is possible to increase the gain of the TQ3131 by using little or no degeneration, input intercept will be degraded.

Figure 2 shows how a spiral pc board trace can be used as the external inductance. It is suggested that such a circuit be used for the initial design prototype. Then the optimum inductance can be found by simply solder bridging across the inductor. The final pc board design can then include the proper shorted version of the inductor.

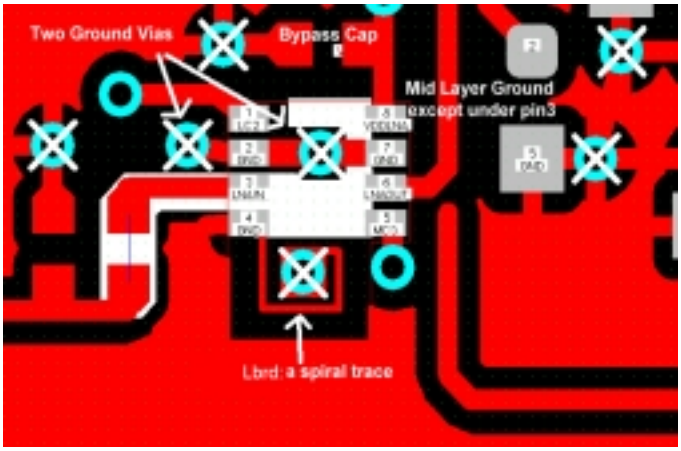


Figure 2 Showing Lbrd and Grounding on Evaluation Board

Selection of the Vdd Bypass Cap for Optimum Performance

The Vdd bypass capacitor has the largest effect on the LNA output match, and is required for proper operation. Because the input match affects the output match to some degree as well, the process of picking the bypass cap value involves some iteration. First, an input match is selected which gives adequate gain and noise figure. Then the bypass capacitor is varied to give the best output match. Generally, the poorer the chip grounding, the smaller the bypass capacitor value will be. The demo board achieves 11-12dB of return loss which is adequate for connection directly to the input of a SAW filter.

Grounding

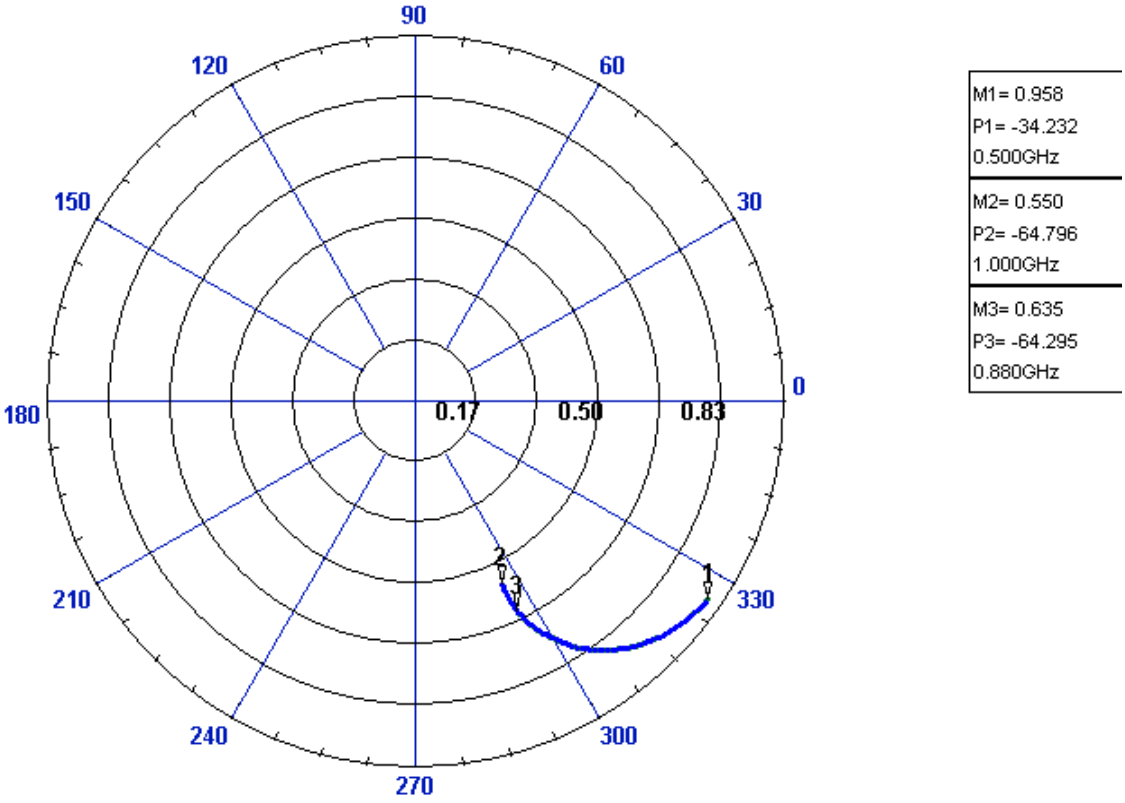
An optimal ground for the device is important in order to achieve datasheet specified performance.

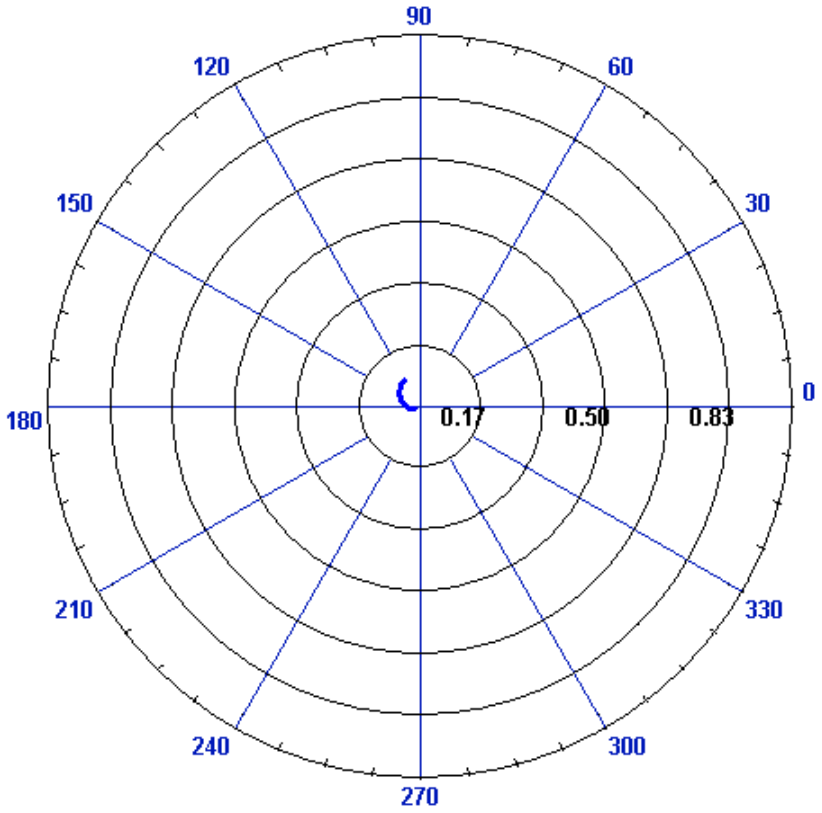
Symptoms of a poor ground include reduced gain and the inability to achieve >2:1 VSWR at the output when the input is matched. It is recommended to use multiple vias to a mid ground plane layer. The vias at pins 2 and 7 to this layer should be as close to the lead pads as possible Additionally, the ground return on the Vdd bypass cap should provide minimal inductance back to chip pins 2 and 7.

TQ3131 S-Parameters

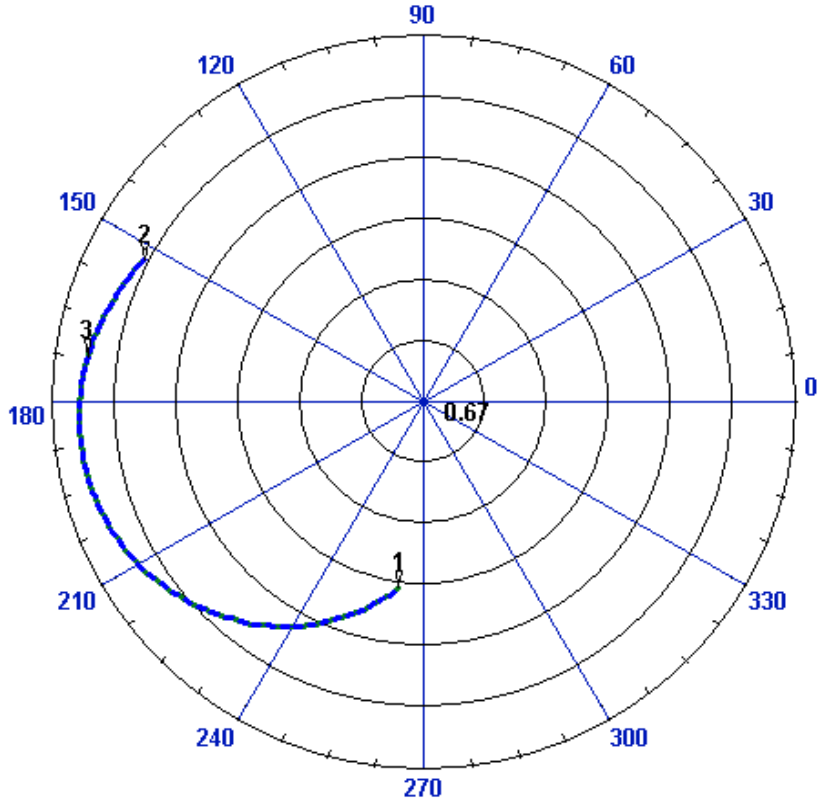
Following are S-Parameter graphs for both the high gain and the AMPS modes. Data was taken on a single "nominal" device at 2.8v Vdd. The reference planes were set at the end of the package pins. Note that the plots are almost identical for both modes.

TQ3131 High Gain Mode S-Parameters S11



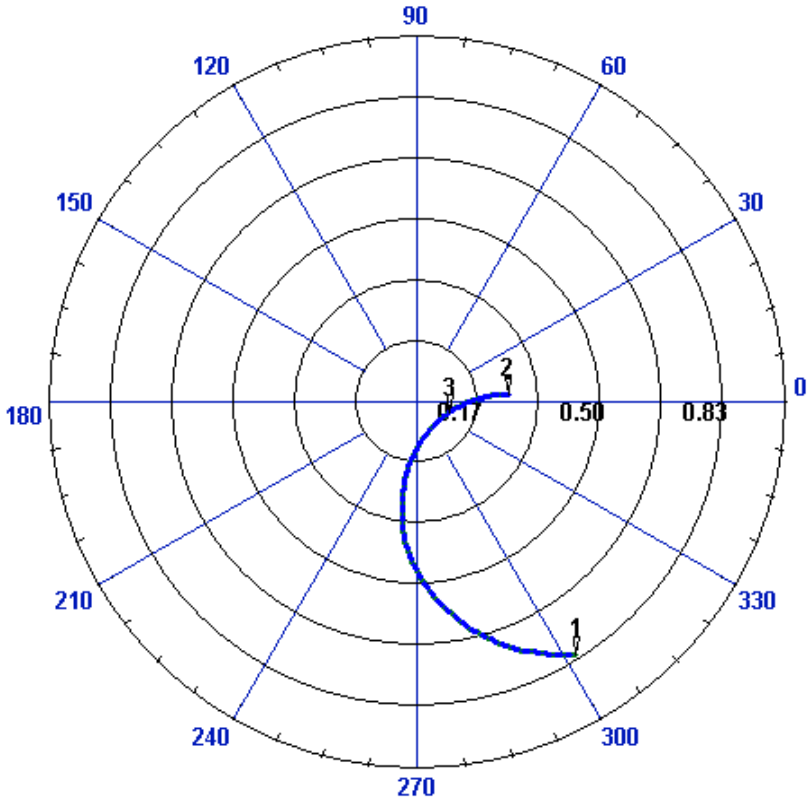


S12



M1 = 2.042	
P1 = -97.643	
0.500GHz	
M2= 3.368	
P2= 152.711	
1.000GHz	
M3= 3.641	
P3= 172.179	
0.880GHz	

S21



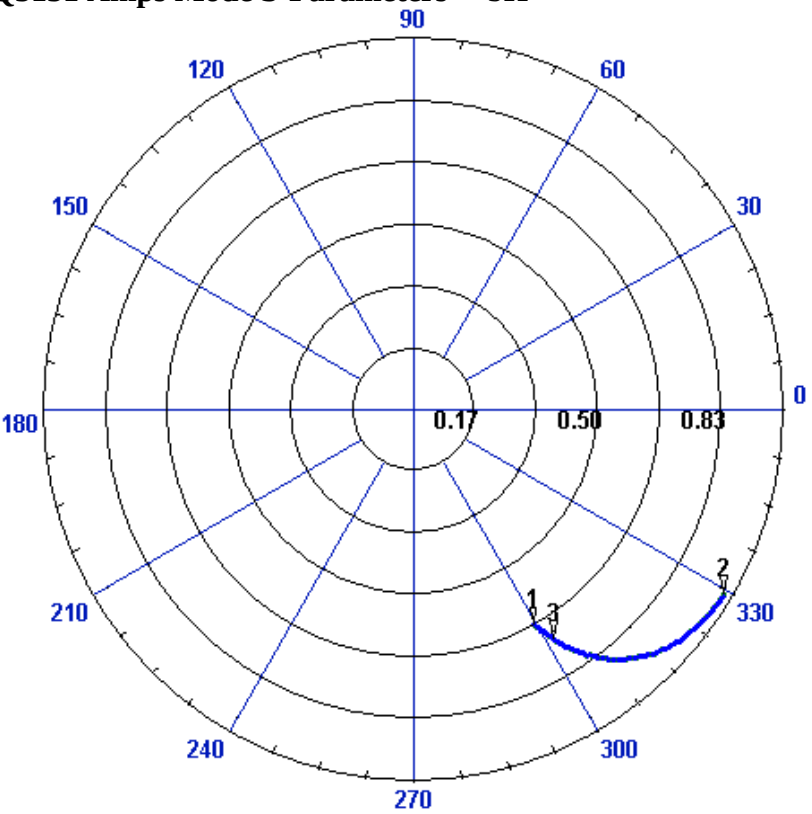
M1= 0.813
P1= -57.832
0.500GHz

M2= 0.249
P2= 4.574
1.000GHz

M3= 0.094
P3= -18.148
0.880GHz

S22

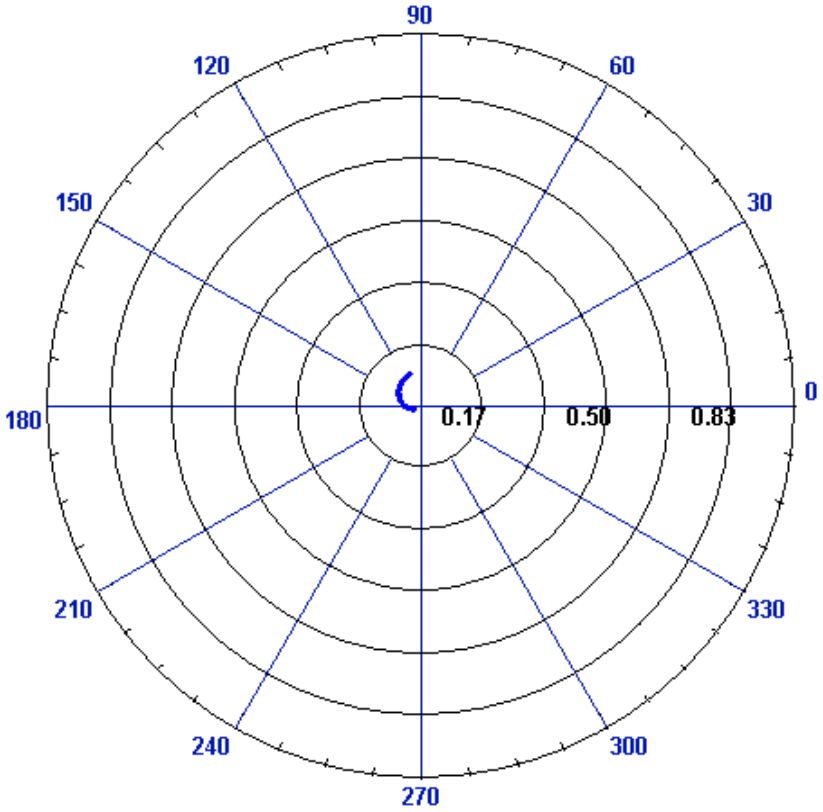
TQ3131 Amps Mode S-Parameters **S11**



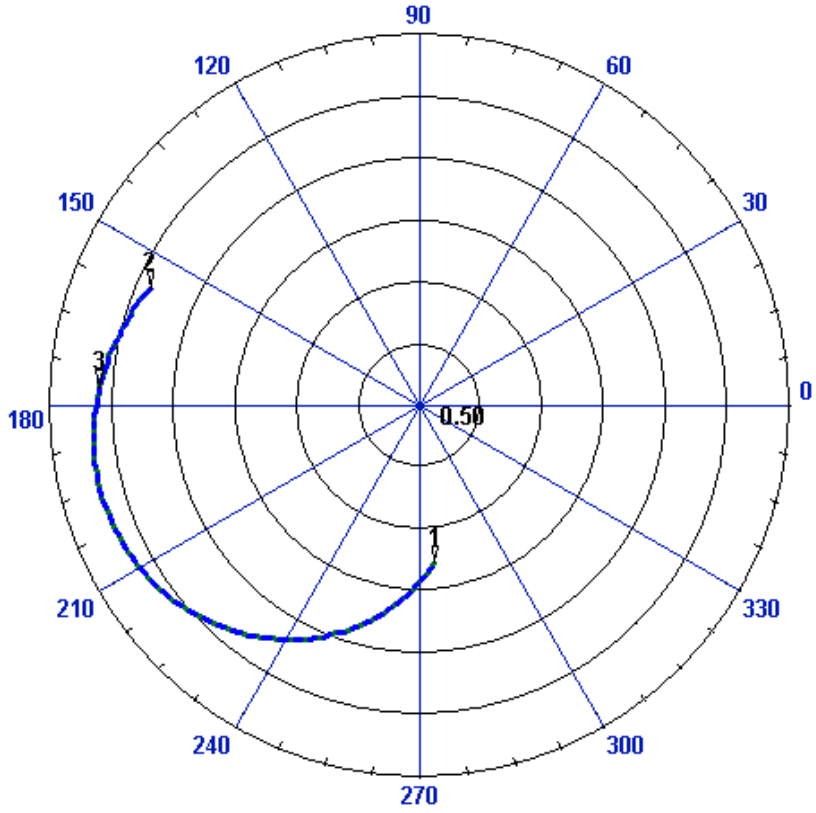
M1= 0.661
P1= -60.851
1.000GHz

M2= 0.971
P2= -30.548
0.500GHz

M3= 0.721
P3= -58.469
0.880GHz



S12

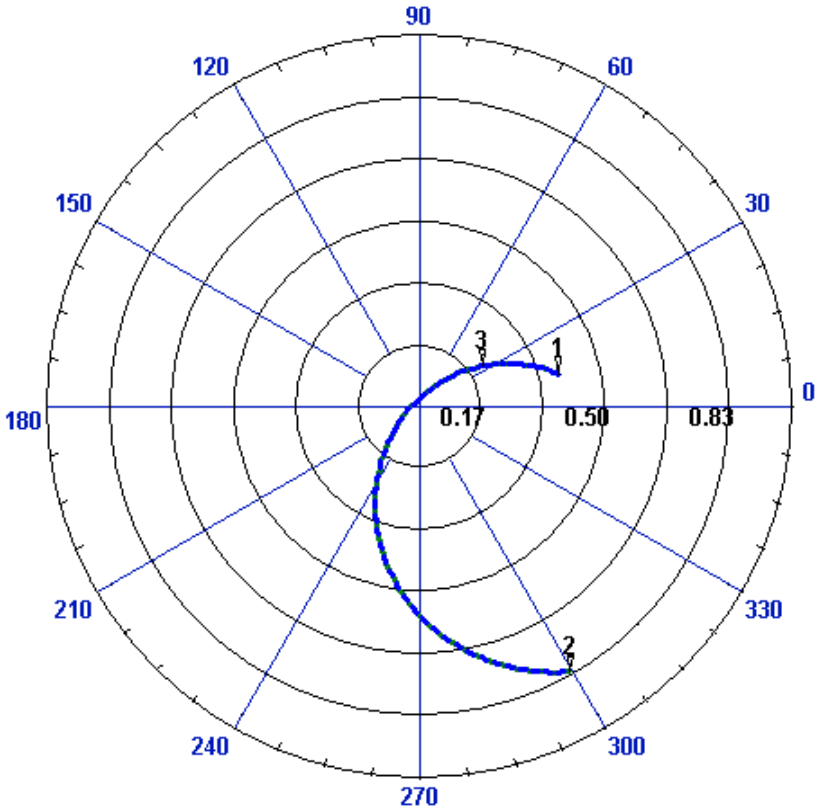


M1= 1.272
P1= -84.698
0.500GHz

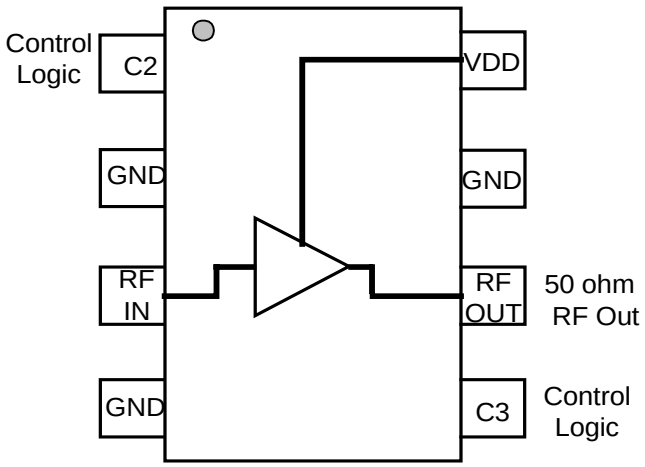
M2= 2.376
P2= 156.462
1.000GHz

M3= 2.599
P3= 176.662
0.880GHz

S21


90
120
60
150
30
180
0
210
330
240
300
270
0.17
0.50
0.83
1
2
3
M1= 0.381
P1= 13.304
1.000GHz
M2= 0.818
P2= -60.502
0.500GHz
M3= 0.200
P3= 33.418
0.880GHz

S22

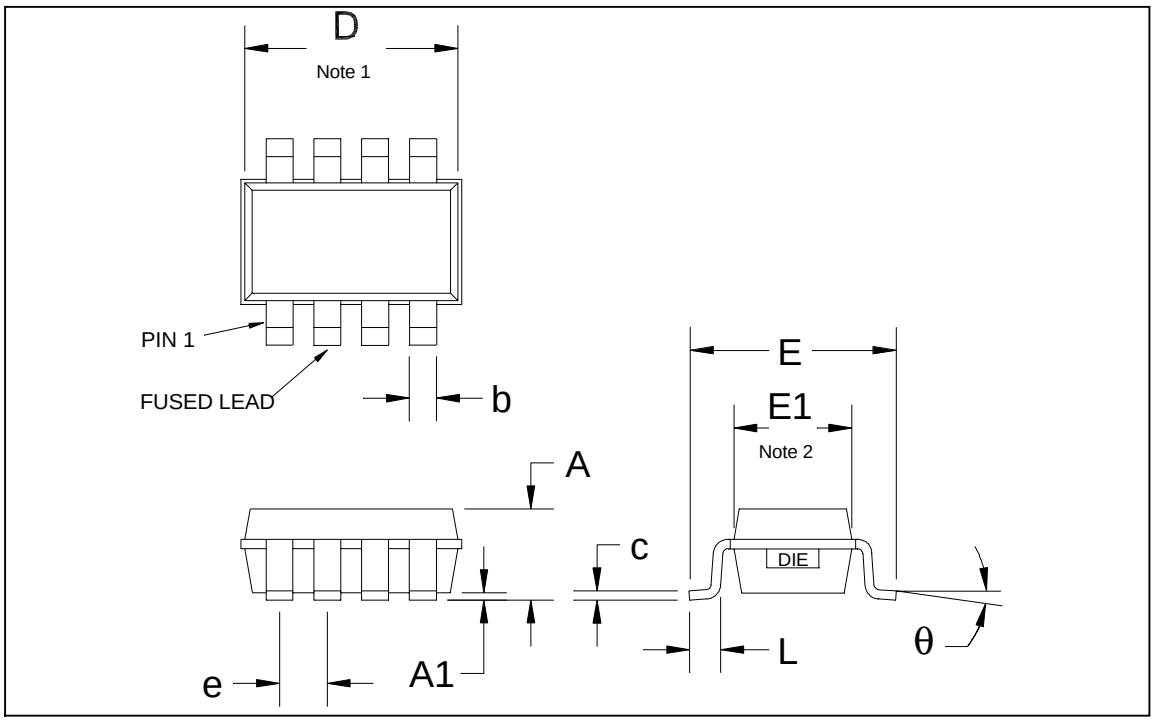


Package Pinout

Pin Descriptions

Pin Name	Pin #	Description and Usage
C2	1	Control logic 2
GND	2	Ground, paddle
RF IN	3	RF input, off-chip matching required
LNA GND	4	Ground
C3	5	Control logic 3
RF OUT	6	RF output, no matching required
LNA GND	7	Ground
Vdd	8	LNA Vdd, typical 2.8V, C2 capacitor required

Package Type: SOT23-8 Plastic Package



DESIGNATION	DESCRIPTION	METRIC		ENGLISH		NOTE
A	OVERALL HEIGHT	1.20	+/-.25 mm	0.05	+/-.250 in	3
A1	STANDOFF	.100	+/-.05 mm	.004	+/-.002 in	3
b	LEAD WIDTH	.365	mm TYP	.014	in	3
c	LEAD THICKNESS	.127	mm TYP	.005	in	3
D	PACKAGE LENGTH	2.90	+/-.10 mm	.114	+/-.004 in	1,3
e	LEAD PITCH	.65	mm TYP	.026	in	3
E	LEAD TIP SPAN	2.80	+/-.20 mm	.110	+/-.008 in	3
E1	PACKAGE WIDTH	1.60	+/-.10 mm	.063	+/-.004 in	2,3
L	FOOT LENGTH	.45	+/-.10 mm	.018	+/-.004 in	3
Theta	FOOT ANGLE	1.5	+/-1.5 DEG	1.5	+/-1.5 DEG	

Notes
1. The package length dimension includes allowance for mold mismatch and flashing.
2. The package width dimension includes allowance for mold mismatch and flashing.
3. Primary dimensions are in metric millimeters. The English equivalents are calculated and subject to rounding error.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Revision A, January, 2000