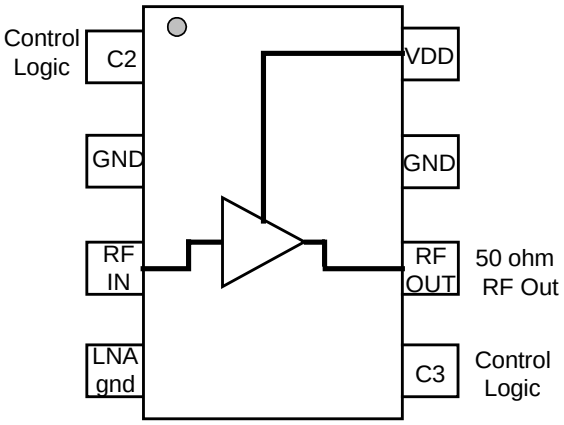
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ3632

DATA SHEET

Low Current, 3V PCS Band CDMA LNA IC



Features

- *Small size: SOT23-8*
- *Single 3V operation*
- *Low-current operation*
- *Gain Select*
- *High IP3 performance*
- *Few external components*

Applications

- *IS-95 CDMA PCS Mobile Phones*

Product Description

The TQ3632 is a low current, 3V, RF LNA IC designed specifically for PCS band CDMA applications. It's RF performance meets the requirements of products designed to the IS-95 specifications. The TQ3632 is designed to be used with the TQ5631 or TQ5633 (CDMA mixer) which provides a complete CDMA receiver for 1900MHz phones.

The LNA incorporates on-chip switches which determine high, low and bypass mode select. When used with the TQ5631 or TQ5633 (CDMA RFA/mixer), four gain steps are available for use which provide low current/high IP3 and gain. The RF output port is internally matched to 50 Ω, greatly simplifying the design and minimizing the number of external components. The TQ3632 achieves excellent RF performance with low current consumption, supporting long standby and talk times in portable applications. Coupled with the very small SOT23-8 package, the part is ideally suited for PCS band mobile phones.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Frequency		1960		MHz
Gain		12.5		dB
Noise Figure		1.5		dB
Input 3rd Order Intercept		7.0		dBm
DC supply Current		7.5		mA

Note 1: Test Conditions: Vdd=2.8V, RF=1960MHz, Tc=25C, CDMA High Gain state.

Electrical Characteristics

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency	PCS band	1810	1960	1990	MHz
CDMA Mode-High Gain					
Gain		10.5	12.5		dB
Noise Figure			1.5	1.9	dB
Input IP3		5.0	7.0		dBm
Input Return Loss (with external matching)		10			dB
Output Return Loss		10			dB
Supply Current			7.5	9.5	mA
CDMA Mode-High Gain-Low Linearity					
Gain		8.5	11.0		dB
Noise Figure			1.8		dB
Input IP3		2.0	4.0		dBm
Input Return Loss (with external matching)		10			dB
Output Return Loss		10			dB
Supply Current			4.5	6.5	mA
Bypass Mode					
Gain		-3.0	-2.0	-1.0	dB
Noise Figure			2.0	3.0	dB
Input IP3		20.0	25.0		dBm
Input Return Loss (with external matching)		10			dB
Output Return Loss		10			dB
Supply Current			1.0	2.5	mA
Supply Voltage		2.7	2.8	3.3	V

Note 1: Test Conditions: Vdd=2.8V, RF=1960MHz, T_C = 25 °C, unless otherwise specified.

Note 2: Min/Max limits are at +25°C case temperature, unless otherwise specified.

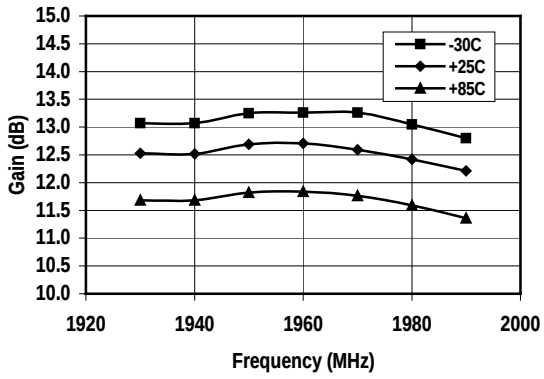
Absolute Maximum Ratings

Parameter	Value	Units
DC Power Supply	5.0	V
Power Dissipation	500	mW
Operating Temperature	-40 to 85	C
Storage Temperature	-60 to 150	C
Signal level on inputs/outputs	+20	dBm
Voltage to any non supply pin	+0.3	V

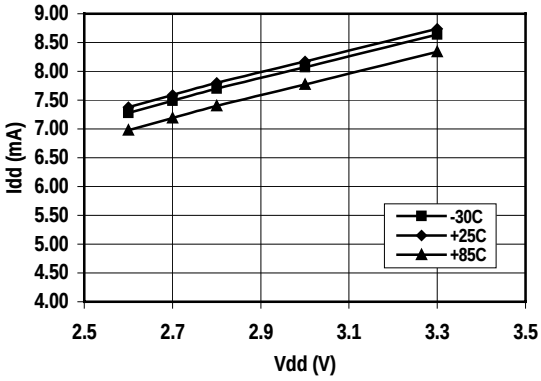
Typical Performance

Test Conditions, unless Otherwise Specified: Vdd=2.8V, Tc=25C, RF=1960MHz

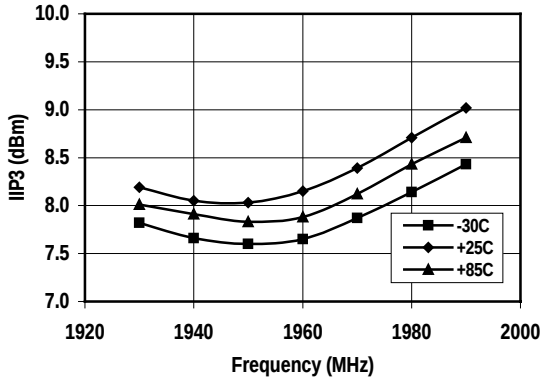
CDMA High Gain Mode
Gain v Freq v Temp



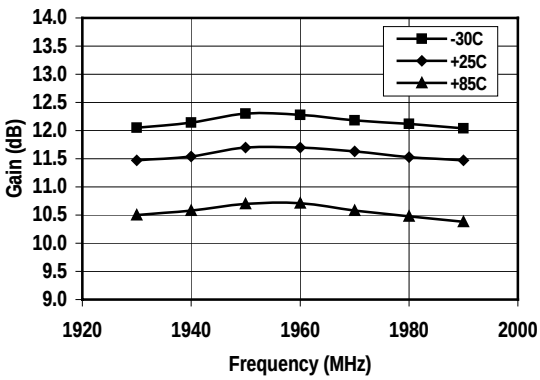
CDMA High Gain Mode
Idd v Vdd v Temp



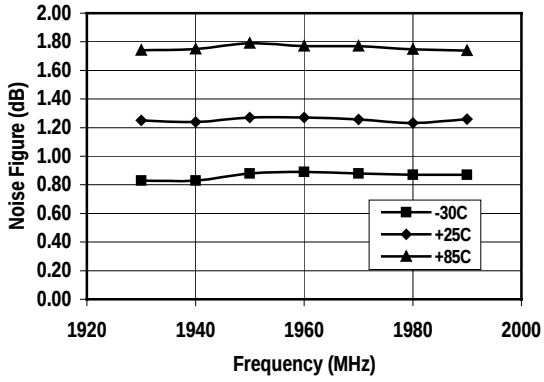
CDMA High Gain Mode
IIP3 v Freq v Temp



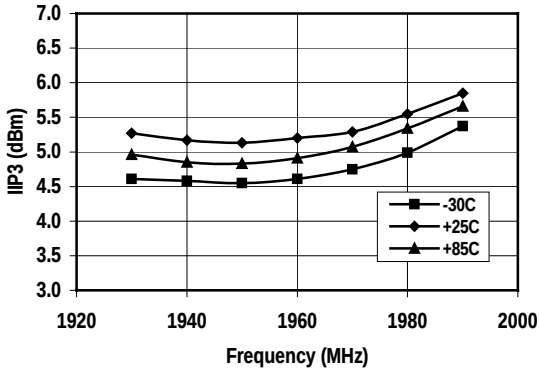
High Gain/Low Linearity Mode
Gain v Freq v Temp



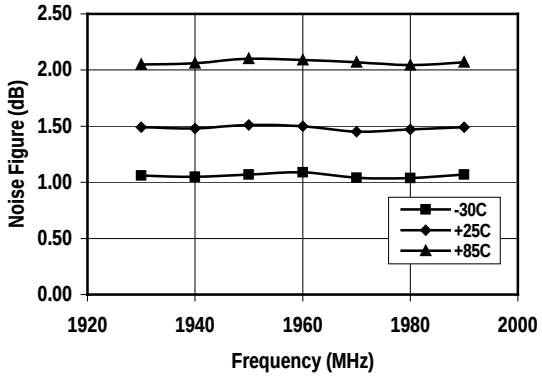
CDMA High Gain Mode
Noise Figure v Freq v Temp



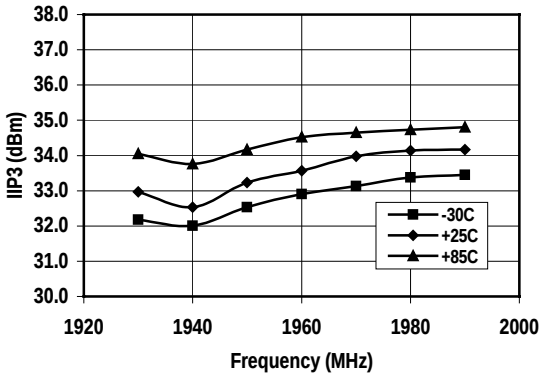
High Gain/Low Linearity Mode
IIP3 v Freq v Temp



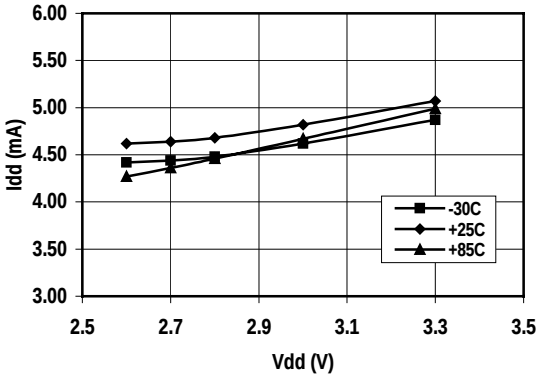
High Gain/Low Linearity Mode
Noise Figure v Freq v Temp



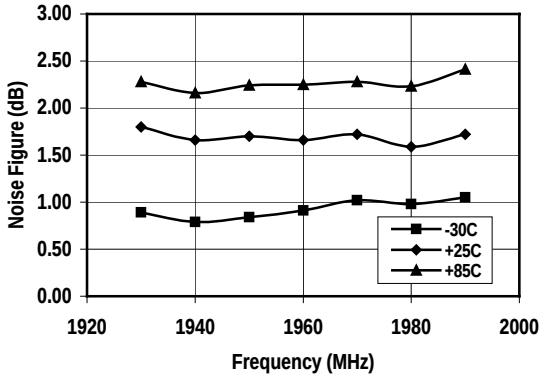
BYPASS Mode
IIP3 v Freq v Temp



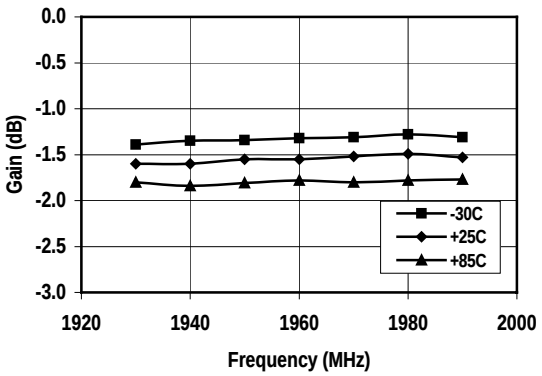
High Gain/Low Linearity Mode
Idd v Vdd v Temp



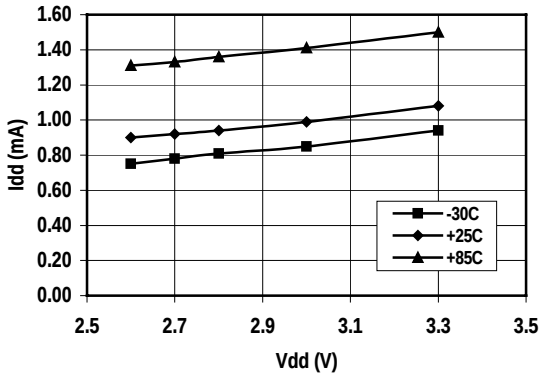
BYPASS Mode
Noise Figure v Freq v Temp



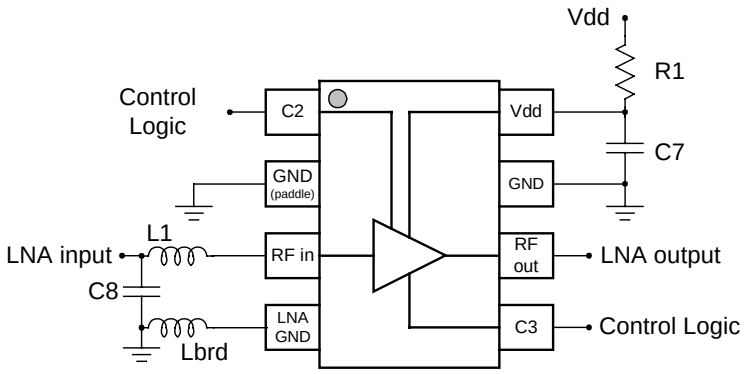
BYPASS Mode
Gain v Freq v Temp



BYPASS Mode
Idd v Vdd v Temp



Application/Test Circuit



Bill of Material for TQ3632 LNA Application/Test Circuit

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC	U1	TQ3631		SOT23-8	TriQuint Semiconductor
Capacitor	C7		4.7pF	0402	
Capacitor	C8		1.5pF	0402	
Resistor	R1		3.3Ω	0402	
Inductor	L1		4.7nH	0402	Panasonic
Inductor	Lbrd		See application note		

TQ3632 Product Description

The TQ3632 LNA uses a cascode low noise amplifier along with signal path switching. A bias control circuit sets the quiescent current for each mode and ensures peak performance over process and temperature, see Figure 1. In the application, CMOS level signals are applied to pins 1 and 5 and are decoded by an internal logic circuit, this sets the device to the desired mode. See Table 1 for truth table.

In the high gain mode, switches S1, S2, and S5 are closed, with switches S3 and S4 open. In the bypass mode, switches S1, S2, and S5 are open, with switches S3 and S4 closed. Six internal switches ensures there are no parasitic feedback paths for the RF signal. In the AMPS mode, control logic switches the LNA into a low current bias condition.

Only three external components are needed. The chip uses an external cap and inductor for the input match to pin 3. The output is internally matched to 50 ohms at pin 6. A Vdd bypass cap is required close to pin 8.

External degeneration of the cascode is required between pin 4 and ground. However, a small amount of PC board trace can be used as the inductor. Alternatively, if an extra component can be tolerated, a small value chip inductor could be used. See Figure 2.

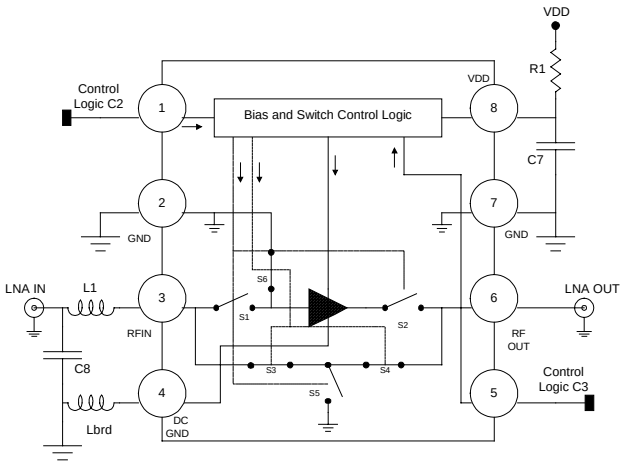


Figure 1 TQ3632 Simplified Schematic

Operation

MODE	C2	C3	Typical Gain
High Gain	0 1	0 0	13(dB)
High Gain Low linearity	0	1	11(dB)
Bypass	1	1	-2(dB)

Table 1 LNA States and Control Bits

LNA Input Network Design

Input network design for most LNA's is a straightforward compromise between noise figure and gain. The TQ3632 is no exception, even though it has 3 different modes. The device was designed so that one only needs to optimize the input match in the high gain mode. As long as the proper grounding and source inductance are used, the other two modes will perform well with the same match.

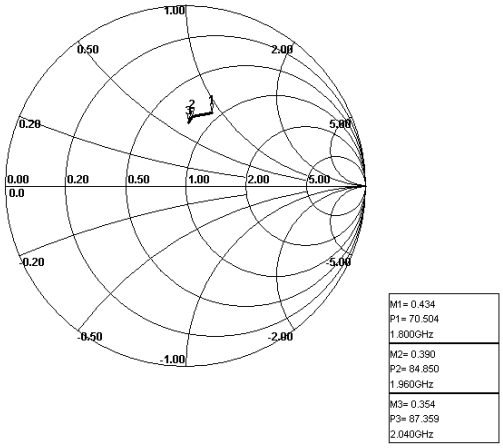
It is probably wise to synthesize the matching network component values for some intermediate range of Gamma values, and then by experimentation, find the one which provides the best compromise between noise figure and gain. The quality of the chip ground will have some effect on the match, which is why some experimentation will likely be needed. The input match will affect the output match to some degree, so S22 should be monitored.

The values used on our evaluation board may be used as a starting point.

Noise Parameter Analysis

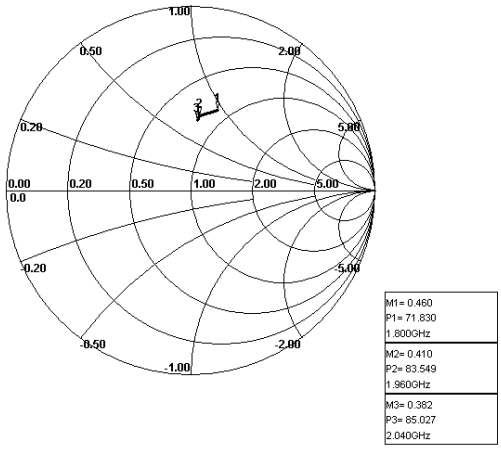
A noise parameter analysis is shown on the next page for the high gain and high gain low linearity modes. A "nominal" device was mounted directly on a standard evaluation board without a matching network (thru connected). The input reference plane was set at pin 3 and board loss was included in the calculations. C7 was set to 4.7pF.

Gamma Opt analysis for TQ3632 High Gain Mode



Freq. (MHz)	Γ Opt	Γ Angle	Fmin (dB)	R noise
1800	0.454	70.5	1.534	29.27
1960	0.390	84.8	1.209	18.47
2040	0.354	87.3	1.369	16.94

Gamma Opt analysis for TQ3632 High Gain Low Linearity Mode



Freq. (MHz)	Γ Opt	Γ Angle	Fmin (dB)	R noise
1800	0.454	70.5	1.534	29.27
1960	0.390	84.8	1.209	18.47
2040	0.354	87.3	1.369	16.94

Gain Control via Pin 4 Inductance

The source connection of the LNA cascode is brought out separately through pin 4. That allows the designer to make some range of gain adjustment. The total amount of inductance present at the source of the cascode is equal to the bond wire plus package plus external inductance. One should generally use an external inductance such that gain in the high gain CDMA mode = 13.0dB. Although it is possible to increase the gain of the TQ3632 by using little or no degeneration, input intercept will be degraded.

Figure 2 shows how a spiral PC board trace can be used as the external inductance. It is suggested that such a circuit be used for the initial design prototype. Then the optimum inductance can be found by simply solder bridging across the inductor. The final PC board design can then include the proper shorted version of the inductor.

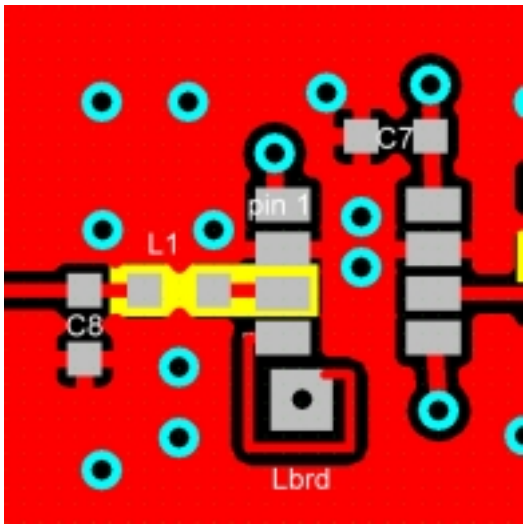


Figure 2 Showing Lbrd and Grounding on Evaluation Board

Selection of the Vdd Bypass Cap for Optimum Performance

The Vdd bypass capacitor has the largest effect on the LNA output match, and is required for proper operation. Because the input match affects the output match to some degree as well, the process of picking the bypass cap value involves some iteration. First, an input match is selected which gives adequate gain and noise figure. Then the bypass capacitor is varied to

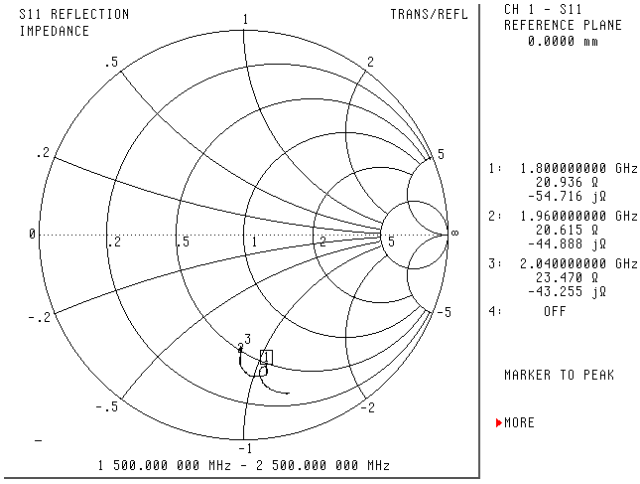
give the best output match. The demo board achieves 11-12dB of return loss which is adequate for connection directly to the input of a SAW filter.

Grounding

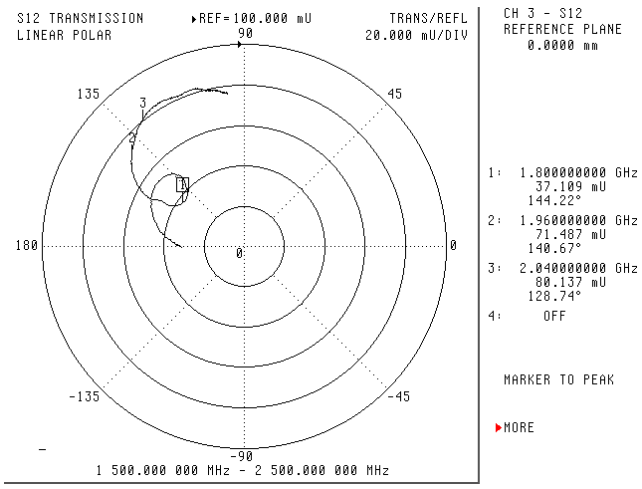
An optimal ground for the device is important in order to achieve datasheet specified performance. Symptoms of a poor ground include reduced gain and the inability to achieve <2:1 VSWR at the output when the input is matched. It is recommended to use multiple vias to a mid ground plane layer. The vias at pins 2 and 7 to this layer should be as close to the lead pads as possible Additionally, the ground return on the Vdd bypass cap should provide minimal inductance back to chip pins 2 and 7.

TQ3632 S-Parameters

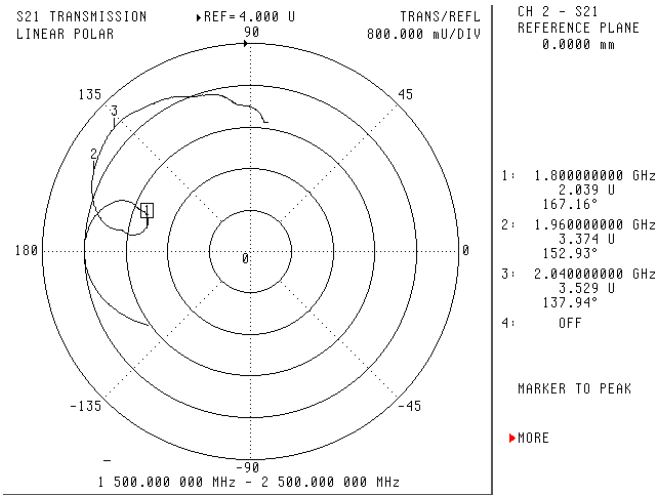
Following are S-Parameter graphs for the high gain and high gain low linearity modes. Data was taken on a single "nominal" device at 2.8v Vdd. The reference planes were set at the end of the package pins.



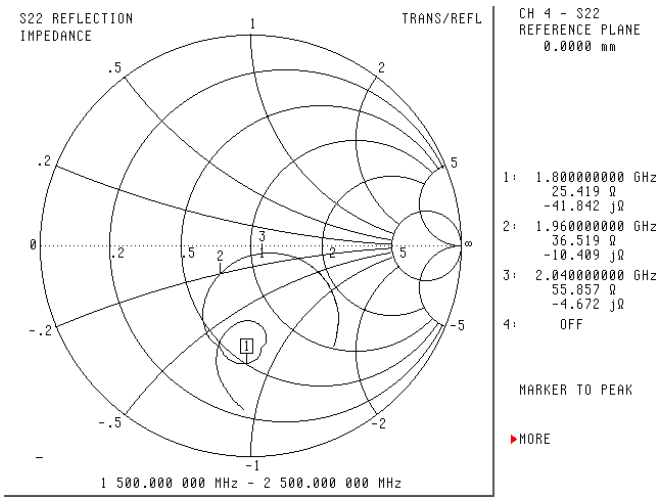
TQ3632 High Gain Mode S-Paremeters S11



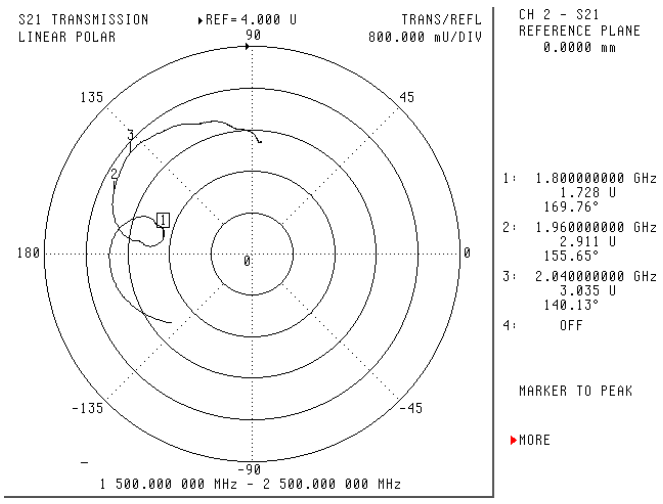
TQ3632 High Gain Mode S-Parameters S12



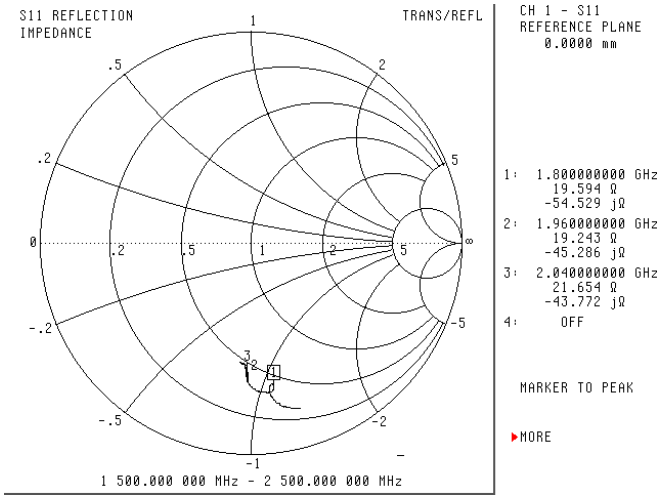
TQ3632 High Gain Mode S-Parameters S21



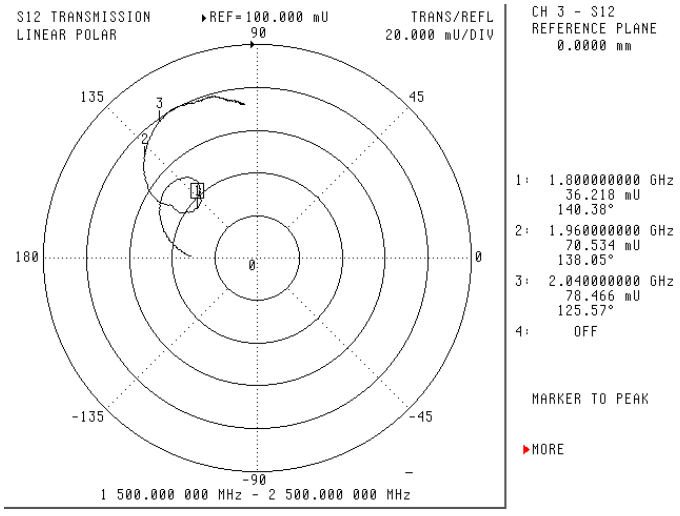
TQ3632 High Gain Mode S-Parameters S22



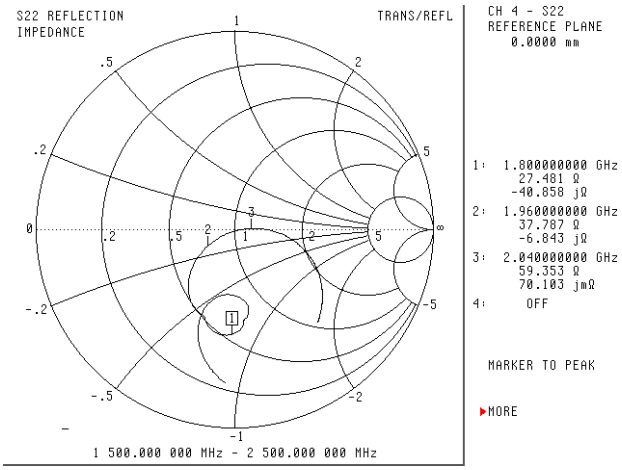
TQ3632 High Gain Low Linearity Mode S-Parameters S21



TQ3632 High Gain Low Linearity Mode S Parameters S11

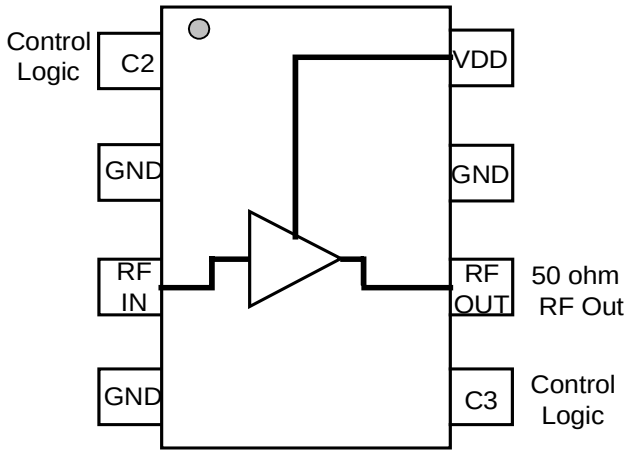


TQ3632 High Gain Low Linearity Mode S-Parameters S12



TQ3632 High Gain Low Linearity Mode S-Parameters S22

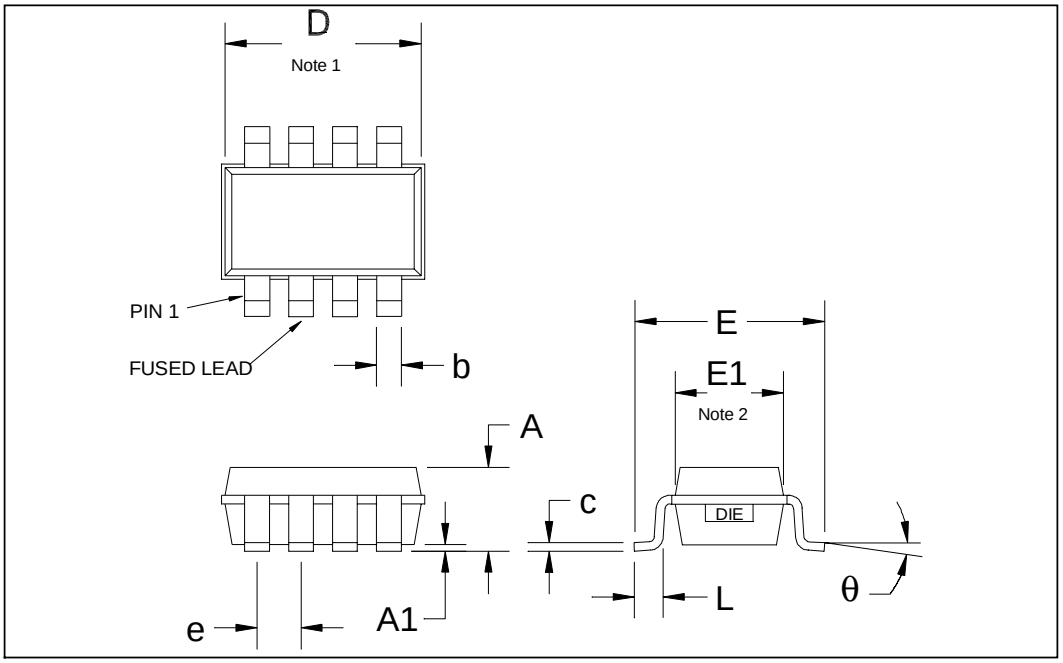
Package Pinout



Pin Descriptions

Pin Name	Pin #	Description and Usage
C2	1	Control logic 2
GND	2	Ground, paddle
RF IN	3	RF input, off-chip matching required
DC GND	4	Source of input FET
C3	5	Control logic 3
RF OUT	6	RF output, no matching required
GND	7	Ground
Vdd	8	LNA Vdd, typical 2.8V, C2 capacitor required

Package Type: SOT23-8 Plastic Package



DESIGNATION	DESCRIPTION	METRIC		ENGLISH		NOTE
A	OVERALL HEIGHT	1.20	+/-.25 mm	0.05	+/-.250 in	3
A1	STANDOFF	.100	+/-.05 mm	.004	+/-.002 in	3
b	LEAD WIDTH	.365	mm TYP	.014	in	3
c	LEAD THICKNESS	.127	mm TYP	.005	in	3
D	PACKAGE LENGTH	2.90	+/-.10 mm	.114	+/-.004 in	1,3
e	LEAD PITCH	.65	mm TYP	.026	in	3
E	LEAD TIP SPAN	2.80	+/-.20 mm	.110	+/-.008 in	3
E1	PACKAGE WIDTH	1.60	+/-.10 mm	.063	+/-.004 in	2,3
L	FOOT LENGTH	.45	+/-.10 mm	.018	+/-.004 in	3
Theta	FOOT ANGLE	1.5	+/-1.5 DEG	1.5	+/-1.5 DEG	

Notes
1. The package length dimension includes allowance for mold mismatch and flashing.
2. The package width dimension includes allowance for mold mismatch and flashing.
3. Primary dimensions are in metric millimeters. The English equivalents are calculated and subject to rounding error.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: info_wireless@tqs.com **Fax: (503) 615-8900**

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