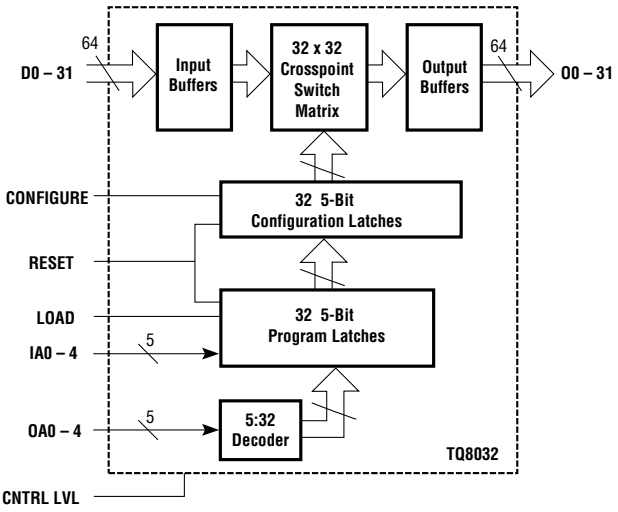
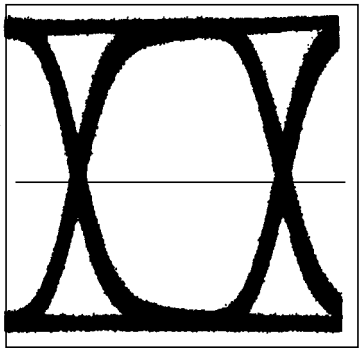
TQ8032

800 Megabit/sec 32x32 Digital ECL Crosspoint Switch





Typical output waveform with all channels driven

The TQ8032 is a non-blocking 32 x 32 digital crosspoint switch capable of 800 Megabits per second per port data rates. Utilizing a fully differential internal data path and ECL I/O, the TQ8032 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8032 is ideally suited for digital video, data communications and telecommunication switching applications.

The non-blocking architecture uses 32 fully independent 32:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 5-bit program latch (OA0:4) with the desired input port address (IA0:4) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

	Min	*Max*	*Units*
Data Rate/Port	800		Mb/s
Jitter		150	ps pk-pk
Channel Propagation Delay		2300	ps
Ch-to-Ch Propagation Delay Skew		500	ps

Features

- *>25 Gb/s aggregate BW*
- *800 Mb/s/port NRZ data rate*
- *Non-blocking architecture*
- *500 ps delay match*
- *Differential ECL-level data I/O; Selectable CMOS/TTL-level control inputs*
- *Low jitter and signal skew*
- *Fully differential data path*
- *Double buffered configuration latches*
- *196-pin CQFP package*

Applications

- *Telecom/Datacom Switching*
- *Hubs and Routers*
- *Video Switching*

SWITCHING PRODUCTS

Figure 1. Architecture

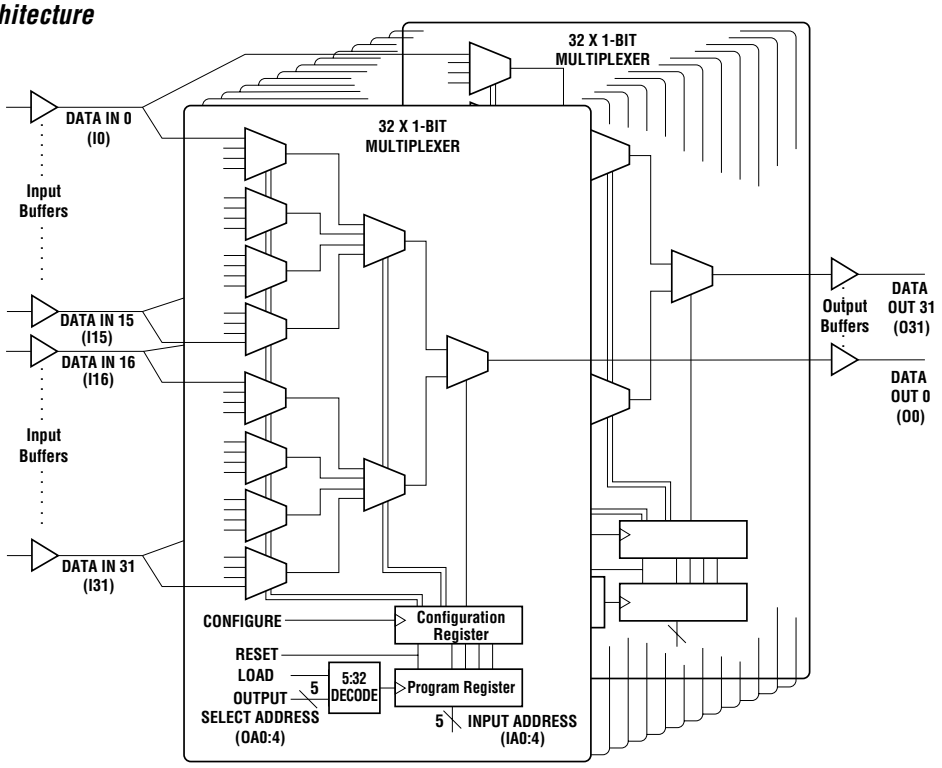


Table 2. Pin Descriptions

Signal	*Name/Level*	*Description*
I0 to I31, NI0 to NI31	Data input true and complement. Differential ECL	Differential data input ports.
O0 to O31, NO0 to NO31	Data output true and complement. Differential ECL	Differential data output ports.
IA0:4	Input address. CMOS/TTL	Input port selection address that is written into the selected output port program latches (OA0:4).

IA4	IA3	IA2	IA1	IA0	Input port
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
:	:	:	:	:	:
1	1	1	1	1	31

OA0:4 CMOS/TTL	Output select address.	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:4) is written.

OA4	OA3	OA2	OA1	OA0	Output port
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
:	:	:	:	:	:
1	1	1	1	1	31

Figure 2. Package Pinout

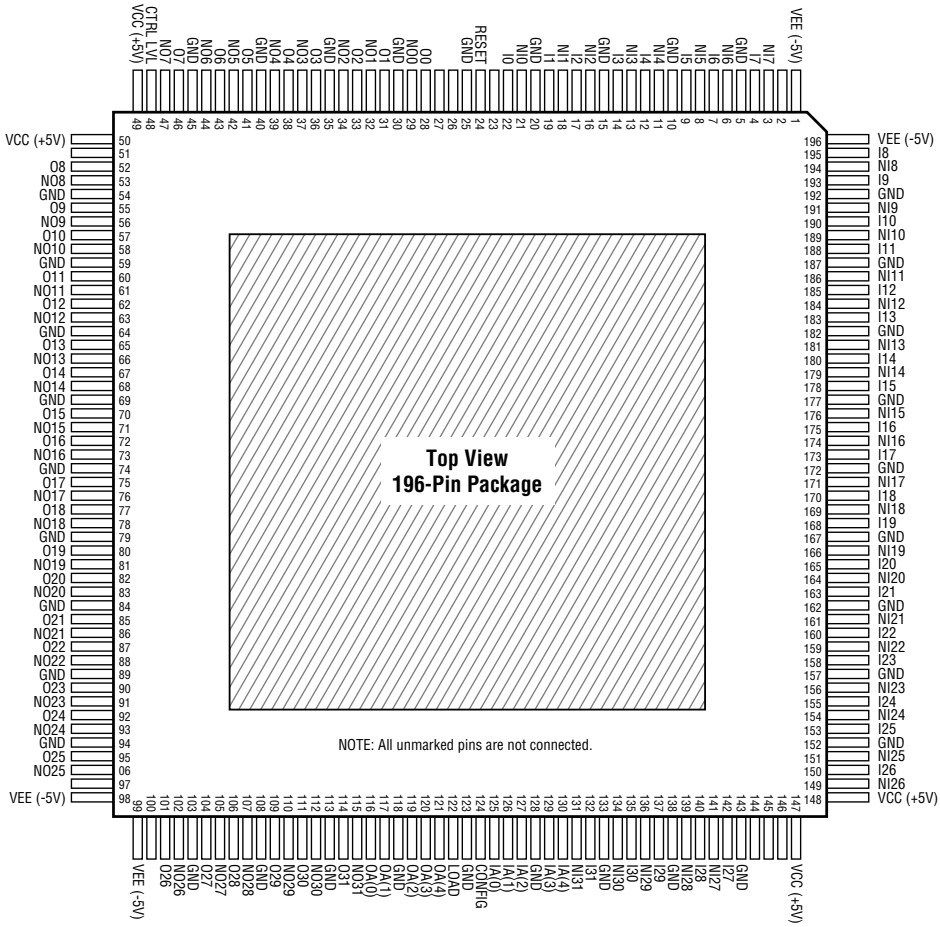


Table 2. Pin Descriptions *(continued)*

Signal	*Name/Level*	*Description*
LOAD	CMOS/TTL Latches the data when set to a 'low' level.	Enables the selected output port program latches while set 'high'.
CONFIGURE	CMOS/TTL	Transfers the program latches data to the configuration latches and implements the switch changes while set "high." Latches the data when set to a "low" level.
RESET	CMOS/TTL	Puts the switch into *Broadcast* or *Pass-Through* configuration, overwriting existing configurations. **Broadcast mode:** All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low." **Pass-through mode:** I0 is connected to O0, I1 to O1, etc. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "high."
CNTRL LVL	Input level control. GND/Open	Selects the input levels for the input address (IA0:4), output address(OA0:4), CONFIGURE, LOAD and RESET inputs. Inputs are configured for TTL when tied to GND and CMOS when left unconnected.

Table 3. Absolute Maximum Ratings[5]

Symbol	Parameter	Absolute Max. Rating	Notes
T_{STOR}	Storage Temperature	–65° C to +150° C	
T_{CH}	Junction (Channel) Temperature	–65° C to +150° C	1
T_C	Case Temperature Under Bias	–65° C to +125° C	2
V_{CC}	Supply Voltage	0 V to +7 V	3
V_{EE}	Supply Voltage	–7 V to 0 V	3
V_{TT}	Load Termination Supply Voltage	V_{EE} to 0 V	4
V_{IN}	Voltage Applied to Any ECL Input; Continuous	V_{EE} –0.5 V to +0.5 V	
I_{IN}	Current Into Any ECL Input; Continuous	–1.0 mA to +1.0 mA	
V_{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	–0.5 V to V_{CC} +0.5 V	
I_{IN}	Current Into Any TTL/CMOS Input; Continuous	–1.0 mA to +1.0 mA	
V_{OUT}	Voltage Applied to Any ECL Output	V_{EE} –0.5 V to +0.5 V	4
I_{OUT}	Current From Any ECL Output; Continuous	–40 mA	
P_D	Power Dissipation per Output $P_{OUT} = (GND – V_{OUT}) \times I_{OUT}$	50 mW	

Notes: 1. For die applications.
2. T_C is measured at case top.
3. All voltages specified with respect to GND, defined as 0V.
4. Subject to I_{OUT} and power dissipation limitations.
5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 4. Recommended Operating Conditions[4]

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Case Operating Temperature	0		85	°C	1,3
V_{CC}	Supply Voltage	4.5		5.5	V	
V_{EE}	Supply Voltage	–5.5		–4.5	V	
V_{TT}	Load Termination Supply Voltage		–2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ_{JC}	Thermal Resistance Junction to Case			2	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
3. Contact the Factory for extended temperature range applications.
4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 5. DC Characteristics[1,2] – *Within recommended operating conditions, unless otherwise indicated.*

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	–1100	–500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}	–1500	mV		
I_{IH}	ECL Input Current High		+30	µA	V_{IH} = –0.7 V	
I_{IL}	ECL Input Current Low		–30	µA	V_{IL} = –2.0 V	
V_{ICM}	ECL Input Common Mode Voltage	–1500	–1100	mV		
V_{IDIF}	ECL Input Differential Voltage (pk-pk)	400	1200	mV		
V_{IH}	CMOS/TTL Input Voltage High	3.5/2.0	V_{CC}/V_{CC}	V		2
V_{IL}	CMOS/TTL Input Voltage Low	0/0	1.5/0.8	V		2
I_{IH}	CMOS/TTL Input Current High		+100	µA	$V_{IH} = V_{CC}$	2
I_{IL}	CMOS/TTL Input Current Low		–100	µA	V_{IL} = 0 V	2
V_{OCM}	ECL Output Common Mode	–1500	–1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600		mV		
V_{OH}	ECL Output Voltage High	–1000	–600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}	–1600	mV		
I_{OH}	ECL Output Current High	20	27	mA		
I_{OL}	ECL Output Current Low	0	8	mA		
I_{CC}	Power Supply Current (+)		20	mA		
I_{EE}	Power Supply Current (–)		–1950	mA		

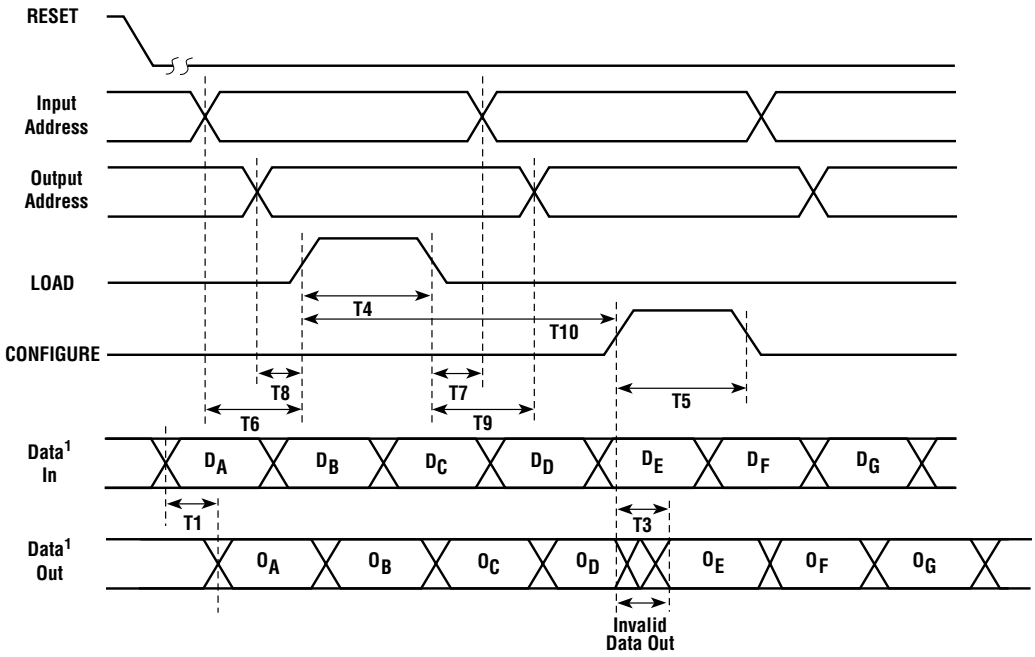
Notes: 1. Test conditions unless otherwise indicated: V_{TT} = –2.0 V, R_{LOAD} = 50 Ω to V_{TT}.
2. Input level is selected by the CNTRL_LVL input. Tieing CNTRL_LVL to GND selects TTL levels, leaving CNTRL_LVL OPEN selects CMOS levels.

Table 6. AC Characteristics[1] – *Within recommended operating conditions, unless otherwise indicated.*

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			800	Mb/s	1,2
	Jitter			150	ps pk-pk	1
T_1	Channel Progagation Delay			2300	ps	
T_2	Channel-to-Channel Delay Skew			500	ps	
T_3	CONFIG to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	7			ns	
T_5	CONFIG Pulse Width	7			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	3			ns	
T_8	OAi to LOAD High Setup Time	0			ns	
T_9	LOAD to OAi Low Hold Time	3			ns	
T_{10}	Load ↑ to CONFIG ↑	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		300	400	ps	3

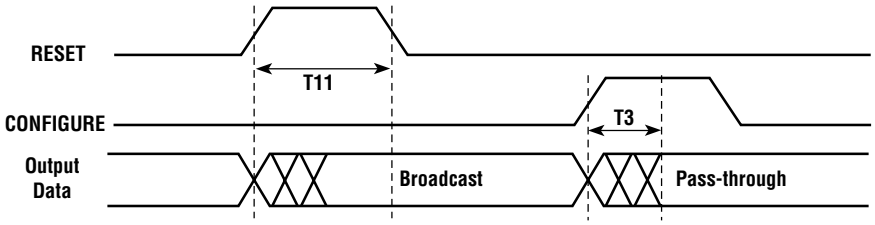
Notes: 1. Test conditions: V_{TT} = –2.0 V, R_{LOAD} = 50 Ω to V_{TT}; ECL inputs: V_{IH} = –1.1 V; V_{IL} = –1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: $V_{OH} \geq$ –1.0 V, $V_{OL} \leq$ –1.6 V; ECL inputs rise and fall times ≤1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E – 13 BER or better for 2^{23} – 1 PRBS pattern, jitter and rise/fall times are guaranteed through characterization.
2. 800 Mb/s Non-Return-Zero (NRZ) data equivalent to 400 MHz clock signal.
3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 3. Timing Diagram – Switch Configuration



Notes: 1. No data loss on unchanged paths.

Figure 4. Timing Diagram – Reset



Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
2. "Broadcast" is defined as data input 0 to all data outputs (0..31).
3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

Typical Performance Data

Figure 5. Jitter – Single Channel

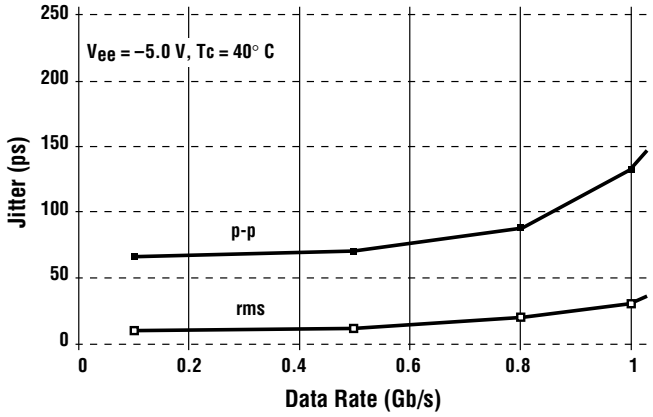


Figure 6. Output Delay

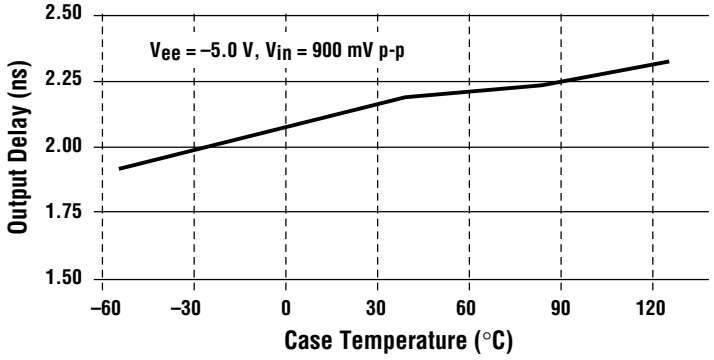
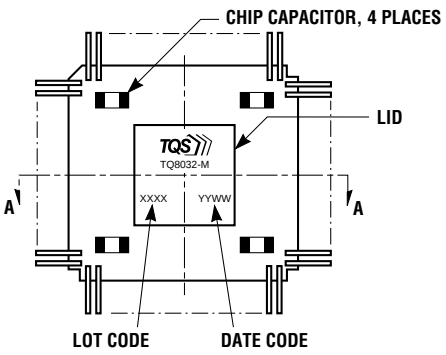
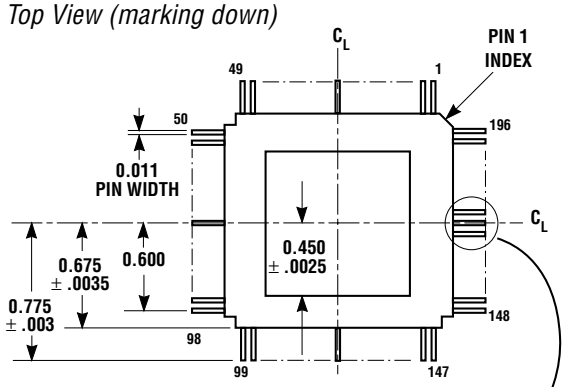


Figure 7. Mechanical Dimensions

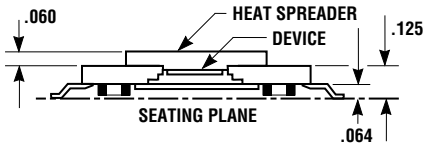
Bottom View (marking up)

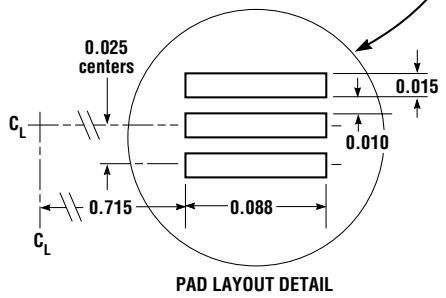


Top View (marking down)



Section A-A





Ordering Information

TQ8032-M *800 Mb/s 32x32 ECL Crosspoint Switch*

Additional Information

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