

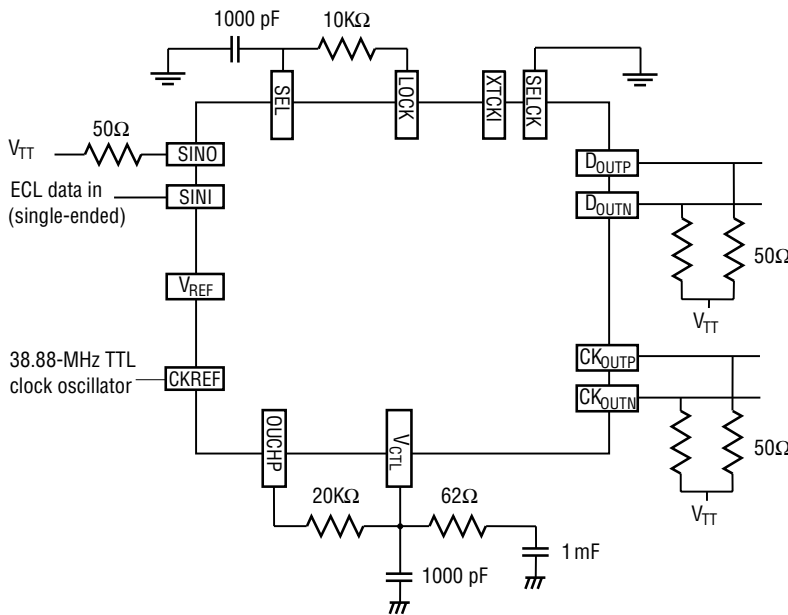
The TQ8103 is a monolithic clock and data recovery (CDR) IC that receives NRZ data, extracts the high-speed clock, and presents the separated data and clock as its outputs. This device is designed specifically for SONET OC-12 and SDH STM-4 applications at 622 Mb/s.

Its on-chip phase-locked loop (PLL) generates a stable 622.08 Mb/s reference based upon an external 38.88 MHz TTL reference. The PLL is based on a VCO constructed from integrated reactive components, which form a low-jitter, high-Q differential tank circuit. Both frequency- and phase-detect circuits reliably acquire and hold lock in worst-case SONET jitter conditions and scrambling patterns. The lock-detect circuitry signals when the CDR acquires frequency lock.

Typical SONET/SDH system applications for the TQ8103 include:

- Transmission system transport cards
- Switch and cross-connect line cards
- ATM physical layer interfaces
- Test equipment
- Add/drop multiplexers

Figure 1. Typical Application



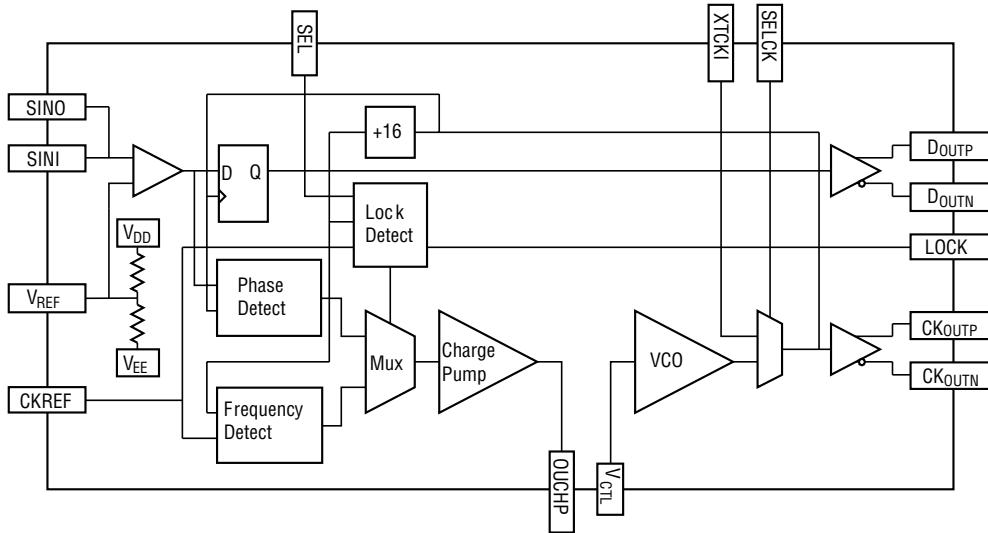
TQ8103

622 Mb/s Clock & Data Recovery

Features

- Single-chip CDR circuit for 622 Mb/s data
- Exceeds Bellcore and ITU jitter tolerance maps
- Single-ended ECL input has loop-through path for external 50 ohm termination to minimize stubs and reflections
- Clock and data outputs are differential ECL
- Provides complete high-speed OC-12/STM-4 solution when used with TQ8101 or TQ8105 Mux/Demux/Framer/PLL
- External loop filter requires simple passive network
- Maintains clock in absence of data
- 28-pin leaded chip carrier
- Can be used with a high-speed external clock

Figure 2. TQ8103 Block Diagram



Functional Description

The TQ8103 CDR integrates separate detectors for acquiring frequency lock and maintaining precise phase lock. When the CDR is locked onto an incoming NRZ data stream, its phase-detect circuitry compares the phase of the incoming NRZ data and the phase of the generated 622.08 MHz clock. When they differ, the resulting error signal nulls the phase difference and puts the generated 622.08 MHz clock back in phase with the incoming data. In this mode, the LOCK output is high.

The phase-detect circuit operates only when the incoming NRZ data transitions between states. SONET and SDH employ scrambling, which provides an average transition density of 50 percent; however, some data patterns can generate legitimate scrambled signals with a significant number of consecutive ones or zeros. The TQ8103 maintains lock over bit sequences of over 100 consecutive zeros or ones.

When the input data is lost or too many bit times occur without a transition, the PLL (which generates the 622.08 MHz clock) eventually drifts. The lock-detect circuit constantly compares the generated 622.08 MHz clock (divided by 16) and the external 38.88 MHz

reference. When the PLL drifts more than 2000 PPM from the reference, the LOCK output goes low.

The SEL input selects between the phase-detect and frequency-detect circuits. When the PLL drifts out of lock, taking SEL low reverses the drift by switching in the frequency-detect circuit. Connecting the LOCK output directly to the SEL input should ensure that frequency lock is maintained in the absence of data. It is recommended, however, that a low-pass filter be added between LOCK and SEL to allow for orderly transitions between these circuits. Once the PLL frequency is within 500 PPM of the reference, the LOCK output returns high. As the SEL input goes high, the phase-detect circuit again maintains lock to the incoming NRZ data.

The TQ8103 can also be used as a standalone 622.08 MHz frequency reference. When SEL is held low, the PLL utilizes only the frequency-detect circuit. The PLL locks onto the external 38.88 MHz reference to generate the desired 622.08 MHz output.

Application Information

Loop Filter Design

The TQ8103 requires an external loop filter. Care should be taken in the implementation of the filter. Good high-frequency design techniques should be used, with the loop filter being connected into the analog ground. The analog supply should be well filtered.

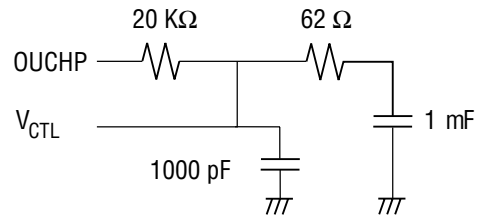
Data Input Considerations

The serial data input line is a high-frequency ECL signal, and should be kept in a 50 ohm controlled impedance environment. Reflections on the serial input are minimized through the use of a separate loopback termination pin, SINO. A 50 ohm chip resistor between SINO and V_{TT} minimizes stub length for the best signal quality. Another physical design consideration is to place the TQ8103 and its companion high-speed ICs as close as possible to the optics while observing good analog design practice on supply filtering and grounding.

External Frequency Reference

The externally supplied 38.88 MHz CKREF input needs to have low jitter with fast rise and fall times. Typical applications will use a telecom crystal oscillator such as the Connor-Winfield S14R6-38.88. SONET requires frequency sources to be accurate to ± 20 ppm over temperature, voltage, and aging. The CKREF input is a reference frequency for initial frequency lock and for the lock-detect circuit, so it can tolerate accuracies of up to ± 100 ppm.

Figure 3. External Loop Filter



Jitter Tolerance

Jitter tolerance describes the ability of the CDR circuit to track timing variations (jitter) in the received signal. The Bellcore and ITU specifications allow the received optical signal to contain jitter. The amount of jitter that must be tolerated is a function of the frequency content of the jitter. The CDR must tolerate many unit intervals (bit times) of low-frequency jitter, but is not asked to tolerate large amounts of jitter at higher frequency. The performance shown in the “Typical Performance Data” section shows that the TQ8103 offers a wide margin over the specification limits.

Jitter tolerance is a system-level issue that is directly affected by the quality of the optics, the quality of the layout (and decoupling), and the specific implementation of the loop filter. The recommended loop filter, described above, has been chosen to provide a robust margin on jitter tolerance.

TQ8103

Figure 4. TQ8103 Pinout

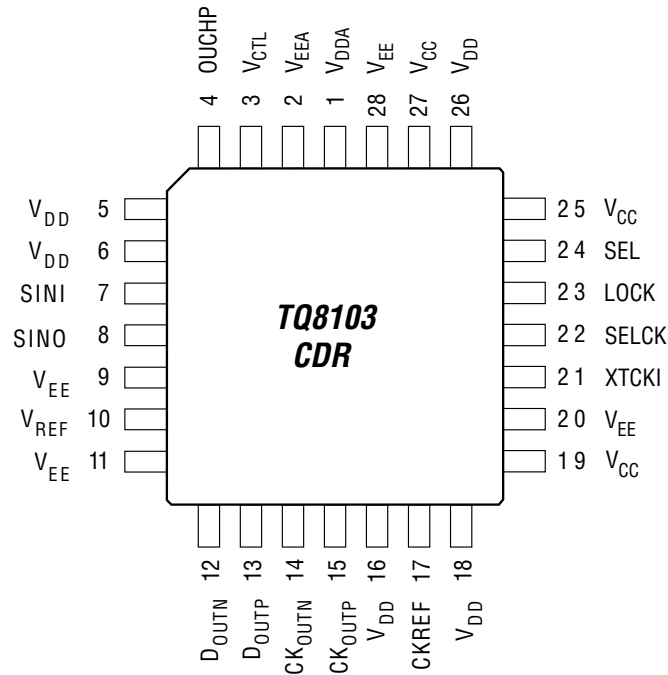


Table 1. Signal Descriptions

Pin	Signal	Type	Description
1	V _{DDA}	Supply	Analog ground for VCO
2	V _{EEA}	Supply	Analog -5V supply for VCO
3	V _{CTL}	Analog In	VCO control voltage input; connect to loop filter
4	OUCHP	Analog Out	Charge pump output; connect to loop filter
5	V _{DD}	Supply	Ground (0V)
6	V _{DD}	Supply	Ground (0V)
7	SINI	ECL In	Serial data input
8	SINO	ECL Term	Loopback of SINI for termination of serial data input; connect with 50 Ω to V _{TT}
9	V _{EE}	Supply	-5V supply
10	V _{REF}	Analog	Optional reference voltage for single-ended ECL input
11	V _{EE}	Supply	-5V supply
12	D _{OUTN}	ECL Out	Differential data output, complement
13	D _{OUTP}	ECL Out	Differential data output, true
14	CK _{OUTN}	ECL Out	Differential clock output, complement

(Continued on next page)

Table 1. Signal Descriptions (continued)

Pin	Signal	Type	Description
15	CK _{OUTP}	ECL Out	Differential clock output, true
16	V _{DD}	Supply	Ground (0V)
17	CKREF	TTL In	Reference clock input for frequency detect and lock detect
18	V _{DD}	Supply	Ground (0V)
19	V _{CC}	Supply	+5V supply
20	V _{EE}	Supply	-5V supply
21	XTCKI	ECL In	External clock input; selected using SELCK
22	SELCK	TTL In	External clock select: low = internal VCO, high = XTCLK
23	LOCK	TTL Out	Lock-detect output
24	SEL	TTL In	Detection circuit select; low = frequency-detect, high = phase-detect
25	V _{CC}	Supply	+5V supply
26	V _{DD}	Supply	Ground (0V)
27	V _{CC}	Supply	+5V supply
28	V _{EE}	Supply	-5V supply

Specifications

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply	V _{CC}	4.5	5	5.5	V
Negative supply	V _{EE}	-5.5	-5	-4.75	V
Termination voltage	V _{TT}	-1.9	-2.0	-2.1	V
Operating ambient temperature	T _A	0		85	°C

Table 3. Power Consumption

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply current	I _{CC}			5	mA
Negative supply current	I _{EE}			210	mA
Thermal impedance	θ _{JA}		4.0		°C/W

Note: These values supersede the recommended operating conditions (Table 2) unless otherwise noted.

TQ8103

Table 4. DC Characteristics—ECL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	(2)	V_{REF}		-1300		mV
Input HIGH voltage	(3)	V_{IH}	-1100		-700	mV
Input LOW voltage	(3, 4)	V_{IL}	V_{TT}		-1500	mV
Output HIGH voltage	(5)	V_{OH}	-1000	0	-700	mV
Output LOW voltage	(5)	V_{OL}	V_{TT}		-1600	mV
Input HIGH current	(6)	I_{IH}		10		μ A

Table 5. DC Characteristics—TTL I/O (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0		V_{CC}	V
Input LOW voltage		V_{IL}	0		0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}			100	μ A
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-100			μ A
Output HIGH voltage	$I_{OH} = 3$ mA	V_{OH}	2.4		V_{CC}	V
Output LOW voltage	$I_{OL} = -1$ mA	V_{OL}	0		0.4	V
Input capacitance	(6)	C_{IN}		8		pF
Output capacitance	(6)	C_{OUT}		10		pF

Table 6. AC Characteristics (1)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Clock to data time	Figure 5	t_0	100		350	ps
Data output rise/fall times	(7)	t_R, t_F			350	ps
Clock output rise/fall times	(7)	t_R, t_F			300	ps
TTL output rise/fall times	(8)	t_R, t_F		5		ns
Acquire time	(9)			3		ms

Notes (Tables 4, 5, and 6):

1. Applies over recommended operating range
2. Single-ended inputs, $V_{EE} = -5V$
3. $V_{REF} = -1300$ mV
4. $V_{TT} = -2.0V$
5. $R_{LOAD} = 50$ ohms to $V_{TT} = -2.0V$
6. Not tested; consistent with V_{OH} and V_{OL} tests
7. 50 ohm load, 20% to 80% levels
8. 20 pF load, 0.8V to 2.0V
9. With recommended loop filter

Figure 5. Clock-to-Data Timing

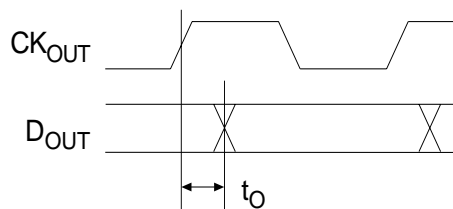


Table 7. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Positive supply	V_{CC}		0	7	V
Negative supply	V_{EE}		-7	0	V
Output voltage	V_O	ECL	$V_{EE} - 0.5$	+0.5	V
Output current	I_O	ECL	—	40	mA
Input voltage	V_I	ECL	$V_{EE} - 0.5$	+0.5	V
Input current	I_I	ECL	-1	1	mA
Output voltage	V_O	TTL	-0.5	$V_{CC} + 0.5$	V
Output current	I_O	TTL		20	mA
Input voltage	V_I	TTL	-0.5	$V_{CC} + 0.5$	V
Input current	I_I	TTL	-1	1	mA
Junction temperature	T_J		-55	+150	° C
Storage temperature	T_S		-65	+175	° C
Power dissipation	P_D			2	W

- Notes:
- If the device is subjected to the listed conditions, its reliability may be impaired.
 - Beyond the listed conditions, the safety of the device cannot be guaranteed.

Typical Performance Data

Figure 6. Jitter Tolerance

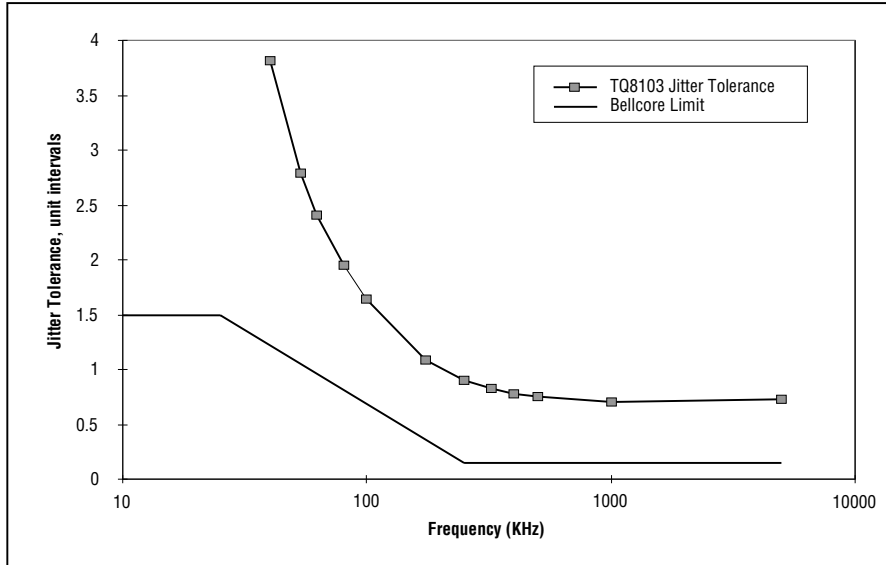


Figure 7. Output Eye Diagram with extracted clock

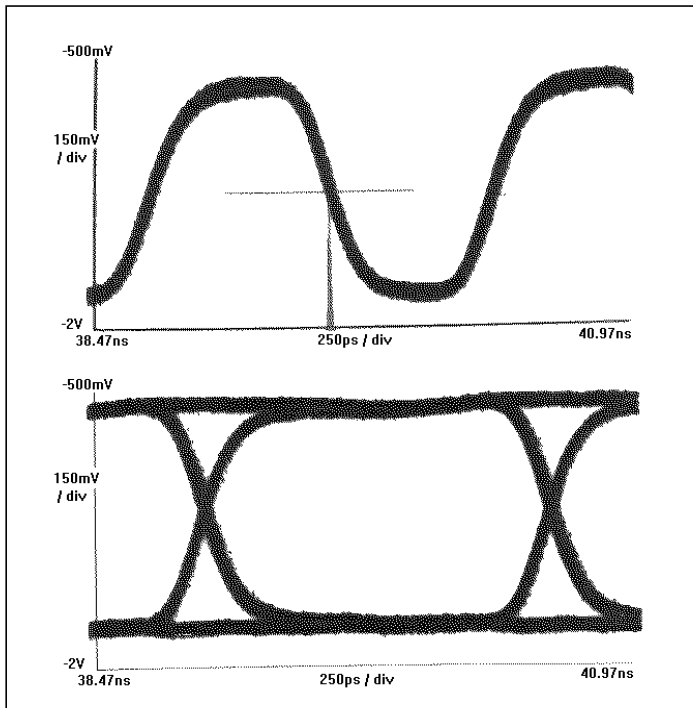
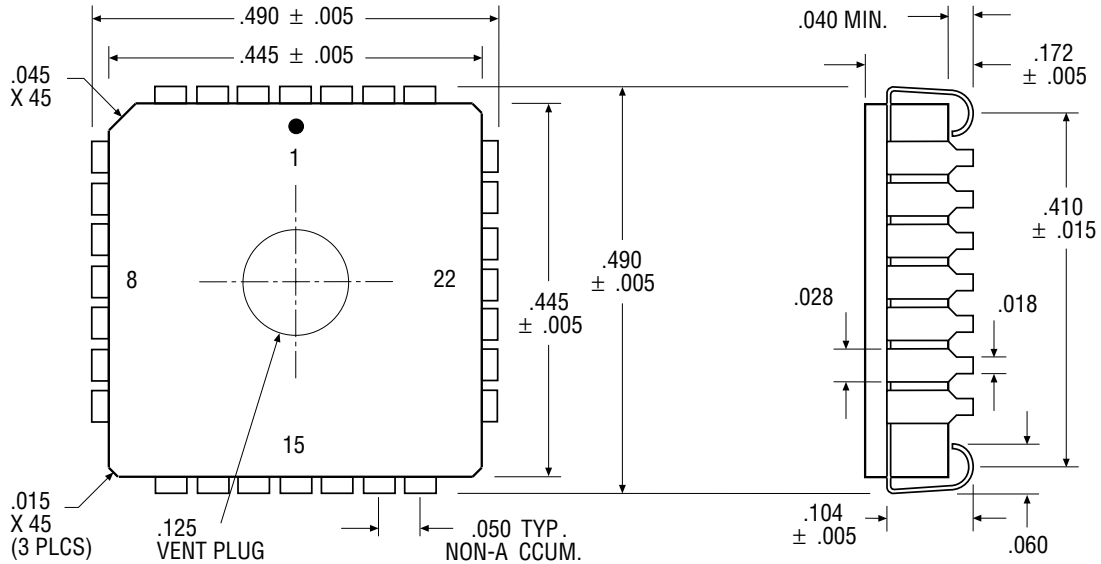


Table 8. Typical Performance Data

Waveforms	2012
PRBS data pattern	2 ⁻²³
RMS jitter	7.855 ps
Peak-to-peak jitter	55 ps

Mechanical Specifications

Figure 8. TQ8103 Package Dimensions



TELECOM PRODUCTS

Ordering Information

- TQ8103-Q** 622 Mb/s Clock & Data Recovery IC in 28-pin MQuad Package
- ETF-8103** Evaluation Board

Additional Information

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