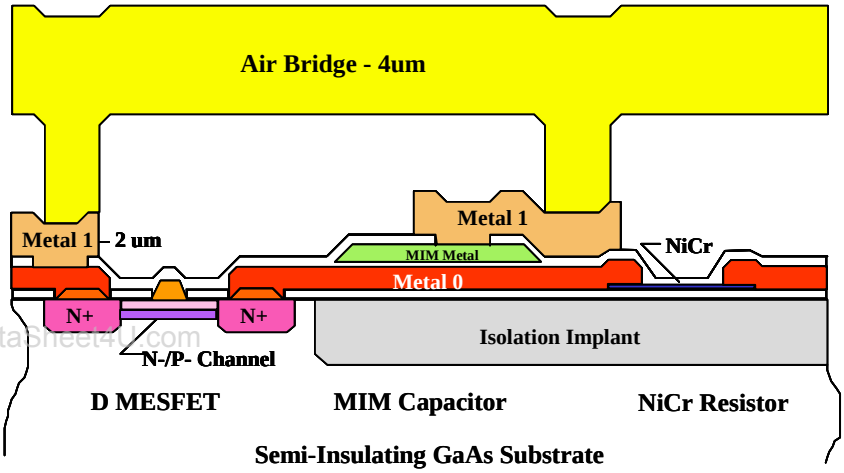
TQHiP

Power MESFET Foundry Service



TQHiP Process Cross-Section

General Description

TriQuint's TQHiP process is our robust, high power density MESFET process. It provides a straight-forward, low cost process for a variety of circuits and applications. Its high operating and breakdown voltages make it ideal for wireless or wired infrastructure applications. A thick (4 µm) gold airbridge complements the 2 µm thick gold global metal and 0.5 µm thick gold surface layer for wiring flexibility and interconnect density. Precision NiCr resistors and high value MIM capacitors are included.

Features

- Power MESFET Process
- Interconnects:
  - 2 Global (one airbridge)
  - 1 Local
- High-Q Passives
- Bulk & Thin Film Resistors
- Backside Vias Optional
- High Volume Production Processes
- Validated Models and Design Support

Applications

- Power Amplifiers
- Switches
- Frequencies thru X-Band
- Base Station Driver Amplifiers
- CATV Line Amplifiers
- Cellular Power Amps, Drivers, Switches

TriQuint Semiconductor
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TQHiP Process Details

TQHiP Process Details			
Element	**Parameter**	**Value**	**Units**
D-FET	Vp	-2.3	V
	Gate Length	0.5	um
	Idss	245	mA/mm
	Imax	370	mA/mm
	Ft @ 50% Idss	16.5	GHz
	Fmax	60	GHz
	Gm	140	mS/mm
	BVgso, Typical	9	V
	BVgdo, Typical	14	V
	BVds, Typical	18	V
Interconnect	Metal Layers	3	
MIM Caps	Values	600	pF/mm2
Resistors	NiCr	50	Ohms/sq
	Bulk	800	Ohms/sq
Inductors	Q	25	@ 2 GHz
Vias		Yes	
Mask Layers	No Vias	14	
	With Vias	16	

Maximum Ratings

Operating Temperature Range	**-65 to +150**	**ºC**
Capacitor Breakdown Voltage—Typ.	40	V
Min.	25	V

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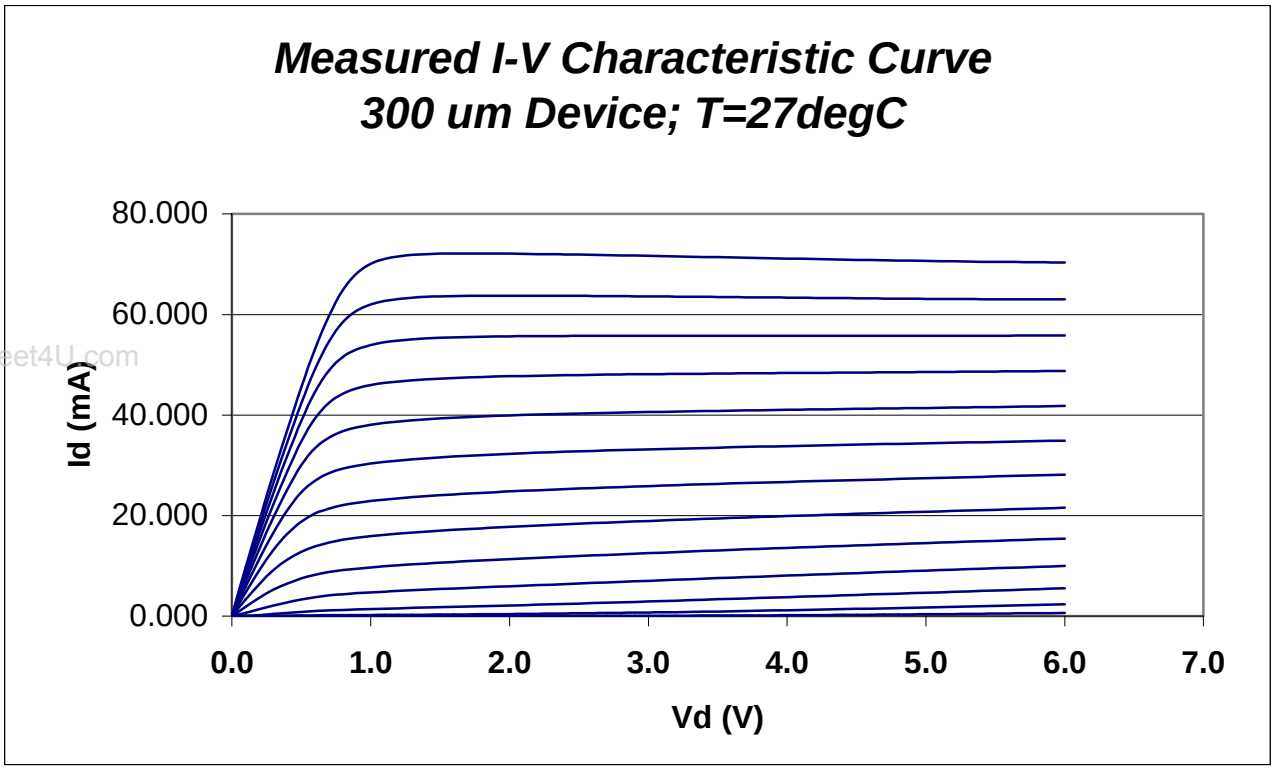

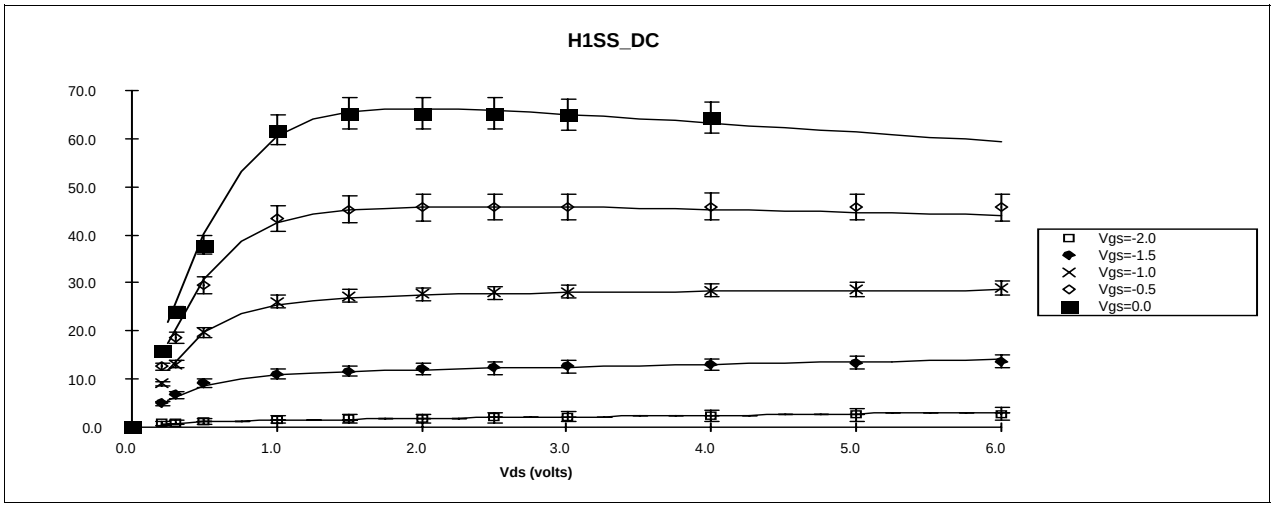

Measured vs. Modeled DC Characteristics; H1SS - D1010 FET
(Lg = 1.0mm, Lgs = Lgd = 1.0mm) Model Parameters; @ T=27°C.

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Prototyping and Development

- Prototype Wafer Option (PWO):
  - Customer-specific Masks, Customer Schedule
  - 2 wafers delivered
  - Hot Lot Cycle Time
  - With thinning and sawing; optional backside vias
- Design Sensitivity Test Run (DST):
  - Yield Analysis
  - Design Sensitivity to Process Variation
  - 14 Wafer Start; Spread of Vp and Cgs values

Design Tools Available

- Device Library of Circuit Elements: FET, Diodes, Thin Film and Implanted Resistors, Capacitors, Inductors
- Parameters for "TriQuint's Own Model" (TOM) in Popular Simulators
- Agilent ADS Design Kit Available Now
- PSPICE Models Available Now
- Layout and Verification Kit for ICEditors Now
- Qualified Package Models for Supported Package Styles

Training

- GaAs Design Classes:
  - Half Day Introduction; Upon Request
  - Four Day Technical Training; Fall & Spring at TriQuint Oregon facility
- For Training and Schedules please visit::
  www.triquint.com/foundry

Process Qualification Status

- TQHiP is a fully released and qualified process
- Reliability Reports
  - TQHiP Process Qualification
  - High Power Product Qualification
  - TQHiP Element Qualification Report
- For more information on Quality and Reliability, contact TriQuint or visit: www.triquint.com/manufacturing/QR/bdy_qr-pubs.htm

Applications Support Services

- Tiling of GDSII Stream Files including PCM
- Design Rule Check Services
- Layout versus Schematic Check Services
- Packaging Development Engineering
- Test Development Engineering:
  - On-Wafer
  - Packaged Parts
- Thermal Analysis Engineering
- Yield Enhancement Engineering
- Part Qualification Services
- Failure Analysis

Manufacturing Services

- Mask Making
- Production 150 Wafer Fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Die Sort Testing
- RF On-Wafer Testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative/ Distributor or Foundry Services Division Marketing for Additional information:
E-mail: sales@triquint.com; Phone: (503) 615-9000 Fax: (503) 615-8905