TQL9065

Ultra Low Noise 2-Stage Bypass LNA

Applications

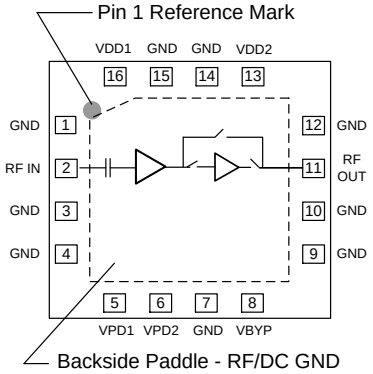
- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

16-pin 3.5 x 3.5 mm Package

Product Features

- 1.5 – 3.8 GHz Operational bandwidth
- 2nd stage LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 0.5 dB at 1.95 GHz
- 36 dB Gain at 1.95 GHz, 17 dB in Low Gain Mode
- +35 dBm Output IP3 in High Gain Mode
- +34 dBm Output IP3 in Low Gain Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 3.5x3.5 mm 16-pin SMT package

Functional Block Diagram



General Description

The TQL9065 is a high-linearity, ultra-low noise 2-stage gain block amplifier module with a bypass mode functionality integrated to the second stage in the product. At 1.95 GHz, the amplifier, under high gain mode, typically provides 36 dB gain, +35 dBm OIP3, and 0.5 dB noise figure while drawing 160 mA current from a +5 V supply. The component also provides high performance in the low gain mode with 17 dB gain, 0.5dB noise figure and +34 dBm OIP3 while drawing 70 mA current.

The TQL9065 is internally matched using a high performance E-pHEMT process. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9065 covers the 1.5 – 3.8 GHz frequency band and is targeted for wireless infrastructure. The TQL9065 is housed in a 3.5 x 3.5 mm SMT package.

Pin Configuration

Pin No.	Label
1,3,4,7,9,10,12,14,15	GND
2	RFin
5	V_{PD1}
6	V_{PD2}
8	V_{BYP}
11	RFout
13	V_{DD2}
16	V_{DD1}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9065	2-stage Bypass LNA
TQL9065-PCB	1.5-3.8 GHz Evaluation Board
Standard T/R size = 2500 pieces on a 13” reel	

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
Drain Voltage (V_{DD})	+7 V
Input Power (CW)	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_{DD})	+3.3	+5.0	+5.25	V
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25°C.

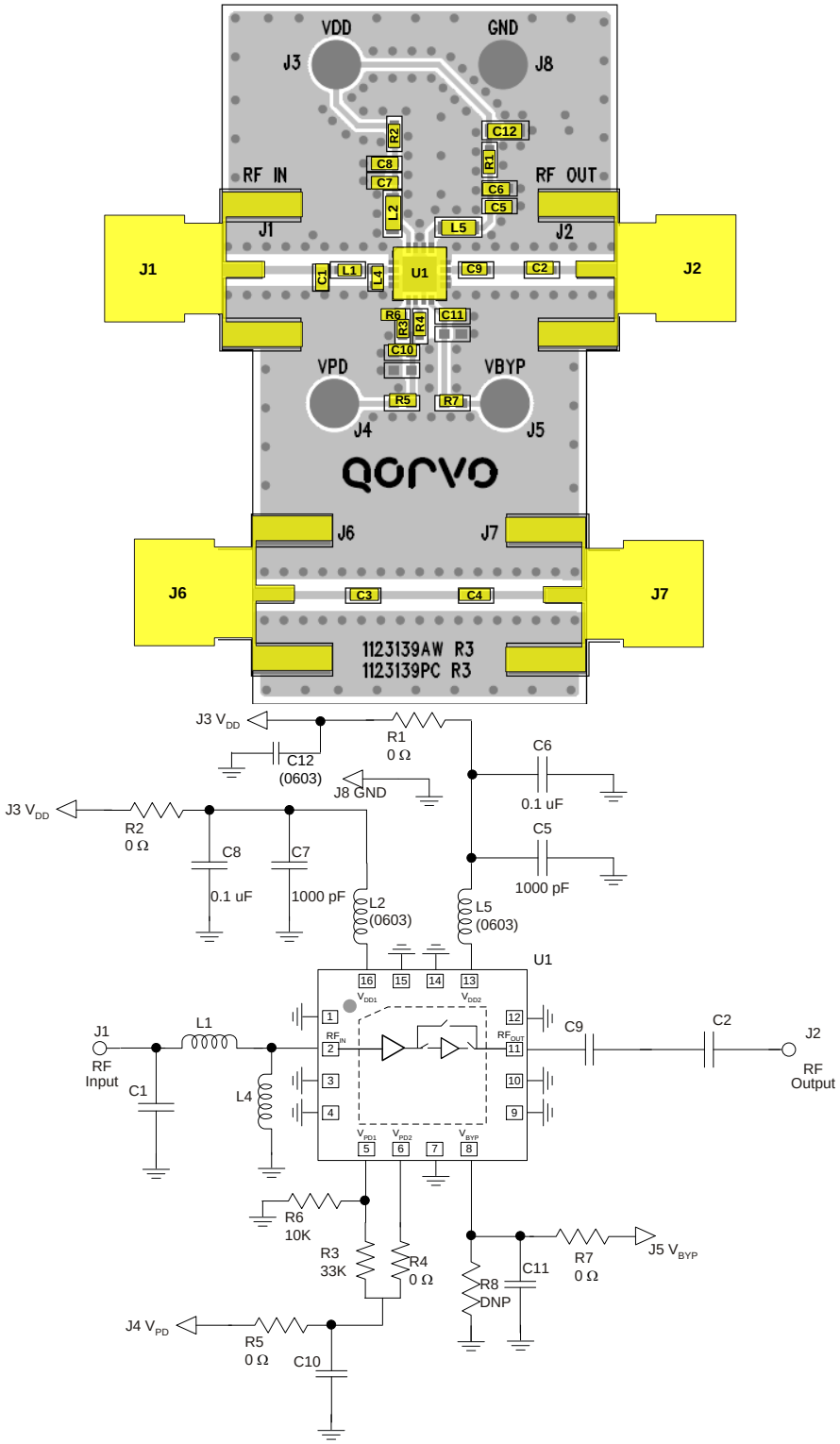
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1500		3800	MHz
Test Frequency			1950		MHz
Gain	LNAs ON, Bypass OFF		36		dB
Input Return Loss	LNAs ON, Bypass OFF		15		dB
Output Return Loss	LNAs ON, Bypass OFF		13		dB
Noise Figure	LNAs ON, Bypass OFF		0.5		dB
Output P1dB	LNAs ON, Bypass OFF		+20		dBm
Output IP3	LNAs ON, Bypass OFF, Pout=+5 dBm/tone, Δf=1 MHz		+35		dBm
Gain	LNA1 ON, Bypass ON		17		dB
Input Return Loss	LNA1 ON, Bypass ON		15		dB
Output Return Loss	LNA1 ON, Bypass ON		12		dB
Noise Figure	LNA1 ON, Bypass ON		0.5		dB
Output P1dB	LNA1 ON, Bypass ON		+18		dBm
Output IP3	LNA1 ON, Bypass ON, Pout=+5 dBm/tone, Δf=1 MHz		+34		dBm
Control Voltage, V_{PD}, V_{BYP} (1)	V_{IH}	2.5		V_{DD}	V
	V_{IL}	0		0.4	V
Current, I_D	LNAs ON, Bypass OFF		160		mA
	LNA1 ON, LNA2 OFF, Bypass ON		70		mA
	LNAs OFF, Bypass OFF		5		mA
Switching Speed	LNAs OFF, Bypass OFF to LNAs ON		566		ns
	LNAs ON, Bypass OFF to LNA1 ON, Bypass ON		250		ns
Thermal Resistance, θ_{jc}	High gain Mode (Channel to case)		42		°C/W
	Low gain Mode (Channel to case)		70		°C/W

Notes:
1. These voltages are reference at the turrets labelled V_{PD} and V_{BYP} on the circuit schematic on page 3.

Control Truth Table

V_{PD1}	V_{PD2}	V_{BYP}	State
1	1	0	LNA1 OFF, LNA2 OFF, Bypass OFF
0	0	0	LNA1 ON, LNA2 ON, Bypass OFF
0	x	1	LNA1 ON, LNA2 OFF, Bypass ON
1	x	1	LNA1 OFF, LNA2 OFF, Bypass ON

TQL9065-PCB Evaluation Board



See Evaluation Board PCB Information section for PCB material and stack-up.

Bill of Material – TQL9065-PCB

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	PCB	Qorvo	1123139
U1	n/a	2-Stage Bypass LNA	Qorvo	TQL9065
R1, 2, 4, 5, 7, C2	0 Ω	RES, 0402, +/-5%, 1/16W	Various	
R3	33K	RES, 0402, 5%, 1/16W	Various	
R6	10K	RES, 0402, 5%, 1/16W	Various	
C1	0.5 pF	CAP, 0402, +/-0.1pF, 50V, C0G	Murata	GJM1555C1HR50BB01
L1	1.5 nH	IND, 0402, +/-0.1nH	Murata	LQP15MN1N5B02D
L4	6.8 nH	IND, 0402, 5%	Murata	LQG15HS6N8J02
C3, 4, 5, 7, 9, 10, 11	100 pF	CAP, 0402, +/-5%, 50V	Various	
C6, 8	0.1 uF	CAP, 0402, 20%, 16V, Y5V	Various	
C12	4.7 uF	CAP, 0603, 20%, 10V, Y5V	Various	
L2	5.6 nH	IND, 0603, 5%, 700mA	Coilcraft	0603CS-5N6XJLU
L5	18 nH	IND, 0603, 5%	Coilcraft	0603CS-18NXJL

Typical Performance - High Gain Mode (LNA1 ON, LNA2 ON, Bypass OFF)

Test conditions unless otherwise noted: V_{DD1} = V_{DD2} = +5 V, V_{PD} = 0.4V, V_{BYP} = 0.4V, I_D = 160 mA, Temp.=+25 °C.

Parameter	Typical Value			Units
Frequency	1800	2200	2600	MHz
Gain	37.6	34.8	32.6	dB
Noise Figure	0.50	0.58	0.66	dB
Input Return Loss	16.0	15.0	14.4	dB
Output Return Loss	11.5	13.0	17	dB
OIP3 (Pout/tone=+5 dBm, Δf = 1 MHz)	+36.3	+35.9	+35.3	dBm
P1dB	+20.7	+20.7	+21.2	dBm

Typical Performance - Low Gain Mode (LNA1 ON, LNA2 OFF, Bypass ON)

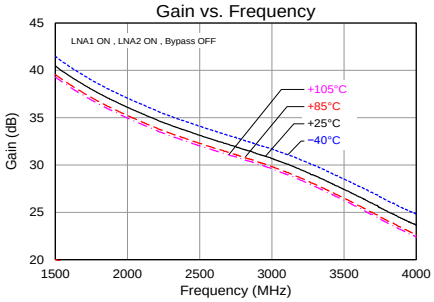
Test conditions unless otherwise noted: V_{DD1} = V_{DD2} = +5 V, V_{PD} = 0.4V, V_{BYP} = 2.5, I_D = 70 mA, Temp.=+25 °C.

Parameter	Typical Value			Units
Frequency	1800	2200	2600	MHz
Gain	17.9	16.3	14.5	dB
Noise Figure	0.45	0.56	0.64	dB
Input Return Loss	15.8	17.1	18.5	dB
Output Return Loss	11.6	13.2	16.7	dB
Output IP3 (Pout/tone=+5 dBm, Δf = 1 MHz)	+35.8	+36.3	+36.1	dBm
P1dB	+18.5	+18.1	+17.8	dBm

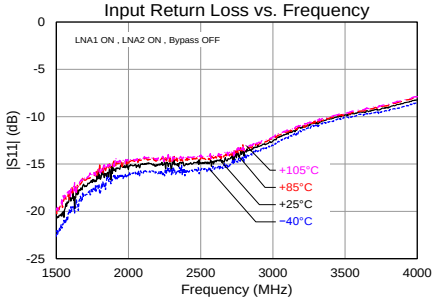
Performance Plots

Test conditions unless otherwise noted: V_{DD1} = V_{DD2} = +5 V

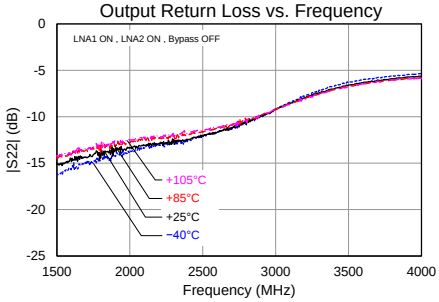
Gain vs. Frequency



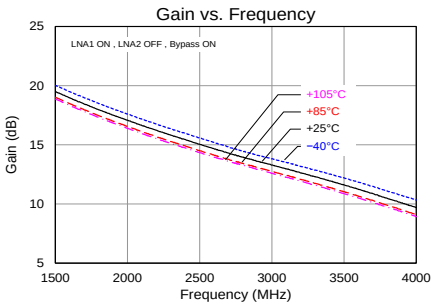
Input Return Loss vs. Frequency



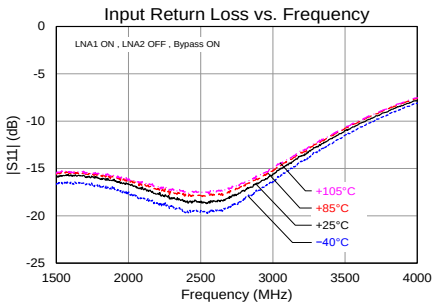
Output Return Loss vs. Frequency



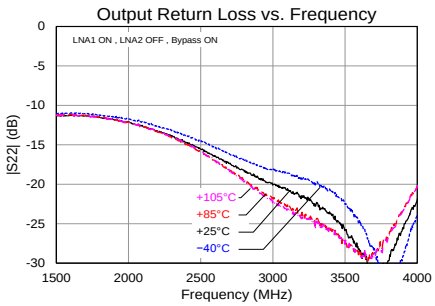
Gain vs. Frequency



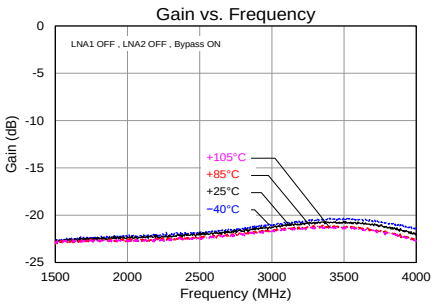
Input Return Loss vs. Frequency



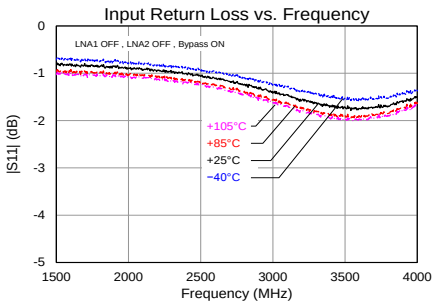
Output Return Loss vs. Frequency



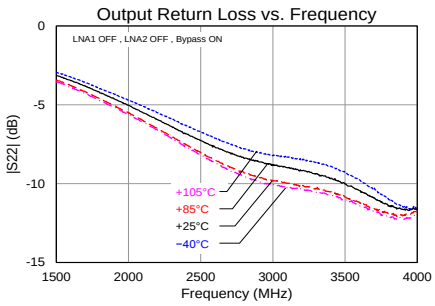
Gain vs. Frequency



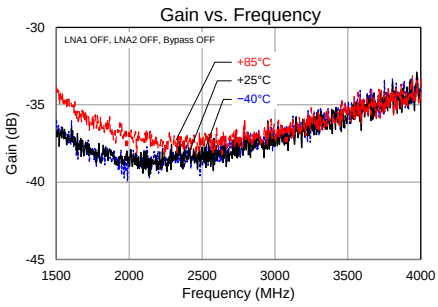
Input Return Loss vs. Frequency



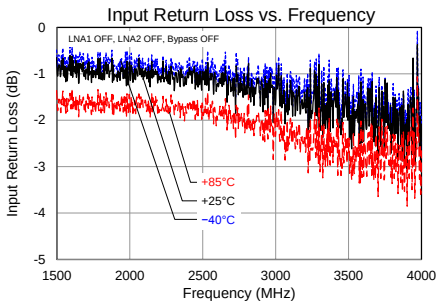
Output Return Loss vs. Frequency



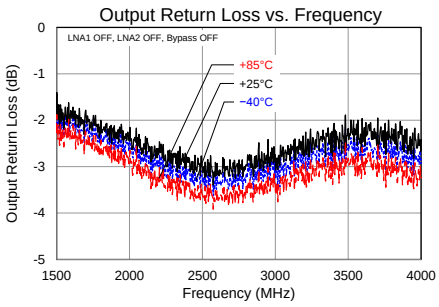
Gain vs. Frequency



Input Return Loss vs. Frequency

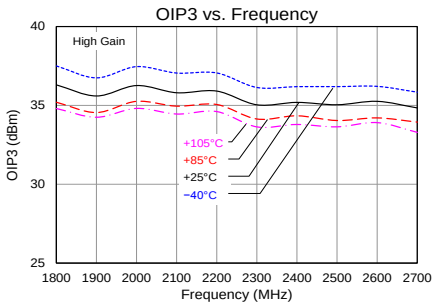


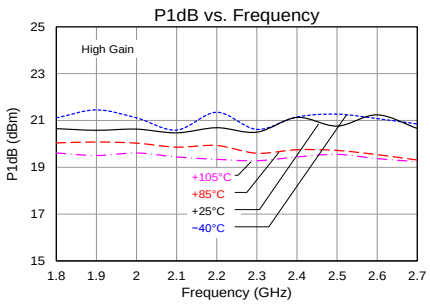
Output Return Loss vs. Frequency

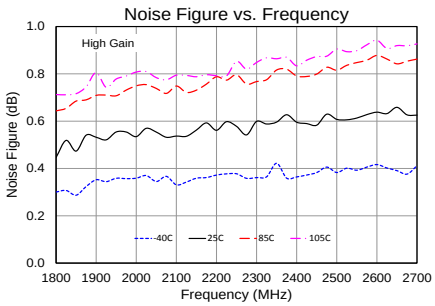


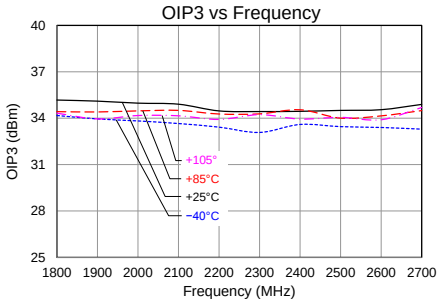
Performance Plots (cont.)

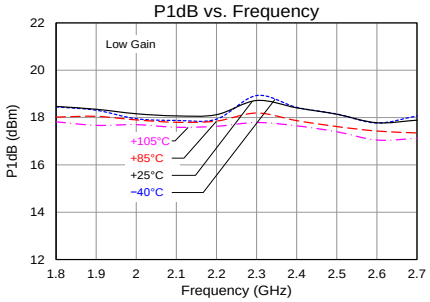
Test conditions unless otherwise noted: V_{DD1} = V_{DD2} = +5 V. Noise Figure de-embedded to device pins.

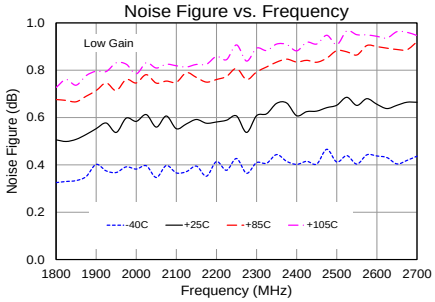




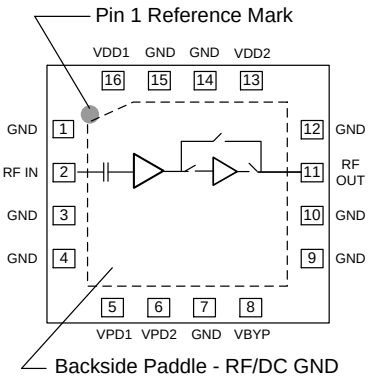








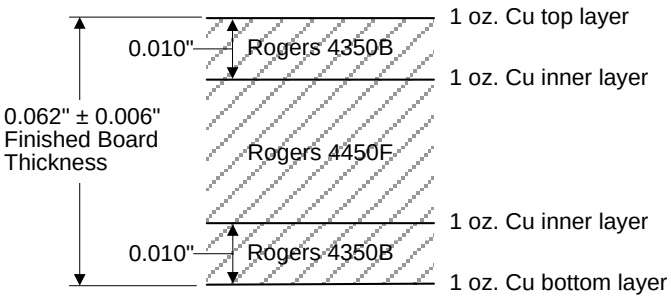
Pin Configuration and Description



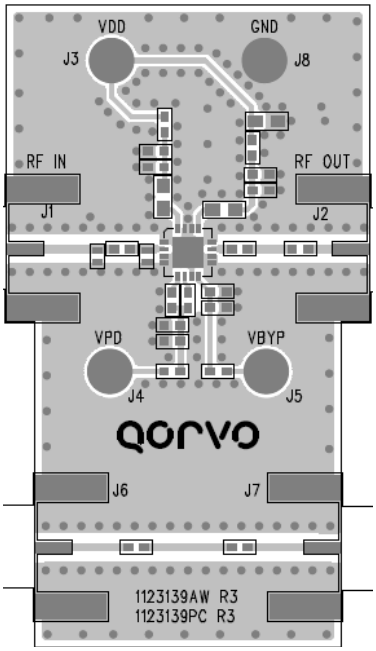
Pin No.	Label	Description
1,3,4,7,9,10,12,14,15	GND	RF/DC Ground pin.
2	RFin	RF input pin. Internally DC blocked.
5	V_{PD1}	Power Down control for LNA1. Refer to truth table on pg. 2.
6	V_{PD2}	Power Down control for LNA2. Refer to truth table on pg. 2.
8	V_{BYP}	Bypass mode enable pin for LNA2. Refer to truth table on pg. 2.
11	RFout	RF output pin. External DC block required.
13	V_{DD2}	Supply voltage pin for LNA2.
16	V_{DD1}	Supply voltage pin for LNA1.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

Qorvo PCB 1123139 Material and Stack-up



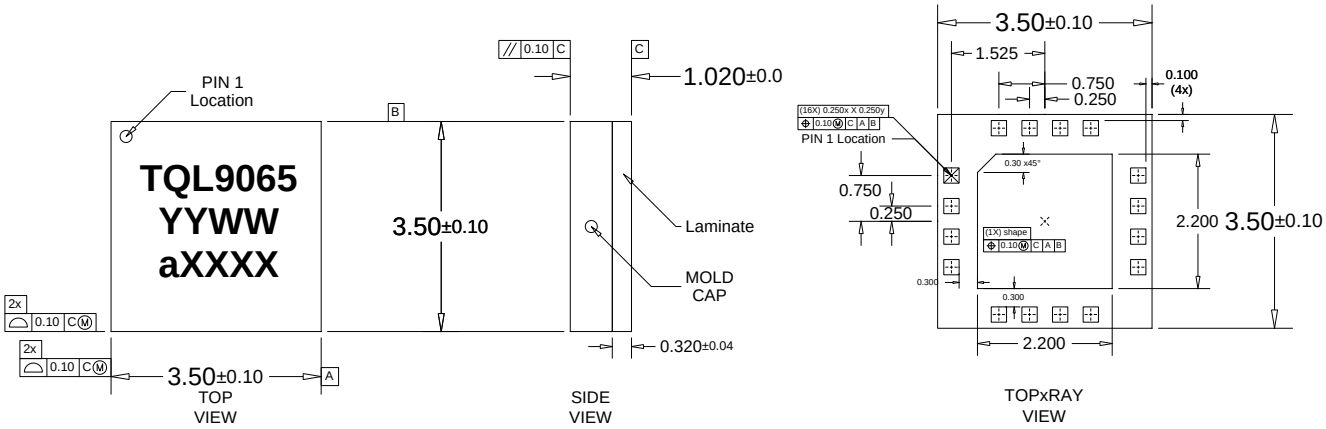
50 ohm line dimensions: width = .020”, spacing = .032”



Mechanical Information

Package Marking and Dimensions

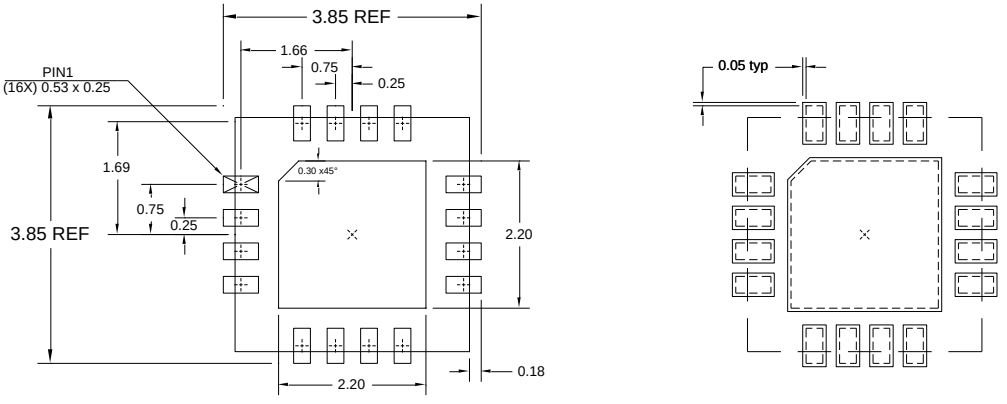
Marking: Part number – TQL9065
Year/Week – YYWW
Lot Code – aXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥250V to <500V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: Electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 877-800-8584**
Email: customer.support@qorvo.com

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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