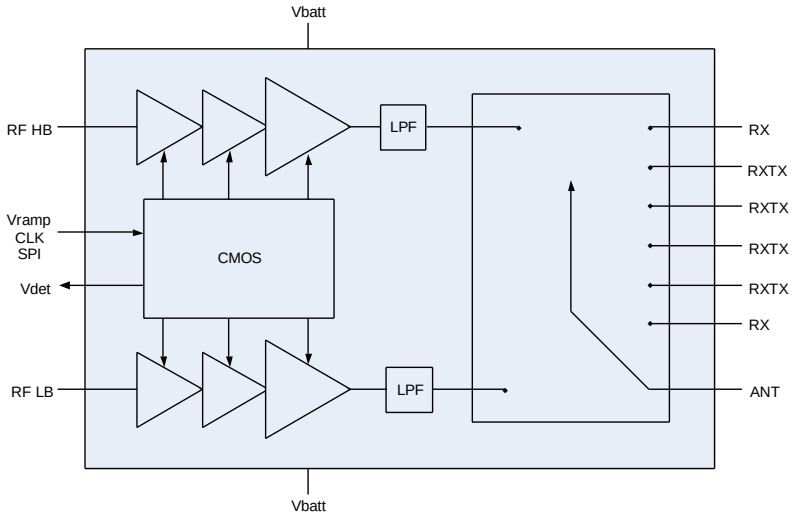
TRP-Enabled Quad-Band WEDGE Transmit Module

Functional Block Diagram



Product Description

This advanced quad-band multimode GSM / WEDGE Transmit Module with integrated multi-mode switch is designed for highly integrated next generation 3G and EDGE mobile handset applications and provides full RF transmit and multimode Tx/Rx-switch functionality in a size of only 52.5 mm^2. TQM6M9014 has been designed for stringent linearity requirements in next generation EDGE and 3G applications while maintaining high GSM / EDGE efficiency and receive sensitivity.

The transmit module supports full quad band GMSK / 8PSK transmit operation while providing Tx/Rx switch functionality with an integrated SP8T switch including four high linearity ports for 3G multi band operations.

Stringent linearity requirements are fulfilled with an integrated linear power detector with voltage output for closed loop APC operation in the overall phone system. By maintaining this linearity into a mismatch at the antenna port of the transmit module, this design is meeting so-called Transmitted Radiated Power (TRP) target specifications set by mobile phone network providers.

The CMOS controller provides full power amplifier and switch control and interfaces with the transceiver/ baseband unit through a Serial Programmable Interface.

Features

Highly Integrated GMSK / 8PSK WEDGE Transmit Module (PA & Switch).

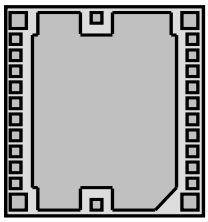
- Integrated SP8T switch with 4 high linearity ports for WCDMA.
- Integrated linear power detector with voltage output for closed loop APC operation.
- Fully aligned to market accepted 3G chipset.
- Meets stringent Transmitted Radiated Power specification.
- Serial Programmable Interface.
- Up to 75% duty cycle to support multi slot class 45 (6Tx /1Rx).
- 50 ohm input and output port impedance.
- Halogen Free product

Applications

- 3G handset and modem applications with various EDGE & WCDMA band combinations.

Package Style

LGA Package
- 7.0 x 7.5 x 1.1 mm³
- (+ / - 0.1 mm)
- 26 pins
- 1 Central Ground Plane



TRP-Enabled Quad-Band WEDGE Transmit Module

1. 1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
Vbatt	Positive Supply Voltage	Sleep Mode	-0.5 to 6.0	V
Vramp	Power Control Voltage		-0.5 to 3.0	V
Duty	Duty Cycle	Power reduction per 3GPP 45.005 Power Profile 2 = 4dB	75 (6 TX Slots)	%
	Output Load VSWR	All phases	20:1	
Tstorage	Storage Temperature		-55 to 125	°C
Tcase	Operating Case Temperature		-30 to 85	°C
Pin	Maximum input power	TX-LB, pin 25 TX-HB, pin 14 RX-L1, pin 3 RX-M3, pin 12 RXTX-L2, pin 5 RXTX-H, pin 7 RXTX-M1, pin 9 RXTX-M2, pin 11	10 10 10 10 30 30 30 30	dBm
Tmax	Peak Reflow Temperature		260	°C
MSL	Moisture Sensitivity Level	J_STD_020A	MSL3	

Note: The part may not survive all maximums applied simultaneously.

1.2 Standard Operating Conditions

Note: At startup and any time the power is interrupted the following SPI telegram must be entered:

SPI Trim Telegram: ***HEX 0102A0C9*** *or BIN:* ***000001 00000010 10100000 11001001*** *(30 bits)*

This sets the detector buffer gain to 0.9, from its default setting of 1.0 (see section 5.1.9)

TRP-Enabled Quad-Band WEDGE Transmit Module

Parameter (Units)	Symbol	Min	Typ	Max
Supply Voltage GMSK Mode(V)	Vbatt	3.2	3.4	4.2
Supply Voltage 8PSK Mode(V)	Vbatt	3.2	3.5	4.2
Vramp Voltage GMSK Mode(V)	Vramp	0.2		2.1
Vramp Voltage 8PSK Mode(V)	Vramp	0.2	See 2.3	2.1
Tx Input Power GMSK GSM850/900 (dBm)	Pin	3	6	9
Tx Input Power GMSK GSM1800/1900 (dBm)	Pin	3	6	9
Tx Frequency Range GSM850 (MHz)	Freq	824		849
Tx Frequency Range GSM900 (MHz)	Freq	880		915
Tx Frequency Range GSM1800 (MHz)	Freq	1710		1785
Tx Frequency Range GSM1900 (MHz)	Freq	1850		1910
RX-L1/RX-M3 Frequency Range (MHz)	Freq	869		1990
RX/TX-L2/RXTX-M1/RXTX-M2 Frequency Range (MHz)	Freq	824		1990
RXTX-H Frequency Range (MHz)	Freq	1710		2170
All RF Port Impedance (Ohm)	Zport		50	
Detector Input Impedance(Ohm)	Zdet		100k	
Duty Cycle (Period=4.616ms) %	Duty Cycle		25	
Operating Case Temp(deg C)	Tcase	-20	25	85

1. 3 General Characteristics

Parameter (units)	Target Spec		
	Min	Typ	Max
Digital Signal Current HI (uA)	0.1	1	100
Digital Signal Current LO (uA)	-0.1	0.1	100
Vramp Current (mA)	0	0.1	1
RX Mode Current (uA)	50	200	500
Leakage Current (uA)	1	10	35
Input Capacitance Digital and Analog Control Lines (pF)	1	3	5
RF Turn-on / Turn-off Time (us)	0.1	0.5	2
Mode Switching Time (us)	0.1	0.3	1
Bias Switching Time (us)	0.1	0.3	1
Switch Path Switching Time (us)	0.1	0.5	1
Switch Voltage Doubler Settling Time (us)	5	10	12

TRP-Enabled Quad-Band WEDGE Transmit Module

Parameter (units)	Target Spec			Special Test Conditions
	Min	Typ	Max	
V-SPI Voltage Range (V)	1.5	1.8	3.0	
V Logic Low input (V) (V-SPI > 1.7V)	-0.30		0.3*V-SPI	
V Logic High input (V) (V-SPI > 1.7V)	0.7*V-SPI		V-SPI +0.3V	
V Logic Low input (V) (V-SPI < 1.7V)	-0.30		0.2*V-SPI	
V Logic High input (V) (V-SPI < 1.7V)	0.8*V-SPI		V-SPI +0.3V	
SS & CLK Input Load (pF)	1		4	
DRW Input Load (pF)	1		5	
DRW Output Load (pF)	1		24	
Vramp Input R (kOhm)	20		50	
Vramp Input C (pF)	1		5	
Power Det Turn-on Time (us)	1		5	No input power, difference to fully settled detector output voltage (offset voltage) less than 1mV.

2. 1 Power Detector Characteristics

Parameter (units)		Target Spec		Special Test Conditions
		Min	Max	
Detector Output Range (V)		.03	2.75	RF On
Detector Offset Voltage (mV)		30	90	RF Off
Detector Output Impedance Active Mode (ohms)		500	1000	TX-EN “on”
Detector Output Impedance Idle Mode (M-ohms)		1	100	TX-EN “off”
Detector Sensitivity (mV/dB)	33dBm 20dBm 5dBm/0dBm (Low/High Band)	170 30 2	400 90 5	
Forward Power Variation into VSWR 3:1 (+/-dB)	Pmax 13dBm….Pmax 0dBm….13dBm	-0.5 -1.0 2.0	0.75 1.0 2.0	
Power Accuracy at fixed Detected Voltage (+/-dB)	Pmax 13dBm….Pmax 0dBm….13dBm	-0.5 -1.0 -2.0	0.5 1.0 2.0	Vdet=Vdet(25C)+kT x (85C-25C)

TRP-Enabled Quad-Band WEDGE Transmit Module

2. 2 APC Related Requirements

Parameter (units)	Target Spec		Special Test Conditions
	Min	Max	
GMSK Carrier Phase Shift (deg/dB)	1	10	Pout=Pmax-6dB…Pmax
GMSK Total Gain Variation Vramp/Vdet (%)	-50	50	Pout any value 0dBm…Pmax Referenced to 3.4V, 25C
GMSK Total Bandwidth Vramp/Vdet -3dB (MHz)	2	10	Pout=0dBm…Pmax-0.5dB
GMSK Pedestal Tolerance (dB)	-3	3	Pout Reference -10dBm at 3.4V, 25C, Pin=5dBm

2.3 8PSK BIAS Table

Transmit Band	Step Number	Power Range (dBm)	Minimum Vramp (V)
GSM 850/900	1	27.3	1.80
	2	26.3 to 22.2	1.60
	3	23.2 to 18.2	1.30
	4	19.2 to 14.2	1.00
	5	15.2 to 10.2	0.80
	6	11.2 to 7.2	0.65
	7	8.2 to MIN	0.60
GSM 1800/1900	1	26.5	1.65
	2	24.3 to 19.0	1.45
	3	21.0 to 17.0	1.10
	4	18.0 to 12.0	1.00
	5	13.0 to 8.0	0.90
	6	9.0 to 3.0	0.85
	7	4.0 to MIN	0.80

TRP-Enabled Quad-Band WEDGE Transmit Module

3. 1. 1 GSM850/900 GMSK Mode Electrical Characteristics

Standard Conditions: Vbatt=3.4V, Pin=+6 dBm, Tc=25°C

Parameter (units)		Target Spec			Special Test Conditions
		Min	Typ	Max	
Input VSWR	Pfwd>Pmax-3dB	1:1		2.0:1	
	Pfwd<Pmax-3dB	1:1		2.5:1	
	Idle Mode	1:1		6:1	
Forward Power (dBm)		32.8	34.0	37.0	3.4V, 25C
		32.3		33.3	3.4V, Load VSWR<3:1, Phase 90-300°
		32.0		37.0	3.2V, -20 to 85C, Pin= +3dBm
Efficiency (%)		37	41	60	3.4V, 32.8dBm, 25C
Battery Current under Output Mismatch (A)		0.2		2.1	Load VSWR=10:1
Battery Current at Low Output Power (mA)		20	85	120	Pfwd=5dBm
Spurious emissions under Mismatch Conditions (dBm)		-124		-36	Load VSWR<15:1 Temperature= -30 to 85C Pin= 0…+10dBm Input VSWR<2.5:1
Ruggedness under Mismatch Conditions		No Permanent Performance Degradation			Load VSWR<20:1 Temperature= -30 to 85C Pin= 0…+10dBm Input VSWR<2.5:1 Vbatt=4.2V Pout<32.8dBm at 50ohms
Output Noise Power (dBm)	869-894MHz	-124	-86	-84	Pfwd>5dBm Temperature= 25C 100kHz RBW
	925-935MHz	-124	-82	-73	
	935-960MHz	-124	-87	-85	
	1805-2170MHz	-124	-93	-77	
Harmonic Response (dBm)	2^{nd} 915MHz	-80	-40	-34	25C, Pout=32.8dBm
	2^{nd}…14^{th}	-80	-42	-35	Unused Ports Any Load
Harmonic Response Under Mismatch (dBm)	2^{nd}…4^{th}	-80		-31	Load VSWR<3:1 at fundamental
	5^{th}…14^{th}	-80		-15	Pout<32.8dBm at 50ohms
Forward Power in Idle Modes (dBm)					Unused Ports Any Load
PA and Switch Disabled		-80	-75	-40	Pin= -32dBm
PA Enabled Switch Disabled		-70	-50	-28	Pin= 9dBm, Vramp=0.2V
PA and Switch Enabled		-60	-30	-10	Pin= 9dBm, Vramp=0.2V
Vramp Slope (dB/V)		0	150	250	Pfwd=0dBm
Power Variation for constant Vramp (dB)		-0.5		0.5	Vbatt=constant

TRP-Enabled Quad-Band WEDGE Transmit Module

3. 1.2 GSM850/900 8PSK Mode Electrical Characteristics

Standard Conditions: Vbatt=3.5V, Tc=25°C

Parameter (units)	Target Spec			Special Test Conditions
	Min	Typ	Max	
Input VSWR	1:1		2.5	-40<Pin< -0.5dBm
Forward Power (dBm)	27.3		32.0	3.5V, 25C
	26.8		32.0	3.5V, 85C, Load VSWR<3:1
	26.3		32.0	3.2V, 25C, Load VSWR<3:1
	25.8		32.0	3.2V, 85C, Load VSWR<3:1
Forward Power Gain (dB)	28	31	34	3.5V, 25C
Forward Power Gain (dB)	27		35	3.2 to 4.2V, -20 to 85C
Forward Power Gain Variation Under Mismatch (dB)	-2		2	Load VSWR<3:1, relative to 1:1, 3.5V, 25C
Forward Power Gain Variation (dB)	-2.5		2.5	3.2 to 4.2V, -20 to 85C
Gain Variation during Burst (dB)	-0.3		0.3	
Efficiency (%)	16	18	30	3.5V, 27.3dBm
Battery Current under Output Mismatch (A)	0.2		2.1	Load VSWR 10:1
Battery Current at Low Output Power (mA)	20	110	125	Pfwd= 5dBm
ACPR @ offset (dBc) 200-400kHz 400-600kHz 600-1800kHz 1.8-3.0MHz 3.0-6.0MHz >6MHz	 -60 -80 -90 -95 -95 -95		 -32 -56 -62 -67 -69 -75	Load VSWR<3:1 Pfwd=26.8dBm for T= 85C Pfwd=26.3dBm for Vbatt= 3.2V Pfwd=25.8dBm for T=85C,Vbatt= 3.2V RBW=30kHz (f<=1.8MHz) RBW=100kHz (f>1.8MHz) Abs Limit -40dBm
400kHz ACPR (dBc)	-80	-64	-58	Pfwd=27.3dBm, 3.5V, 25C
EVM (%)	0	2.5	5	Pfwd=27.3dBm, 3.5V, 25C
EVM under Output Mismatch (%)	0		5.5	Load VSWR<3:1 Pfwd=26.8dBm for T= 85C Pfwd=26.3dBm for Vbatt= 3.2V Pfwd=25.8dBm for T=85C,Vbatt= 3.2V
Spurious emissions under Mismatch Conditions (dBm)	-124		-36	Load VSWR<15:1 Temperature= -20 to 85C Pin= -40…+6dBm Input VSWR<2.5:1

TRP-Enabled Quad-Band WEDGE Transmit Module

Ruggedness under Mismatch Conditions		No Permanent Performance Degradation			Load VSWR<20:1 Temperature= -30 to 85C Pin= -40…+6dBm Input VSWR<2.5:1 Vbatt= 4.2V Pout<27.3dBm at 50ohms
Output Noise Power (dBm)	869-894MHz 925-935MHz 935-960MHz 1805-2170MHz	-124 -124 -124 -124	-85 -85 -87 -85	-84 -79 -85 -77	Pfwd>5dBm Temperature= 25C 100kHz RBW
Harmonic Response (dBm)	2^{nd}…14^{th}	-80	-45	- 35	25C, Pout=27.3dBm Unused Ports Any Load
Harmonic Response Under Mismatch (dBm)	2^{nd}…4^{th} 5^{th}…14^{th}	-80 -80		-31 -15	Load VSWR<3:1
Forward Isolation (dBm) PA and Switch disabled PA Enabled Switch Disabled		 -80 -70	 -75 -65	 -43 -30	Unused Ports Any Load Pin= -32dBm Pin= 0.5dBm

3.2.1 GSM1800/1900 GMSK Mode Electrical Characteristics

Standard Conditions: Vbatt=3.4V, Pin=+6dBm, Tc=25°C

Parameter (units)		Target Spec			Special Test Conditions
		Min	Typ	Max	
Input VSWR	Pfwd>Pmax-3dB	1:1		2:1	
	Pfwd<Pmax-3dB	1:1		2.5:1	
	Idle Mode	1:1		6:1	
Forward Power (dBm)		30	32	35.0	3.4V, 25C
		29.5		35.0	3.4V, 25C, Load VSWR<3:1
		29.5		35.0	3.2V, -20 to 85C, Pin= +3dBm
Efficiency (%)		33	37	50	3.4V, 30dBm, 25C
Battery Current under Output Mismatch (A)		0.1		1.9	Load VSWR=10:1
Battery Current at Low Output Power (mA)		10	55	70	Pfwd=0dBm
Spurious emissions under Mismatch Conditions (dBm)		-124		-36	Load VSWR<15:1 Temperature= -30 to 85C Pin= 0…+10dBm Input VSWR<2.5:1
Ruggedness under Mismatch Conditions		No Permanent Performance Degradation			Load VSWR<20:1 Temperature= -30 to 85C Pin= 0…+10dBm Input VSWR<2.5:1 Vbatt=4.2V Pout<30.0dBm at 50ohms

Output Noise Power (dBm)	1805-1880MHz 1930-1990MHz 869-894MHz 925-935MHz 935-960MHz	-124 -124 -124 -124 -124	-84 -88 -92 -92 -91	-80 -80 -85 -73 -85	Pfwd>0dBm Temperature= 25C 100kHz RBW
Harmonic Response (dBm)	2^{nd}…7^{th}	-80	-40	-35	25C, Pout=30.0dBm Unused Ports Any Load
Harmonic Response Under Mismatch (dBm)	2^{nd}…3^{rd} 4^{th}…7^{th}	-80 -80		-31 -15	Load VSWR<3:1 at fundamental Pout<30.0dBm at 50ohms
Forward Power in Idle Modes (dBm) PA and Switch Disabled PA Enabled Switch Disabled PA and Switch Enabled		 -80 -70 -60	 -65 -40 -23	 -58 -30 -12	Unused Ports Any Load Pin= -32dBm Pin= 9dBm, Vramp=0.2V Pin= 9dBm, Vramp=0.2V
Vramp Slope (dB/V)		0	225	250	Pfwd= -5dBm
Power Variation for constant Vramp (dB)		-0.5		0.5	Vbatt=constant

3. 2. 2 GSM1800/1900 8PSK Mode Electrical Characteristics

Standard Conditions: Vbatt=3.5V, Tc=25°C

Parameter (units)	Target Spec			Special Test Conditions
	Min	Typ	Max	
Input VSWR	1:1		2.5:1	-40<Pin< -0.5dBm
Forward Power (dBm)	26.5		30.0	3.5V, 25C
	26.0		30.0	3.5V, 85C, Load VSWR<3:1
	25.5		30.0	3.2V, 25C, Load VSWR<3:1
	25.0		30.0	3.2V, 85C, Load VSWR<3:1
Forward Power Gain (dB)	31	34.5	37	3.5V, 25C
Forward Power Gain (dB)	30		38	3.2 to 4.2V, -20 to 85C
Forward Power Gain Variation Under Mismatch (dB)	-2		2	Load VSWR<3:1, relative to 1:1, 3.5V, 25C
Forward Power Gain Variation (dB)	-2.5		2.5	3.2 to 4.2V, -20 to 85C
Gain Variation during Burst (dB)	-0.3		0.3	
Efficiency (%)	18	22	30	3.5V, 26.5dBm
Battery Current under Output Mismatch (A)	0.1		1.9	Load VSWR 10:1
Battery Current at Low Output Power (mA)	10	75	85	Pfwd=0dBm

TRP-Enabled Quad-Band WEDGE Transmit Module

ACPR @offset (dBc)	200-400kHz 400-600kHz 600-1800kHz 1.8-3.0MHz 3.0-6.0MHz >6MHz	-60 -80 -90 -95 -95 -95		-32 -56 -62 -67 -69 -75	Load VSWR<3:1 Pfwd=26.0dBm for T= 85C Pfwd=25.5dBm for Vbatt= 3.2V Pfwd=25.0dBm for T=85C,Vbatt= 3.2V RBW=30kHz (f<=1.8MHz) RBW=100kHz (f>1.8MHz) Abs Limit -40dBm
400kHz ACPR (dBc)		-80	-62	-58	Pfwd=26.5dBm, 3.5V, 25C
EVM (%)		0	2	5	Pfwd=26.5dBm, 3.5V, 25C
EVM under Output Mismatch (%)		0		5.5	Load VSWR<3:1 Pfwd=26.0dBm for T= 85C Pfwd=25.5dBm for Vbatt= 3.2V Pfwd=25.0dBm for T=85C,Vbatt= 3.2V
Spurious emissions under Mismatch Conditions (dBm)		-124		-36	Load VSWR<15:1 Temperature= -20 to 85C Pin= -40…+6dBm Input VSWR<2.5:1
Ruggedness under Mismatch Conditions			No Permanent Performance Degradation		Load VSWR<20:1 Temperature= -30 to 85C Pin= -40…+6dBm Input VSWR<2.5:1 Vbatt= 4.2V Pout<26.5dBm at 50ohms
Output Noise Power (dBm)	1805-1880MHz 1930-1990MHz 869-894MHz 925-935MHz 935-960MHz	-124 -124 -124 -124 -124	-80 -81 -88 -88 -87	-77 -77 -85 -73 -85	Pfwd>0dBm Temperature= 25C 100kHz RBW
Harmonic Response (dBm)	2^{nd}…7^{th}	-80	-50	-35	25C, Pout= 30dBm Unused Ports Any Load
Harmonic Response Under Mismatch (dBm)	2^{nd}…3^{rd} 4^{th}…7^{th}	-80 -80		-31 -15	Load VSWR<3:1 at fundamental
Forward Power in Idle Modes (dBm) PA and Switch Disabled PA Enabled Switch Disabled		 -80 -70	 -66 -55	 -55 -35	Unused Ports Any Load Pin= -32dBm Pin = 0.5dBm

TRP-Enabled Quad-Band WEDGE Transmit Module

3. 3 GSM RX / UMTS Operation Characteristics

Parameter (units)		Target Spec			Special Test Conditions
		Min	Typ	Max	
VSWR RXTX / ANT Ports		1:1	1.35	1.5:1	
In-Band Ripple all RX and RXTX Ports (dB)		-0.2		0.2	Pout=Pmax 6TX/1RX
Isolation (dB)	RX-RXTX	24		60	824-960MHz
		18		60	1710-2170MHz
	RXTX-RXTX	25		60	824-960MHz
		18		60	1710-2170MHz
	ANT-RX	24		60	824-960MHz
		20		60	1710-2170MHz
	ANT-RXTX	25		60	824-960MHz
		20		60	1710-2170MHz
Generated Harmonics (dBm)		-80	-70	-45	Pin=25dBm

4.1 Antenna Switch Characteristics

4.1.1 Insertion loss

Item	Path	Conditions	Vbatt (V)	Temp (°C)	Min	Typ	Max	Units
Insertion Loss	ANT / RX-L1	869 MHz – 960 MHz	3.4	25	0.2	0.9	1.2	dB
		869 MHz – 960 MHz	3.2	85	0.2	1.1	1.3	
		1805 MHz – 1990 MHz	3.4	25	0.2	1.5	1.8	
		1805 MHz – 1990 MHz	3.2	85	0.2	1.7	2.0	
	ANT / RXTX-L2	824 MHz - 960 MHz	3.4	25	0.2	0.7	0.8	dB
		824 MHz - 960 MHz	3.2	85	0.2	0.8	0.95	
		1710 MHz - 1990 MHz	3.4	25	0.2	1.0	1.1	
		1710 MHz - 1990 MHz	3.2	85	0.2	1.2	1.3	
	ANT / RXTX-H	1710 MHz - 1980 MHz	3.4	25	0.2	0.9	1.1	dB
		1710 MHz - 1980 MHz	3.2	85	0.2	1.0	1.2	
		1980 MHz - 2170 MHz	3.4	25	0.2	1.0	1.2	
		1980 MHz - 2170 MHz	3.2	85	0.2	1.2	1.35	
	ANT / RXTX-M1	824 MHz - 960 MHz	3.4	25	0.2	0.6	0.8	dB
		824 MHz - 960 MHz	3.2	85	0.2	0.7	0.95	
		1710 MHz - 1990 MHz	3.4	25	0.2	0.9	1.1	
		1710 MHz - 1990 MHz	3.2	85	0.2	1.1	1.3	
	ANT / RXTX-M2	824 MHz - 960 MHz	3.4	25	0.2	0.6	0.8	dB
		824 MHz - 960 MHz	3.2	85	0.2	0.7	0.95	
		1710 MHz - 1990 MHz	3.4	25	0.2	0.9	1.1	
		1710 MHz - 1990 MHz	3.2	85	0.2	1.1	1.3	
	ANT / RX-M3	869 MHz - 960 MHz	3.4	25	0.2	0.9	1.1	dB
		869 MHz - 960 MHz	3.2	85	0.2	1.0	1.25	
		1805 MHz - 1990 MHz	3.4	25	0.2	1.3	1.6	
		1805 MHz - 1990 MHz	3.2	85	0.2	1.5	1.75	

TRP-Enabled Quad-Band WEDGE Transmit Module

4.1.2 IIP2

Item	F_{Tx} (MHz)	$F_{blocker}$ (MHz)	F_{Rx} (MHz)	Impedance			Port	Min (@F_{Rx})	Max	units
				Mag @Fblock	Phase@blocker					
				50 Ohm	DEG					
				Max	Min	Max				
Band I Low IIP2	1920 - 1980	190	F_{Tx} + 190	0.92	135	260	RXTX-M1	104	150	dBm
							RXTX-H	104	150	
Band I High IIP2		2*F_{Tx} + 190	F_{Tx} + 190	0.60	0	360	RXTX-M1	104	150	dBm
							RXTX-H	104	150	
Band II Low IIP2	1850 - 1910	80	F_{Tx} + 80	0.92	90	350	RXTX-M1	104	150	dBm
							RXTX-H	104	150	
Band II High IIP2		2*F_{Tx} + 80	F_{Tx} + 80	0.50	0	360	RXTX-M1	104	150	dBm
							RXTX-H	104	150	
Band V Low IIP2	824 - 849	45	F_{Tx} + 45	0.92	40	360	RXTX-L2	104	150	dBm
							RXTX-M2	104	150	
Band V High IIP2		2*F_{Tx} + 45	F_{Tx} + 45	0.67	0	360	RXTX-L2	104	150	dBm
							RXTX-M2	104	150	
Band VIII Low IIP2	880 - 915	45	F_{Tx} + 45	0.92	45	360	RXTX-L2	104	150	dBm
							RXTX-M2	104	150	
Band VIII High IIP2		2*F_{Tx} + 45	F_{Tx} + 45	0.67	0	360	RXTX-L2	104	150	dBm
							RXTX-M2	104	150	

*FTx picked to be worst case in band, PTx = 20.5 dBm Pblocker= -15.5 dBm referenced at ANT

*Ports RXTXH and RXTXM1 are optimized for high band performance
*Ports RXTXL2 and RXTXM2 are optimized for low band performance

TRP-Enabled Quad-Band WEDGE Transmit Module

4.1.3 IIP3

Item	F_{Tx} (MHz)	$F_{blocker}$ (MHz)	F_{Rx} (MHz)	Impedance				Port	Min (@F_{Rx})	Max	units
				Mag @Fblock 50Ohm		Phase@Fblock DEG					
				Max		Min	Max				
Band I IIP3	1920-1980	F_{Tx} - 190	F_{Tx} + 190	0.7		95	205	RXTX-M1	65	90	dBm
								RXTX-H	65	90	
Band II IIP3	1850-1910	F_{Tx} - 80	F_{Tx} + 80	0.6		80	200	RXTX-M1	65	90	dBm
								RXTX-H	65	90	
								RXTX-H	65	90	
Band V IIP3	824-849	F_{Tx} - 45	F_{Tx} + 45	0.75		30	125	RXTX-L2	65	90	dBm
								RXTX-M2	65	90	
								RXTX-M2	65	90	
Band VIII IIP3	880-915	F_{Tx} - 45	F_{Tx} + 45	0.7		35	120	RXTX-L2	65	90	dBm
								RXTX-M2	65	90	
								RXTX-M2	65	90	

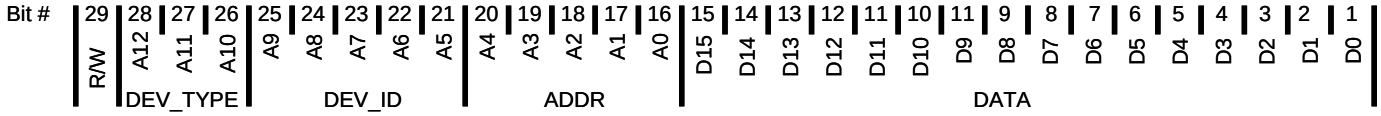
PTx = 20.5 dBm Pblocker= -15.5 dBm referenced at ANT, FTx picked to be worst case in band

*Ports RXTXH and RXTXM1 are optimized for high band performance
*Ports RXTXL2 and RXTXM2 are optimized for low band performance

TRP-Enabled Quad-Band WEDGE Transmit Module

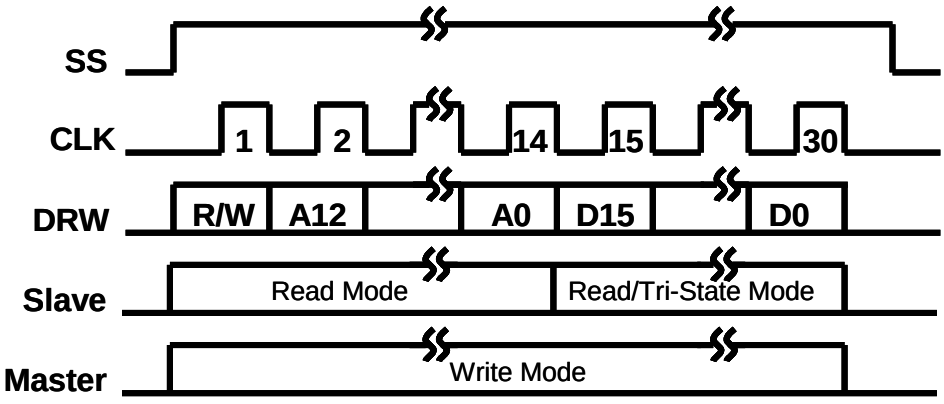
5. 0 Serial Peripheral Interface (SPI)

5.1 SPI data structure



Address Bits A12…A0 are used to select a particular slave and register address within the TX-Module:
DEV_TYPE bits A12…A10 = Device type = (0,0,0) for TX-Module
DEV_ID bits A9…A5 = Supplier ID
ADDR bits A4…A0 = Register Address = (0,0,0,0,0) for Control Register
DATA bits D15…D0 are used for writing data to the TX-Module

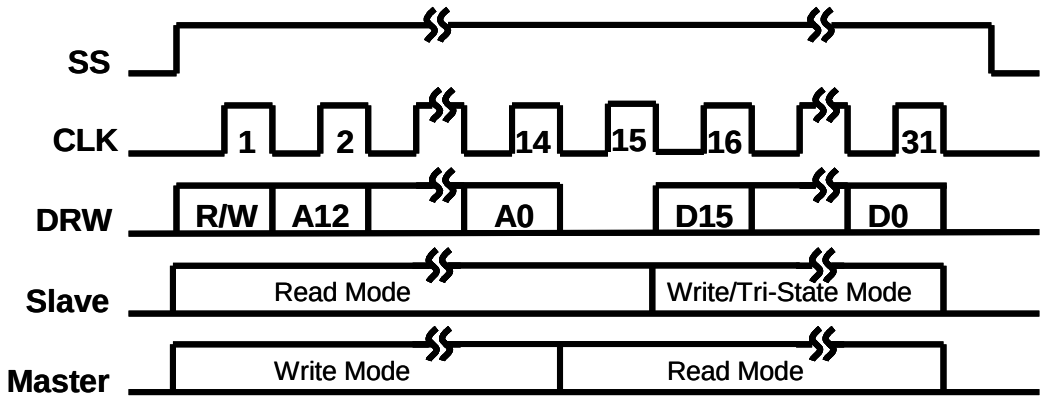
5.1.1 Write Protocol



When the R/W bit is “0” the Tx-Module latches data into the specified address register on falling edge od SS if a clock count of 30 is obtained.Data is ignored if clock count is other than 30.

TRP-Enabled Quad-Band WEDGE Transmit Module

5.1.2 Read Protocol



When the R/W bit is "1" the TX-Module reads the address and returns data 1 clock cycle after the final address bit is received. A total of 31 clock cycles is required to read back 16 bits of data.

5.1.3 Timing

Data is presented on the CLK falling edge and latched on CLK rising edge. Data set-up and hold time is 11.9ns (min) relative to CLK rising edge. SS set-up time is 19.2nS (min) from rising edge of SS to rising edge of first clock cycle. SS hold time is 19.2ns (min) from falling edge of last clock cycle to falling edge of SS. SPI readback propagation delay is 9ns (max) from rising edge of data, DRW rise/fall time is 5ns (max) into a 24pf load. A minimum of one clock cycle turnaround is expected for consecutive write and/or read operations.

5.1.4 Broadcast Mode

When a write command is received with address bits A15…A0 set to all 1's, the TX-Module reverts to the sleep state. Similarly, when V-SPI supply or Vbatt supply are applied, the TX-Module reverts to the sleep state.

5.1.5 Adress and Data Bit Definitions

R/W = 0: Write data to slave
R/W = 1: Read data from slave
Address bits A12…A10 = Device type = (0,0,0) for TX-Module
Address bits A9…A5 = Supplier ID = (0,1,0,0,0) for TriQuint
Address bits A4…A0 = Read/Write Register Address
Data bits are D15…D0

TRP-Enabled Quad-Band WEDGE Transmit Module

5.1.6 Register Map

All Registers can be written to or read from. Some data bits are hard-wired and cannot be changed by write operation. These bits will always read back "0" and are noted in the Register Bit Definitions sections.

Address 00000 is the Write Register. Transceiver writes to TX Module.
Address 00001 is the Read Register. TX Module reads back to Master
Address 00010 is the Trim Register. Transceiver writes Sensor trim values to TX Module

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00000	FE Boost	FE Select				Sensor Config		Reserved	Tempco Trim		Current Sensor Config			TXEN	PA Mode	Band Select
00001	Reserved						Curr Sns response	Reserved				PA temp		Reserved		
00010	Temp threshold 2		Temp threshold 1		Test Mode		Icc summing gain		Vdet trim		Icc sense gain change		Det offset		Summing gain change	

5.1.7 Read Register Adress 00001 Bit Definitions

Bits	Name/Meaning
D15:D10	**Reserved**
000000	Hardwired
D9	**Current Sensor Read back**
0	Sensor Inactive
1	Sensor Active
D8:D5	**Reserved**
0000	Hardwired
D4:D3	**PA Temp**
00	Temp < T1
01	T1<Temp<T2
10	Reserved
11	Temp>T2
D2:D0	**Reserved**
000	Hardwired

5.1.8 Write Register Adress 00000 Bit Definitions

Bits	Name/Meaning	Default
D15	**Voltage Doubler**	
0	Doubler Off	X
1	Doubler On	
D14:D11	**Front End Status**	
0000	SLEEP	X
0001	TX-M	
0010	TX-L	
0011	reserved	
0100	RXTX-M2	
0101	RX-L1	
0110	RX-M3	
0111	reserved	
1000	RXTX-L2	
1001	RXTX-M1	
1010	RXTX-H	
1011	reserved	
1100	reserved	
1101	reserved	
1110	reserved	
1111	reserved	
D10:D9	**Sensor Configuration**	
00	Analog Feedback Off	X
01	Analog Icc Sensor OFF	
10	Analog Icc Sensor ON	
11	Analog Icc Sensor ON	
D8	**Reserved**	
D7:D6	**Vcc Tempco Trim**	
00	0	X
01	-10%	
10	-+10%	
11	Reserved	

Continued

D5:D3	Current Sensor Configuration		
	GMSK	8PSK	
000	1.55 A	600 mA	
001	1.65 A	700 mA	
010	1.75 A	800 mA	
011	1.85 A	900 mA	
100	1.95 A	1.0 A	X
101	2.05 A	1.1 A	
110	2.15 A	1.2 A	
111	2.25 A	1.3 A	
D2	**Tx Enable**		
0	PA Off		X
1	PA On		
D1	**Mode Select**		
0	GMSK		X
1	8PSK		
D0	**Band Select**		
0	Low Band		X
1	High Band		

5.1.9 Trim Register Adress 00010 Bit Definitions

Bits	Name/Meaning	Default
D15:14	**T2 Temp Threshold**	
00	105 degC	
01	115 degC	
10	125 degC	X
11	135 degC	
D13:D12	**T1 Temp Threshold**	
00	95 degC	
01	105 degC	
10	115 degC	X
11	125 degC	
D11:D10	**Test Mode**	
00	Open	X
01	V(Icc)	
10	Reserved	
11	V(Vtemp)	

Continued

D9:D8	Icc Sum Gain	
00	0.3	X
01	0.5	
10	0.8	
11	1.0	
D7:D6	**Vdet trim**	
00	2.45	
01	2.55	
10	2.65	
11	2.75	X
D5:D4	**Icc Term Resistor**	
00	33%	X
01	50%	
10	100%	
11	200%	
D3:D2	**DET Offset Voltage**	
00	40mV	
01	50mV	
10	60mV	X
11	70mV	
D1:D0	**DET Buffer Gain**	
00	0.8	
01	0.9	
10	1.0	X
11	1.2	

TRP-Enabled Quad-Band WEDGE Transmit Module

SPI Overview (Adress and data fields)

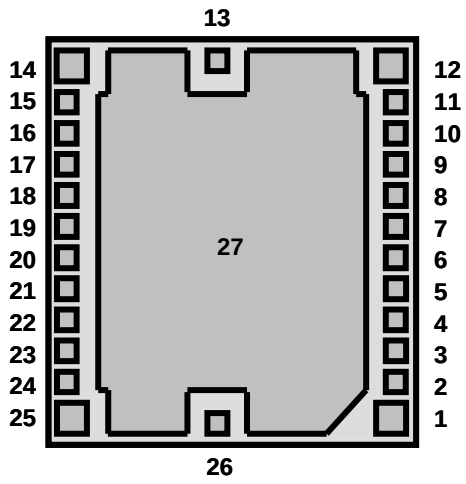
29	28	27	26	25	24	23	22	21	20	19	18	17	16
A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
R/W	Adress (Slave type)			Adress (slave identifier)					Register adress				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data bits															

TRP-Enabled Quad-Band WEDGE Transmit Module

6. 1 Pin Out and Assignments

PIN	SYMBOL	PORT DESCRIPTION
1	ANT	Antenna
2, 4, 6, 8, 10, 15, 24, 27	GND	Ground
3	RX-L1	GSM850/900 Receive
5	RXTX-L2	GSM850/900 Receive WCDMA Band V/VIII Transmit/Receive
7	RXTX-H	WCDMA Band I Transmit/Receive
9	RXTX-M1	GSM1800/1900 Receive WCDMA Band II/III Transmit/Receive
11	RXTX-M2	WCDMA Band V/VIII Transmit/Receive
12	RX-M3	GSM 1800/1900 Receive
13	Vbatt-HB	GSM1800/1900 Q3 Battery Input
14	TX-HB	GSM1800/1900 RF Input
16	RAMP	GMSK Ramping/Bias Control Voltage 8PSK Bias Control Voltage
17	V-CMOS	Analog Section Battery Input
18	GND-SPI	Digital Section Ground
19	V-SPI	Digital Section 1.8V Input
20	CLK	Clock Input
21	DRW	Data Read / Write
22	SS	Slave Select
23	DET	RF Detector Voltage Output
25	TX-LB	GSM850/900 RF Input
26	Vbatt-LB	GSM850/900 Q3 Battery Input



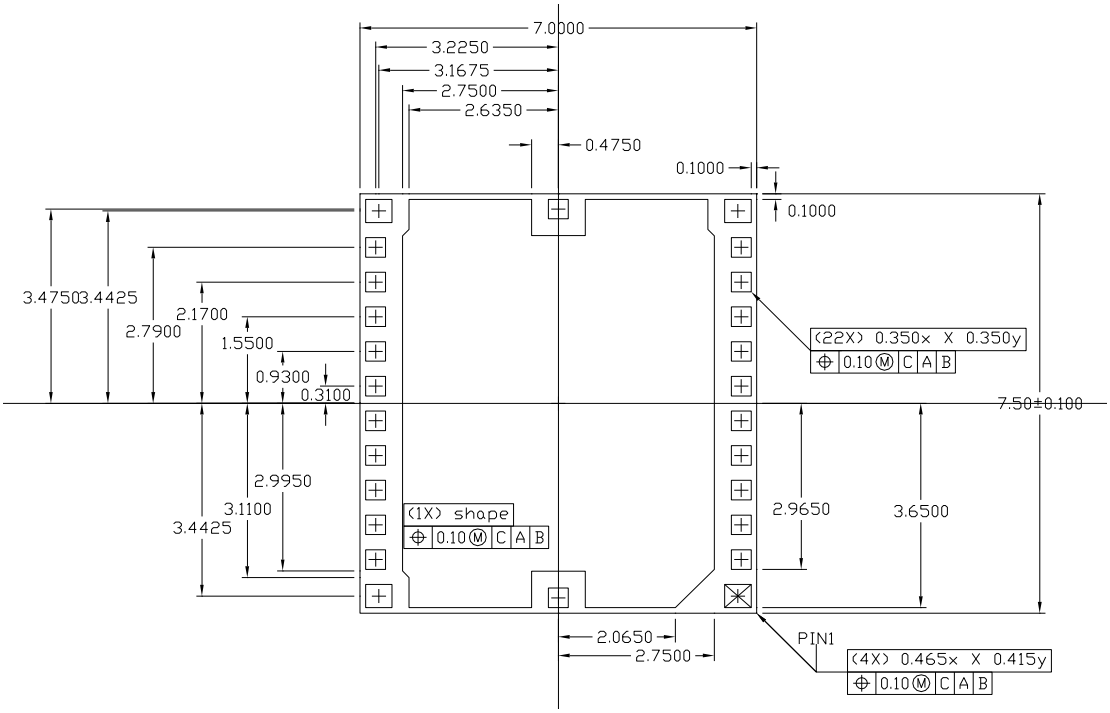
Top View

6. 2 Marking

TriQuint Logo
Product name
YY= production year WW= production week, CCCC= Country code
Aa = Assembly vendor, XXXX= TriQuint Assembly Number

TRP-Enabled Quad-Band WEDGE Transmit Module

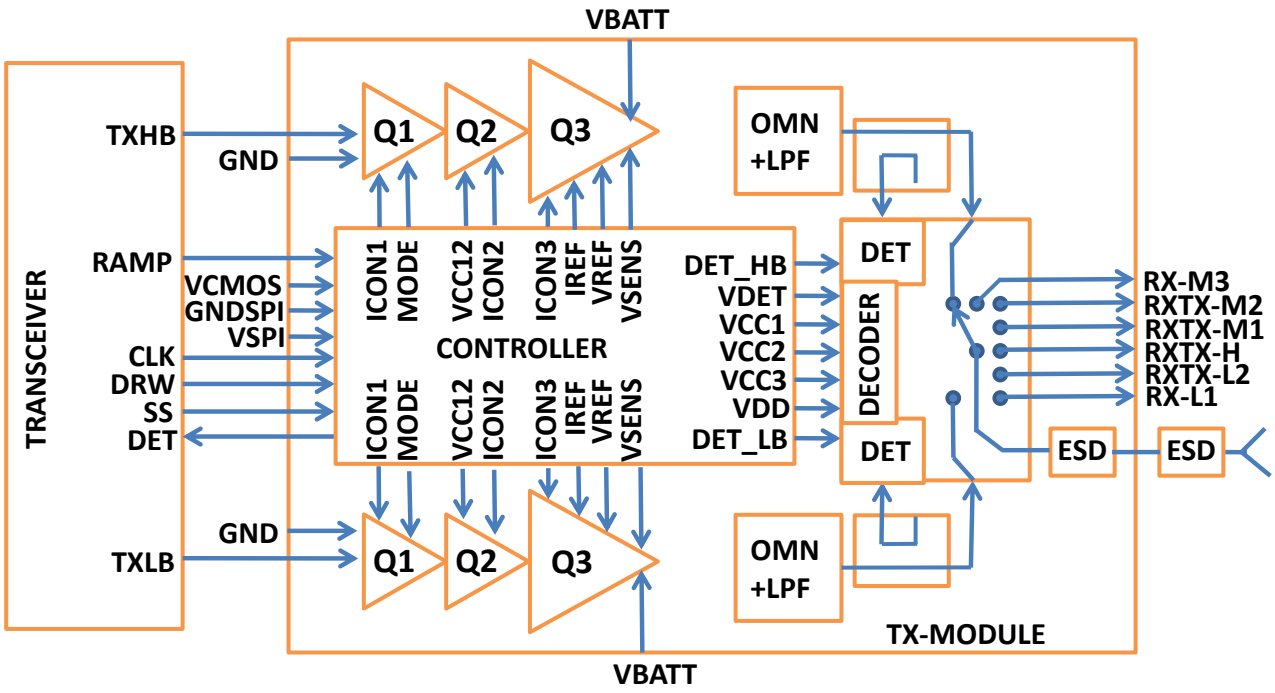
6. 3 Package Drawing:



Top view, looking through package

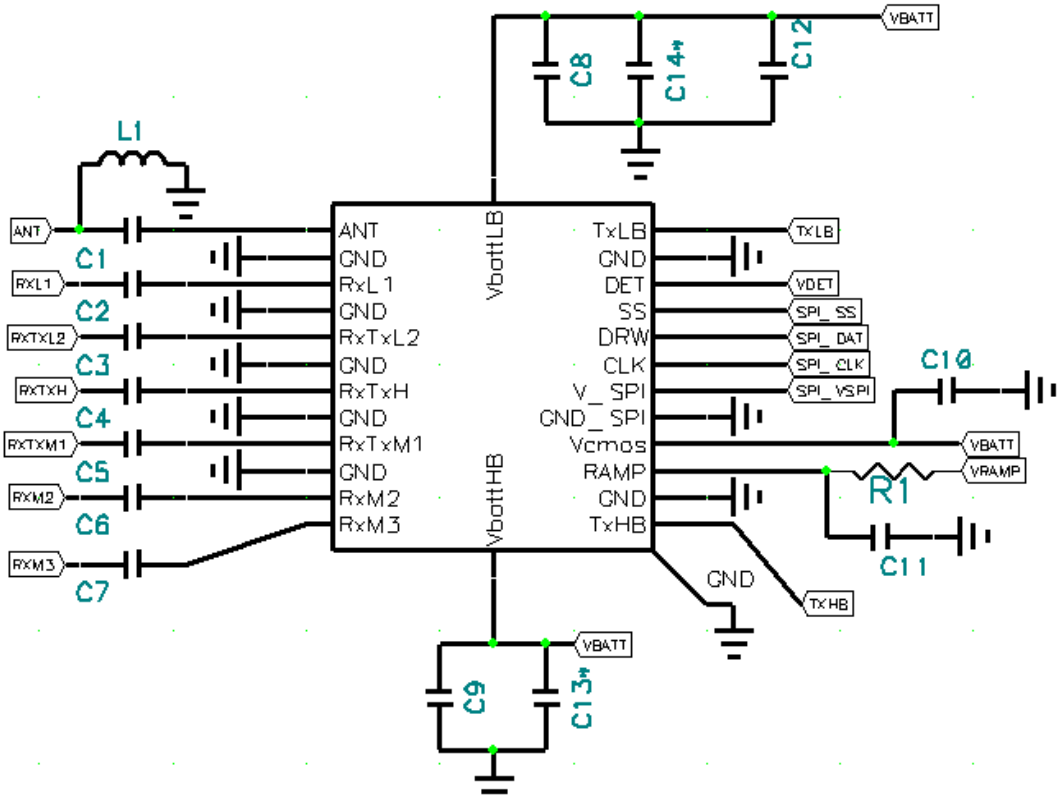
TRP-Enabled Quad-Band WEDGE Transmit Module

7.1 Functional Block diagram



TRP-Enabled Quad-Band WEDGE Transmit Module

Recommended Handset Level Schematic and Layout Considerations



Part	Value	Comment
C1	33pF	DC Block and ESD Cap in conjunction with L1
C2,C3,C4C5, C6,C7	100pF	DC Block Cap
C8,C9,C10	0.01uF	Low frequency bypass capacitor of 3rd stage PA(LB,HB) and CMOS
R1,C11	10kOhm, 150pF	Default setting of Ramp low pass filter. Needs to be changed depending on sampling frequency of base band IC (see page 5)
C12	10uF	Main low frequency bypass capacitor of Battery line
C13*	18p	Optional for HB leakage bypass
C14*	47pF	Optional for LB leakage bypass
L1	27nH	External ESD improvement inductor in conjunction with C1

TRP-Enabled Quad-Band WEDGE Transmit Module

Additional Information [1]

This part is compliant with RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

1 For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**

Email: info_wireless@tqs.com **Fax: (503) 615-8902**

For technical questions and additional information on specific applications:

Email: info_wireless@tqs.com