

# TQP369181

## DC-6 GHz Gain Block

### Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- CATV
- Point to Point
- General Purpose Wireless

### Product Features

- DC-6000 MHz
- 15.3 dB Gain @ 1.9 GHz
- 3.6 dB Noise Figure @ 1.9 GHz
- +28.7 dBm Output IP3
- +14.4 dBm P1dB
- 50 Ohm Cascadable Gain Block
- +5V Single Supply, 45 mA Current
- SOT-363 Package

### General Description

The TQP369181 is a general-purpose buffer amplifier that offers high dynamic range in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 15.3 dB gain, +28.7 dBm OIP3, and 3.6 dB Noise Figure while drawing 45 mA current. The device combines dependable performance with consistent quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The device is housed in a lead-free/green/RoHS-compliant industry-standard SOT-363 package.

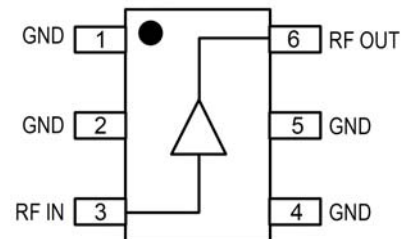
The TQP369181 consists of a Darlington-pair amplifier using the high reliability InGaP/GaAs HBT process technology. Only DC-blocking capacitors, a bias resistor, and an inductive RF choke are required for operation.

This broadband MMIC amplifier can be directly applied to various current and next generation wireless technologies such as CDMA, W-CDMA, and LTE. In addition, the TQP369181 will work for other applications within the DC to 6 GHz frequency range.



SOT-363 Package

### Functional Block Diagram



### Pin Configuration

Pin #	Symbol
3	RF IN
6	RF OUT
1, 2, 4, 5	GND

### Ordering Information

Part No.	Description
TQP369181	InGaP/GaAs HBT Gain Block
TQP369181-PCB	0.5-4 GHz Evaluation Board

Standard T/R size = 3000 pieces on a 7" reel

### Specifications

#### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, CW, 50 Ω, T=25°C	+27 dBm
Device Voltage, V <sub>device</sub>	5.2 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

#### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
T <sub>case</sub>	-40		+85	°C
T <sub>j</sub> (for >10 <sup>6</sup> hours MTTF)			+160	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

#### Electrical Specifications

Test conditions unless otherwise noted: V<sub>SUPPLY</sub> = 5 V, R<sub>BIAS</sub> = 24 Ω, I<sub>CC</sub> = 45 mA, T<sub>CASE</sub> = +25°C, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		DC		6000	MHz
Test Frequency			1900		MHz
Gain			15.3		dB
Input Return Loss			-30		dB
Output Return Loss			-24		dB
Output P1dB			+14.6		dBm
Output IP3	See Note 1.		+28.7		dBm
Noise Figure			3.6		dB
Device Voltage, V <sub>device</sub>			3.9		V
Current, I <sub>cc</sub>			45		mA
Thermal Resistance (jnc to case) θ <sub>jc</sub>				226	°C/W

Notes:

1. OIP3 is measured with two tones at an output power of 0 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule. 2:1 rule gives relative value with respect to fundamental tone.

# TQP369181

## DC-6 GHz Gain Block



### Device Characterization Data

#### S-Parameter Data

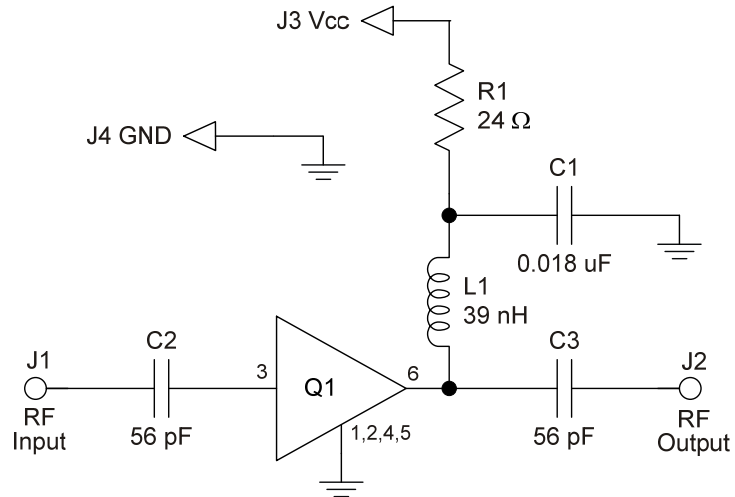
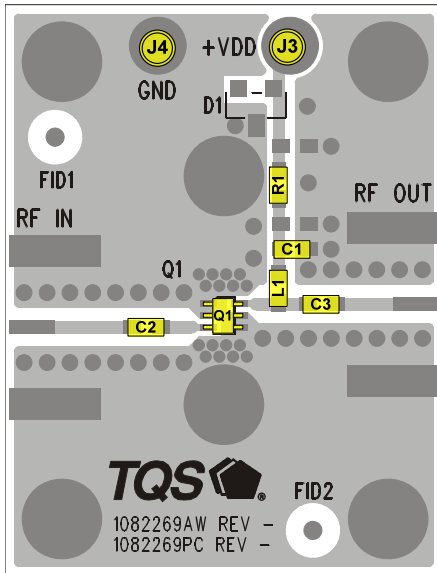
$V_{\text{device}} = 3.9 \text{ V}$ ,  $I_{\text{cc}} = 45 \text{ mA}$ ,  $T_{\text{case}} = +25^\circ \text{ C}$ , unmatched 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-34.9	-4.3	15.9	179.8	-18.8	0.7	-24.1	7.2
20	-35.9	-7.4	16.0	179.3	-18.9	-0.1	-24.1	1.6
50	-37.1	-12.6	16.0	179.0	-18.7	-0.3	-24.1	-2.2
100	-36.9	-8.6	16.0	176.6	-18.7	-1.8	-24.0	-7.0
200	-36.2	-8.6	16.0	173.6	-18.6	-3.1	-23.8	-11.3
500	-35.3	-24.9	16.0	163.6	-18.8	-8.3	-24.0	-31.8
1000	-39.4	-83.8	15.9	146.9	-18.7	-17.7	-24.2	-60.0
1500	-34.7	-158.5	15.9	130.2	-18.8	-26.0	-23.1	-105.9
2000	-28.7	167.6	15.9	113.9	-18.8	-35.4	-21.4	-136.7
2500	-25.1	149.8	15.8	97.0	-18.8	-43.8	-19.0	-170.4
3000	-22.1	138.8	15.7	80.4	-18.8	-52.6	-16.8	167.9
3500	-20.2	123.6	15.5	63.6	-19.0	-61.7	-14.8	145.4
4000	-18.0	114.6	15.4	46.5	-19.1	-70.5	-12.8	130.0
4500	-16.8	107.1	15.1	29.3	-19.1	-79.8	-11.6	116.9
5000	-15.2	97.9	14.9	11.8	-19.4	-89.7	-10.6	101.3
5500	-14.5	91.0	14.7	-5.7	-19.6	-98.1	-9.7	89.3
6000	-13.3	83.4	14.2	-23.3	-19.6	-108.6	-9.1	77.7

# TQP369181

## DC-6 GHz Gain Block

### Application Circuit Configuration



**Notes:**

1. See PC Board Layout, under Application Information section, for more information.
2. All components are of 0603 size unless otherwise stated.

### Bill of Material: TQP369181-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
Q1	n/a	High Linearity LNA Gain Block	TriQuint	TQP369181
C1	0.018 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C2, C3	56 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
L1	39 nH	Inductor, 0603, 5%, CS Series	Coilcraft	
R1	24 Ω	Res, Chip, 0805, 1/10W, 5%	various	

### Component Values for Specific Frequencies

Use the component values in this table for optimal operation at specific frequencies.

Reference Designator	Frequency (MHz)						
	50	500	900	1900	2200	2500	3500
L1	820 nH	220 nH	68 nH	27 nH	22 nH	18 nH	15 nH
C2, C3	.018 uF	1000 pF	100 pF	68 pF	68 pF	56 pF	39 pF

### Bias Resistor Values for Various Supply Voltages

Select R1 to satisfy 45 mA operating current at the available supply voltage.

	V <sub>supply</sub> (Volts)						
	5	6	7	8	9	10	12
R1 Value	24 Ω	47 Ω	68 Ω	91 Ω	110 Ω	130 Ω	180 Ω
Size	0805	1206	1210	1210	1210	2010	2010

# TQP369181

## DC-6 GHz Gain Block



### Typical Performance TQP369181-PCB

Test conditions unless otherwise noted:  $V_{\text{supply}} = 5 \text{ V}$ ,  $R_{\text{bias}} = 24 \Omega$ ,  $I_{\text{cc}} = 45 \text{ mA}$ ,  $T_{\text{case}} = +25^\circ \text{C}$

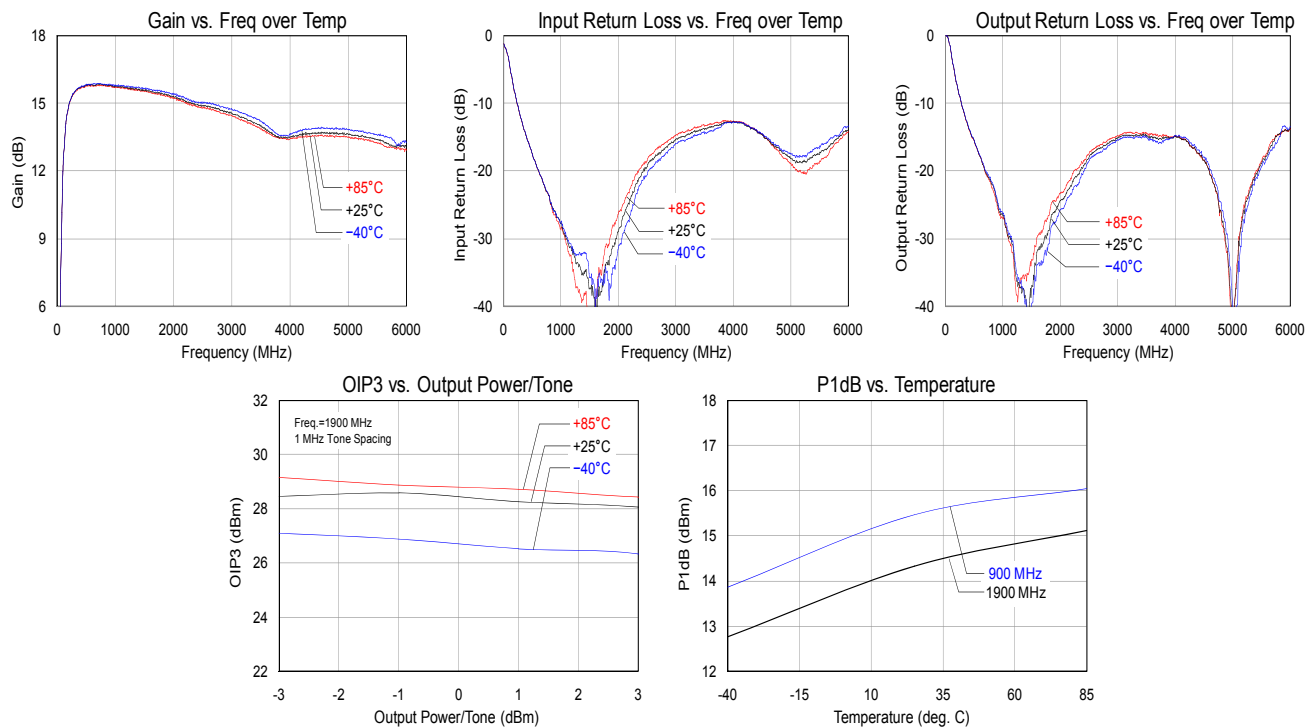
Frequency	MHz	500	900	1900	2100	2600
Gain	dB	15.6	15.6	15.3	15	14.7
Input Return Loss	dB	-17	-26	-30	-24	-17
Output Return Loss	dB	-16	-24	-24	-20	-16
Output P1dB	dBm	+15.4	+15.2	+14.6	+14.3	+14.0
OIP3 [1]	dBm	+30.6	+30.0	+28.7	+28.5	+27.7
Noise Figure	dB	3.6	3.6	3.6	3.6	3.7

Notes:

- OIP3 measured with two tones at an output power of 0 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

### Performance Plots

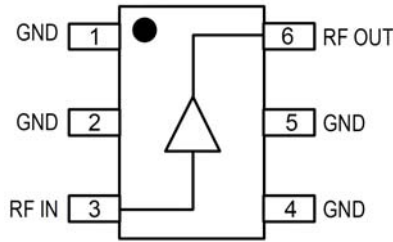
Test conditions unless otherwise noted:  $V_{\text{supply}} = 5 \text{ V}$ ,  $R_{\text{bias}} = 24 \Omega$ ,  $I_{\text{cc}} = 45 \text{ mA}$



# TQP369181

## DC-6 GHz Gain Block

### Pin Description



Pin	Symbol	Description
3	RF IN	RF input, matched to 50 ohms. External DC Block is required.
6	RF OUT	RF output / DC supply, matched to 50 ohms. External DC Block, bias choke, and dropping resistor is required.
1, 2, 4, 5	GND	Multiple vias should be employed to minimize inductance and thermal resistance; see page 8 for mounting configuration.

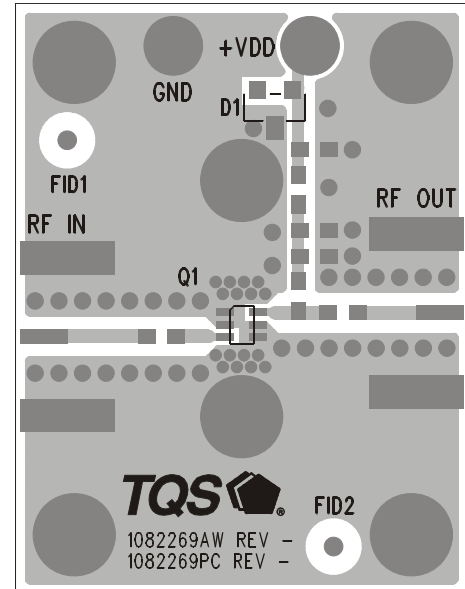
### Applications Information

#### PC Board Layout

Top RF layer is .014" NELCO N4000-13,  $\epsilon_r = 3.7$  typ., 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035"

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to [www.TriQuint.com](http://www.TriQuint.com)



# TQP369181

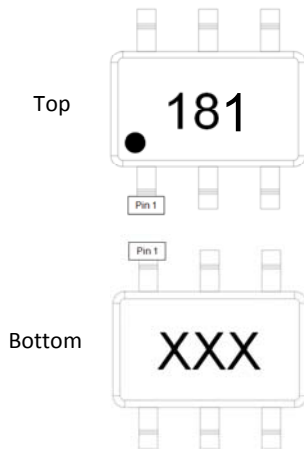
## DC-6 GHz Gain Block



### Mechanical Information

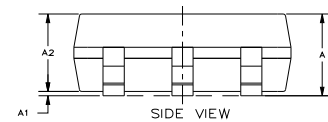
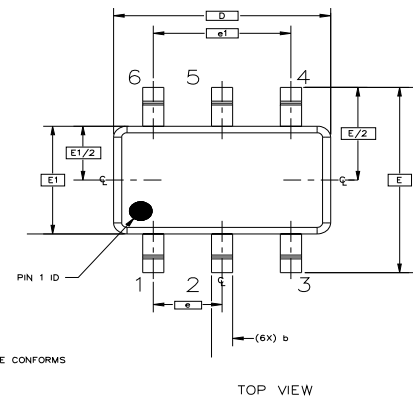
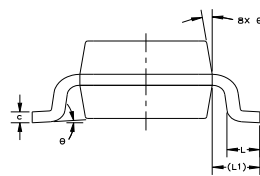
### Package Information and Dimensions

The component is marked on the top surface of the package with a "181" designator and on the bottom surface with an alphanumeric lot code.



SYMBOL	MIN	MAX
A	—	1.10 (.043)
A1	0	.10 (.004)
A2	.70 (.028)	1.00 (.039)
D	2.00 (.079)	BASIC
E	2.10 (.083)	BASIC
E1	1.25 (.039)	BASIC
L	.21 (.008)	.21 (.016)
L1	.42 (.017)	REF
L2	.15 (.006)	BASIC
e	0'.8	8'.8
e1	4'.8	12'.8
b	.15 (.006)	.30 (.012)
c	.06 (.003)	.22 (.009)
e	.65 (.026)	BASIC
e1	1.30 (.051)	BASIC

- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1194. PACKAGE CONFORMS TO JEDEC MO-203, ISSUE B.
  2. DIMENSIONS ARE IN MILLIMETERS (INCHES).



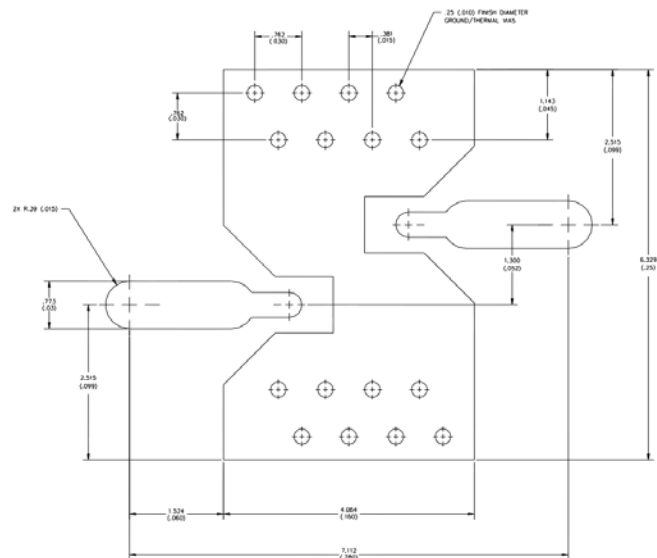
### Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.

### Land Pattern

Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum



## Product Compliance Information

### ESD Information



#### Caution! ESD-Sensitive Device

ESD Rating: Class 1C  
Value: Passes  $\geq 1000$  V to  $< 2000$  V  
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV  
Value: Passes  $\geq 1000$  V  
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

### MSL Rating

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

### Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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