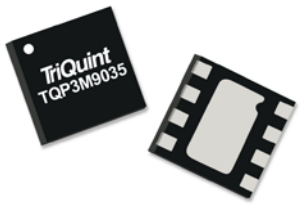
TQP3M9035

High Linearity LNA Gain Block

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

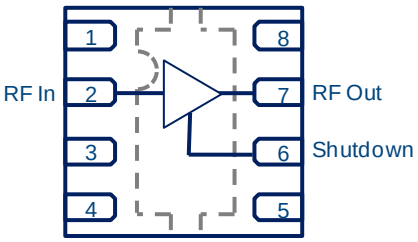


2x2mm 8-lead DFN plastic package

Product Features

- 50-4000 MHz
- 0.66 dB Noise Figure @ 1.9 GHz
- 16.5 dB Gain @ 1.9 GHz
- +37.0 dBm Output IP3
- +22.5 dBm P1dB
- Shut-down capability
- Unconditionally stable
- 50 Ohm Cascadable Gain Block
- +5V Single Supply, 110 mA Current
- 2x2mm 8-lead DFN plastic package

Functional Block Diagram



General Description

The TQP3M9035 is a high linearity low noise gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 16.5 dB gain, +37.0 dBm OIP3, and 0.66 dB Noise Figure. The LNA is also designed to be broadband without the requirement for external matching. The device is housed in a lead-free/green/RoHS-compliant industry-standard 2x2mm package.

The TQP3M9035 has the benefit of having high linearity while also providing very low noise across a broad range of frequencies. This allows the device to be used in both receive and transmit chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The low noise amplifier integrates a shut-down biasing capability to allow for operation for TDD applications.

The TQP3M9035 covers the 0.05 - 4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin #	Symbol
1,3,4,5,8	N/A
2	RF Input
6	SD (Shutdown)
7	RF Output

Ordering Information

Part No.	Description
TQP3M9035	High Linearity LNA Gain Block
TQP3M9035-PCB	0.5-4 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +150 °C
Device Voltage, V_{dd}	+6 V
Max RF Input Power (continuous)	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}		+5	+5.25	V
T_{case}	-40		85	°C
Tj (for>10^6 hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: +25ºC, +5V Vsupply, 50 Ω system.

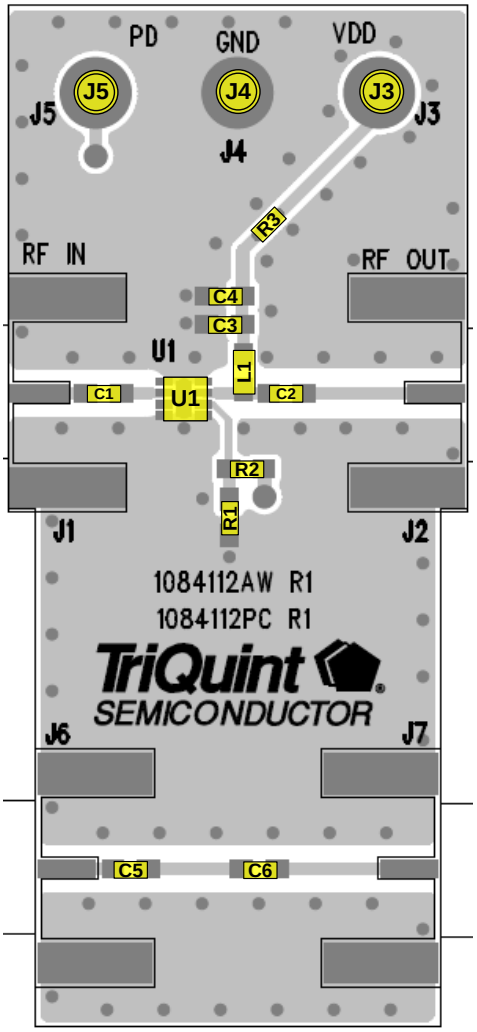
Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		15	16.5	18	dB
Input Return Loss			15		dB
Output Return Loss			10		dB
Output P1dB		+20	+22.5		dBm
Output IP3	See Note 1.	+32.5	+37.0		dBm
Noise Figure			0.66	0.9	dB
V_{dd}			+5		V
Current, I_{dd}	On state		110		mA
	Off state		3.0		mA
Shutdown pin current, I_{sd}	V_{sd} > 3 V		100		µA
Thermal Resistance (jnc to case) θ_{jc}				50	°C/W

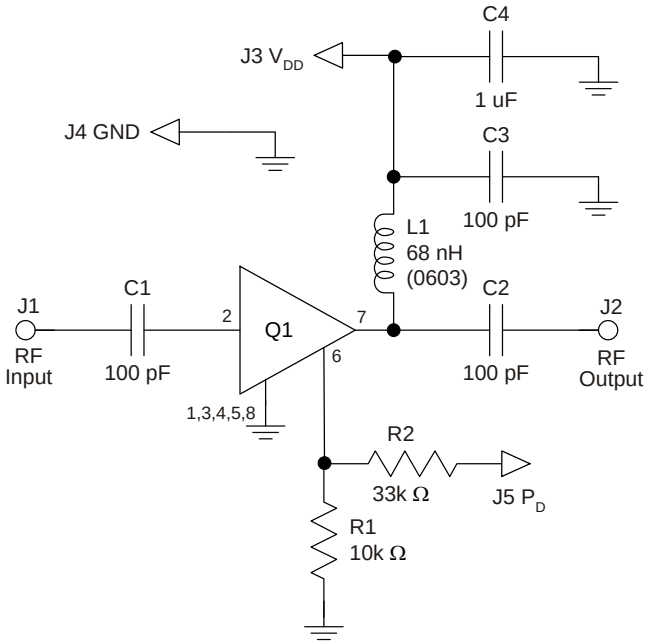
Notes
1. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

Power Shutdown Control

State	Pin 6 Bias Condition
On state	≤ 0.8 V
Power down	≥ 3.0 V

Application Circuit Configuration





Notes:
1. See PC Board Layout, page 5 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. R3 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. All components are of 0402 size unless stated on the schematic.
5. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
6. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
7. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
8. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material

Reference Des.	Value	Description
U1	n/a	TQP3M9035 Amplifier, 2x2 mm Package
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W
L1	68 nH	Inductor, 0603, 5%, Ceramic
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R
C1, C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG
J3, J4, J5	n/a	Solder Turret

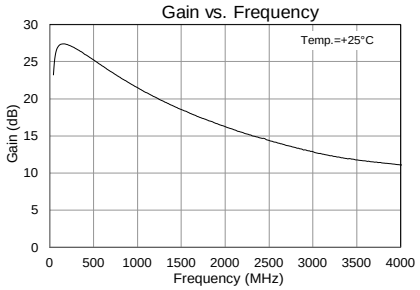
Typical Performance TQP3M9035-PCB

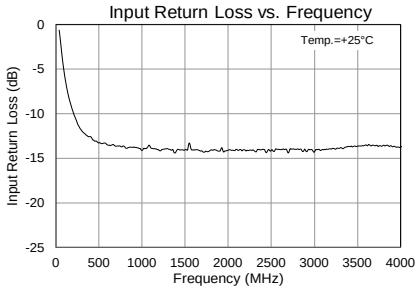
Test conditions unless otherwise noted: +25ºC, +5V, 110 mA, 50 Ω system. The data shown below is measured on TQP3M9035-PCB.

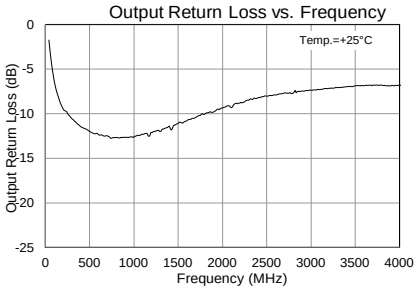
Frequency	MHz	900	1900	2600
Gain	dB	22.0	16.5	14.0
Input Return Loss	dB	14	15	15
Output Return Loss	dB	13	10	8
Output P1dB	dBm	+22.6	+22.5	+22.5
OIP3 [1]	dBm	+37.2	+37.0	+37.3
Noise Figure [2]	dB	0.55	0.66	1.0

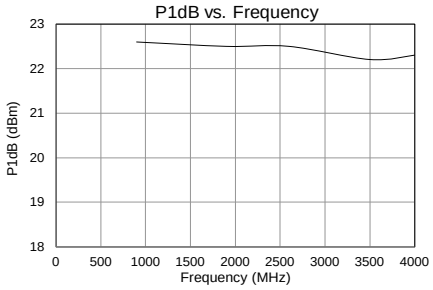
Notes:
1. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is de-embedded to the device leads and removes PCB losses.

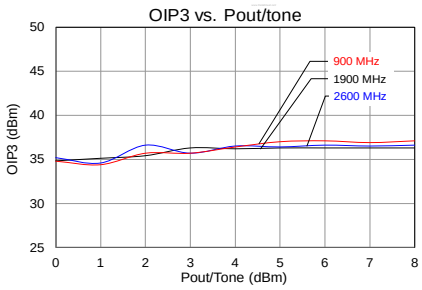
RF Performance Plots

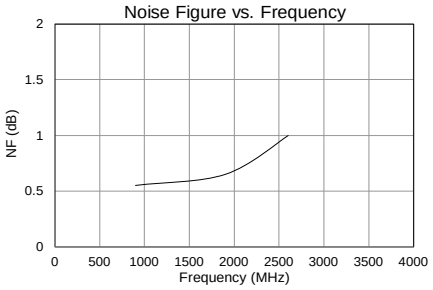


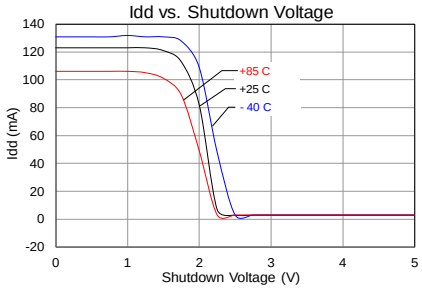




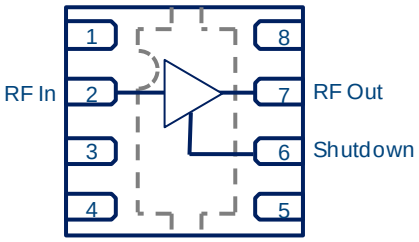








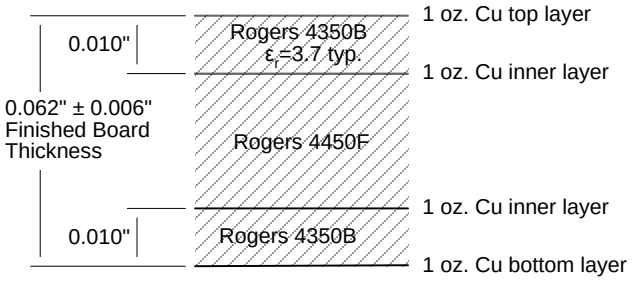
Pin Configuration and Description



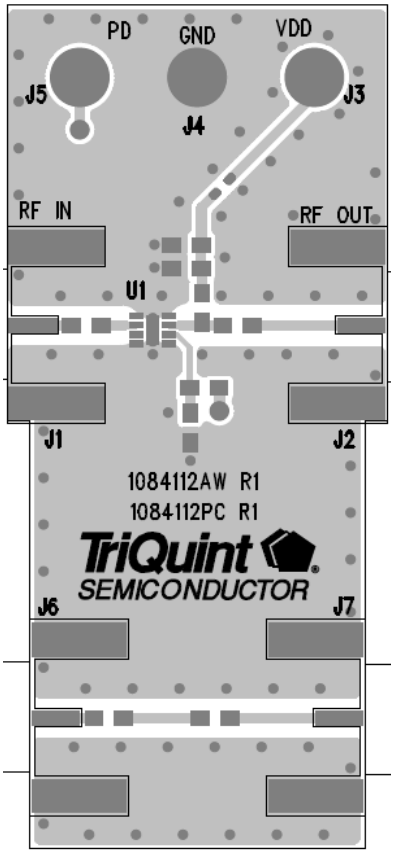
Pin	Symbol	Description
2	RF IN	RF Input, DC Block Required
6	SD	Shut-down pin. A high voltage turns off the device. If the pin is not connected or is less than 1V, then the device will operate under its normal operating condition.
7	RF OUT/BIAS	RF Output, 5V DC Bias
1,3,4,5,8	N/A	Ground or No-connect. No internal connection.

Evaluations Board PCB Specifications

Matirial Stack-Up and Layout



The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

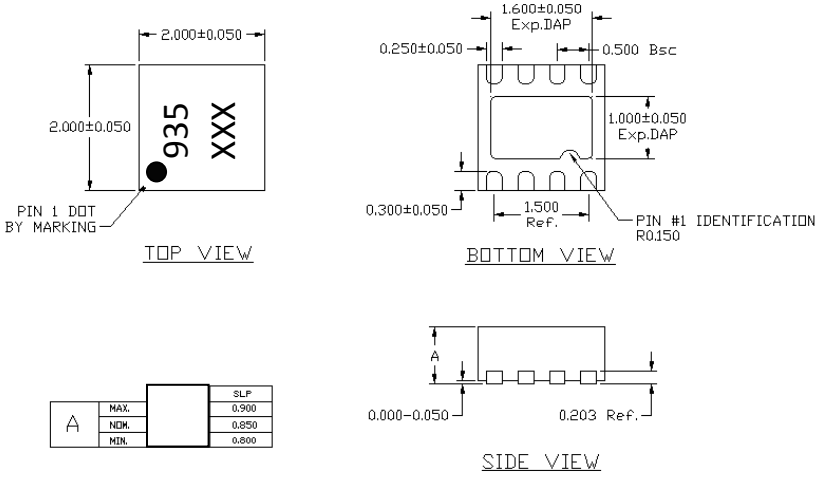


Mechanical Information

Package Information and Dimensions

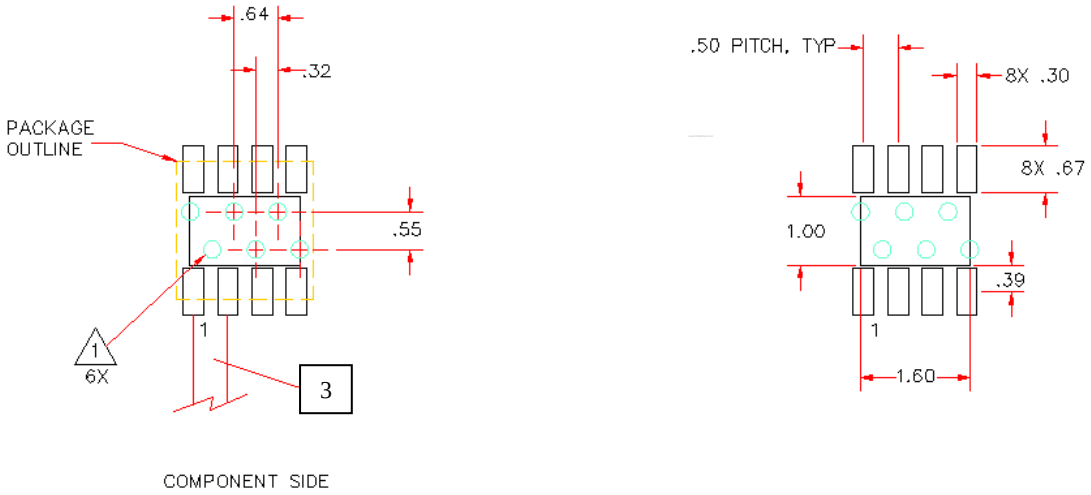
This package is lead-free/RoHS-compliant. The plating material on the backside and leads is annealed matte tin.

The component will be marked with a "935" designator with an alphanumeric lot code on the top surface of package. The "XXX" is an auto generated number.



PCB Mounting Pattern

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 0
Value:	Passes 100V on SD pin (6)
	Passes 250V on RF pins (2, 7)
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes 100V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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