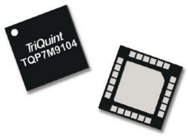
TQP7M9104

2W High Linearity Amplifier

Applications

- Repeaters
- BTS Transceivers
- BTS High Power Amplifiers
- CDMA / WCDMA / LTE
- General Purpose Wireless

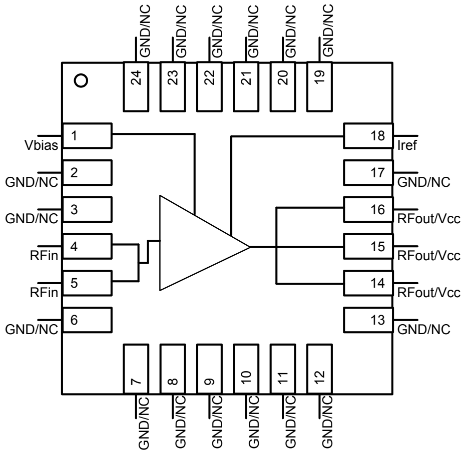


24-pin QFN 4x4mm SMT Package

Product Features

- 700-4000 MHz
- +32.8 dBm P1dB
- +49.5 dBm Output IP3
- 15.8 dB Gain @ 2140 MHz
- +5V Single Supply, 435 mA Collector Current
- Internal RF overdrive protection
- Internal DC overvoltage protection
- Internal Active Bias
- On chip ESD protection
- Shut-down Capability
- Capable of handling 10:1 VSWR @ 5Vcc, 2.14 GHz, 32.8 dBm CW Pout or 23.5 dBm WCDMA Pout

Functional Block Diagram



General Description

The TQP7M9104 is a high linearity driver amplifier in industry standard, RoHS compliant, QFN surface mount package. This InGaP/GaAs HBT delivers high performance across 700-4000 MHz range of frequencies with 15.8 dB Gain, +49.5 dBm OIP3 and +32.5 dBm P1dB at 2.14 GHz while only consuming 435 mA quiescent collector current. All devices are 100% RF and DC tested.

The TQP7M9104 incorporates on-chip features that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system.

The TQP7M9104 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device is an excellent candidate for transceiver line cards and high power amplifiers in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin #	Symbol
1	Vbias
2, 3, 6, 7, 8, 9, 10, 11, 12,13, 17, 19, 20, 21, 22, 23, 24	GND / NC
4, 5	RFin
14, 15, 16	RFout/Vcc
18	Iref

Ordering Information

Part No.	Description
TQP7M9104	2 W High Linearity Amplifier
TQP7M9104-PCB900	TQP7M9104 920-960MHz EVB
TQP7M9104-PCB2140	TQP7M9104 2.11-2.17GHz EVB

Standard T/R size =2500 pieces on a 13” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage, V_{cc}	6.5 V
Maximum Input Power, CW	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}		+5	+5.25	V
T_{case}	-40		+85	°C
Tj (for>10^6 hours MTTF)			160	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

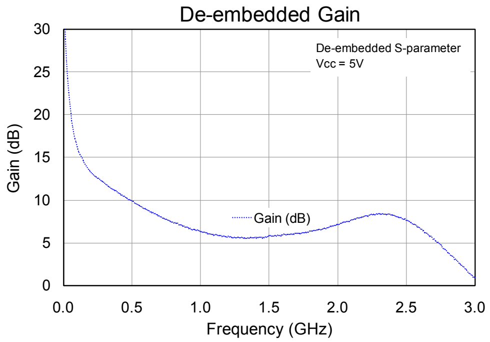
Test Conditions: V_{CC} = +5V, I_{CQ} = 435 mA, T = 25°C using a TQP7M9104-PCB2140 application circuit.

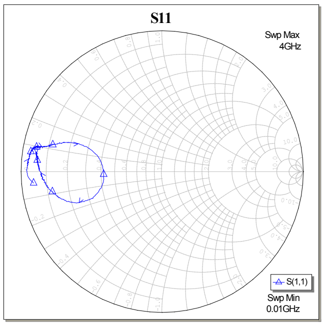
Parameter	Conditions	Min	Typical	Max	Units
Operational Bandwidth		700		4000	MHz
Test Frequency			2140		MHz
Power Gain		14.3	15.8	17.3	dB
Input Return Loss			12		dB
Output Return Loss			9.5		dB
Output IP3 (+17 dBm/tone, Δf = 1 MHz)	See Note 1.	+45.5	+49.5		dBm
WCDMA Channel Power (at -50 dBc ACLR)	See Note 2.		23.8		dBm
Output P1dB		+32	+32.8		dBm
Noise Figure			4.4		dB
Quiescent Collector Current, Icq		355	435	490	mA
Vcc			+5		V
Iref			19		mA
Thermal Resistance (jnc to case) θ_{jc}			15.7		°C/W

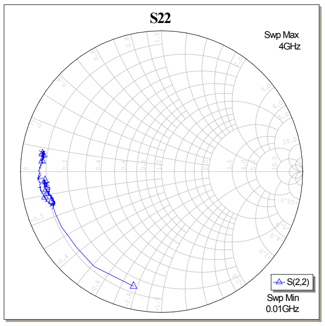
Notes:

1. OIP3 is measured with 1 MHz tone spacing.
2. Using W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 9.7 dB @ 0.01% Probability, 3.84 MHz BW

Device Characterization Data







S-Parameter Data

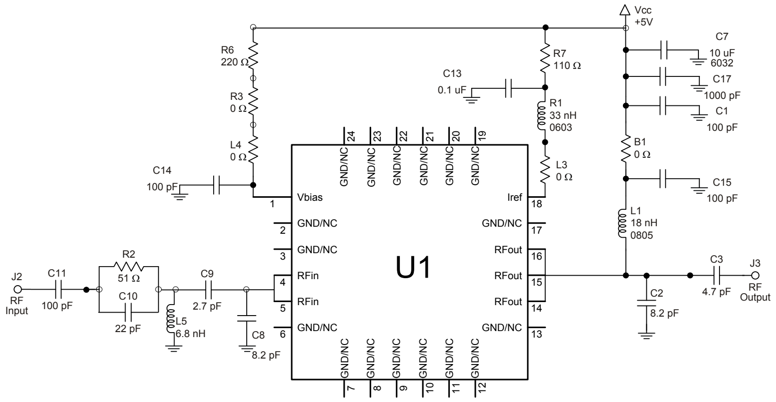
V_{dd} = +5 V, I_{cq} = 435 mA, Iref = 19mA, T = +25°C, unmatched 50 ohm system, calibrated to device leads

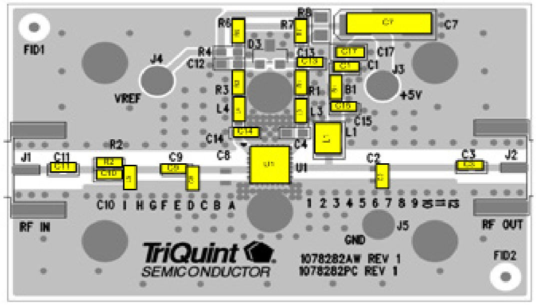
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.4553	-179.26	20.126	118.98	-43.273	4.1446	-1.8524	-155.37
100	-0.4348	178.69	15.971	124.23	-42.615	-1.4433	-1.8878	-166.21
200	-0.4583	176.36	13.24	126.46	-40.235	2.3772	-1.859	-172.01
400	-0.5124	173.38	10.778	118.38	-40.956	0.7196	-1.5792	-174.84
600	-0.5796	171.48	8.9263	108.51	-41.682	10.901	-1.6005	-175.51
800	-0.6594	170.04	7.3201	100.05	-42.533	-8.3414	-1.6164	-174.73
1000	-0.7617	169.21	6.2878	93.94	-42.841	6.4435	-1.531	-173.74
1200	-0.8777	168.95	5.7693	89.116	-40.461	3.1558	-1.6296	-171.43
1400	-1.1121	168.56	5.5556	83.209	-39.435	-0.2787	-1.7656	-170.12
1600	-1.4274	167.84	6.0222	74.67	-41.097	-1.3568	-1.8812	-167.74
1800	-1.9525	165.88	6.3509	63.971	-37.935	-22.971	-1.951	-165.22
2000	-3.0149	163.02	7.1412	51.862	-36.666	-37.917	-1.9853	-163.19
2200	-5.3234	162.27	8.1891	30.583	-35.423	-57.21	-1.7616	-163.18
2400	-7.8162	-179.65	8.2216	2.8455	-35.631	-78.615	-1.5099	-167.05
2600	-5.6951	-159.12	6.6099	-26.943	-35.017	-113.27	-1.2811	-172.58
2800	-3.2673	-161.75	3.8288	-51.412	-37.551	-151.24	-1.2268	-179.96
3000	-2.1416	-169.16	0.9043	-67.725	-39.417	-168.38	-1.4503	175.32

Reference Design 869-894 MHz

Typical Performance at 25 °C

Frequency (MHz)	Units	869	880	894
Gain	dB	20.8	20.8	20.8
Input Return Loss	dB	-13.3	-13	-11.5
Output Return Loss	dB	-7.7	-8.6	-9.8
Output P1dB	dBm	+34.3	+34.1	+33.8
Output IP3 (+23 dBm/tone, Δf = 1 MHz)	dBm	+44.9	+44.9	+44.7
WCDMA Channel Power (at -50 dBc ACLR)	dB	22	22.5	23
Supply Voltage, Vcc	V	+5		
Quiescent Current, Icq	mA	435		
Reference Current, Iref	mA	19		

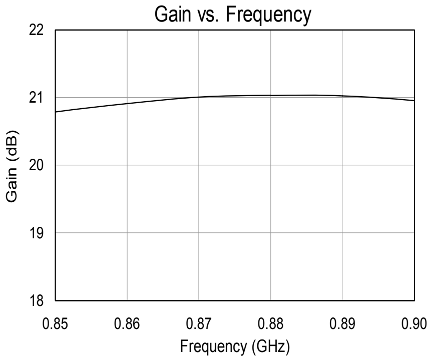


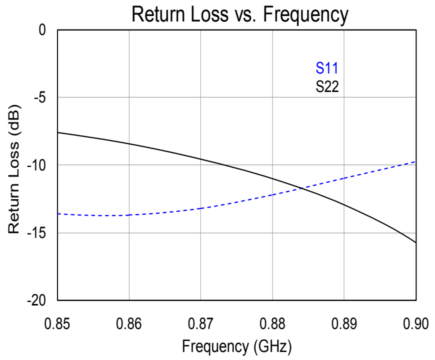


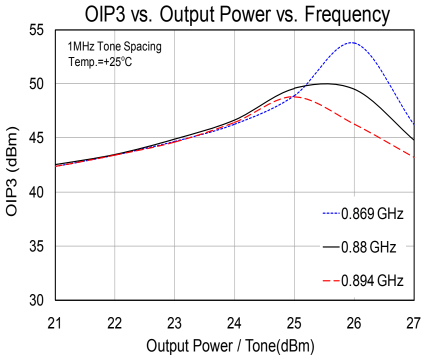
Notes:

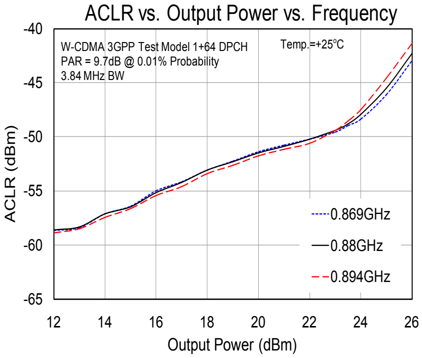
1. Components shown on the silkscreen but not on the schematic are not used.
2. 0 Ω resistor may be replaced with copper trace in the target application layout.
3. Iref can be used as device power down current by placing R7 at location R8.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. R1 is critical for device linearity performance.
7. Critical component placement locations:
   Distance between center of C8 and TQP7M9104 (U1) device package is 243 mil.
   Distance between center of L5 and TQP7M9104 (U1) device package is 452 mil.
   Distance between center of C2 and TQP7M9104 (U1) device package is 355 mil.
   Distance between center of C9 and TQP7M9104 (U1) device package is 275 mil.

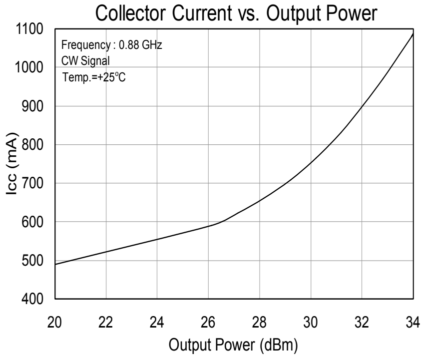
RF Performance Plots 869-894 MHz



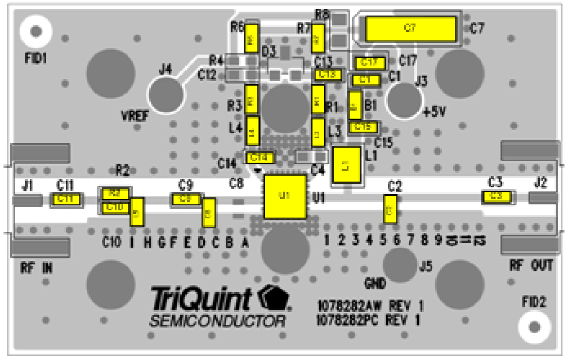


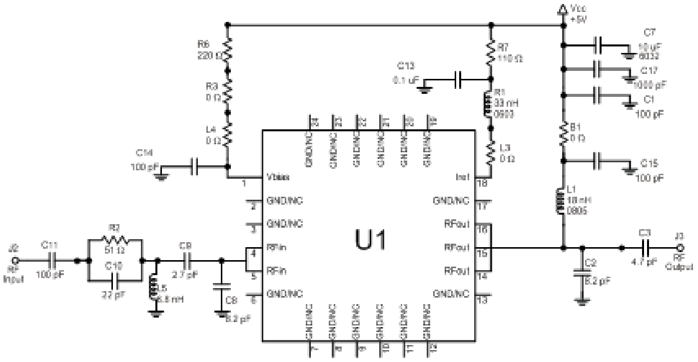






Application Circuit 920-960 MHz (TQP7M9104-PCB900)





Notes:

1. See PC Board Layout under Application Information section for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistor may be replaced with copper trace in the target application layout.
4. Iref can be used as device power down current by placing R7 at location R8.
5. The recommended component values are dependent upon the frequency of operation.
6. All components are of 0603 size unless stated on the schematic.
7. R1 is critical for device linearity performance.
8. Critical component placement locations:
   Distance between center of C8 and TQP7M9104 (U1) device package is 190 mil.
   Distance between center of L5 and TQP7M9104 (U1) device package is 452 mil.
   Distance between center of C2 and TQP7M9104 (U1) device package is 305 mil.
   Distance between center of C9 and TQP7M9104 (U1) device package is 275 mil.

Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
U1	n/a	2W High Linearity Amplifier	TriQuint	TQP7M9104
n/a	n/a	Printed Circuit Board	TriQuint	1078282
C9	2.7 pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J2R7ABSTR
B1, L3, L4, R3	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L5	6.8 nH	Inductor, 0603, 5%	Toko	LL1608-FSL6N8
C3	4.7 pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J4R7ABSTR
C2, C8	8.2 pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J8R2ABSTR
C10	22 pF	Capacitor, Chip, 0603, 5%, 50 V, NPO/COG	various	
C1, C14, C15, C11	100 pF	Capacitor, Chip, 0603, 5%, 50V, NPO/COG	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C17	1000 pF	Capacitor, Chip, 0603, 10%, 50V, NPO/COG	various	
C13	0.1 uF	Capacitor, Chip, 0603, 50V, X5R, 10%	various	
C7	10 uF	Capacitor , Tantalum, 6032, 35V, 10%	various	
R2	51 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R6	220 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R7	110 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R1	33 nH	Inductor, 0603, 5%	Toko	LL1608-FSL33N
R8, R4, C12, C4,D3	n/a	Do Not Place		

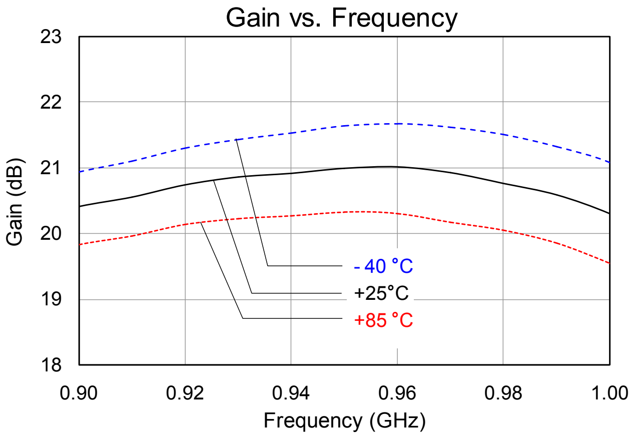
Typical Performance 920-960 MHz

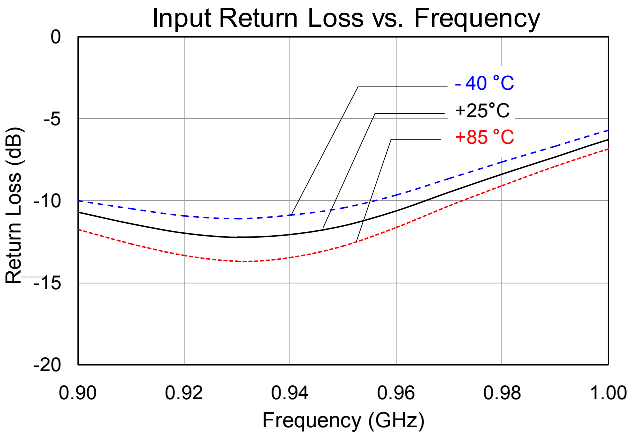
Frequency	**MHz**	**920**	**940**	**960**
Gain	dB	20.8	21	21
Input Return Loss	dB	-13	-12	-11
Output Return Loss	dB	-9	-11.8	-15
Output P1dB	dBm	+33.9	+33.8	+33.4
Output IP3 (+23 dBm/tone, Δf = 1 MHz)	dBm	+45	+45	+45
WCDMA Channel power (at -50 dBc ACLR) [1]	dBm	+24	+23.5	+23
Supply Voltage, Vcc	V	+5		
Quiescent Collector Current, Icq	mA	435		
Reference Current , Iref	mA	19		

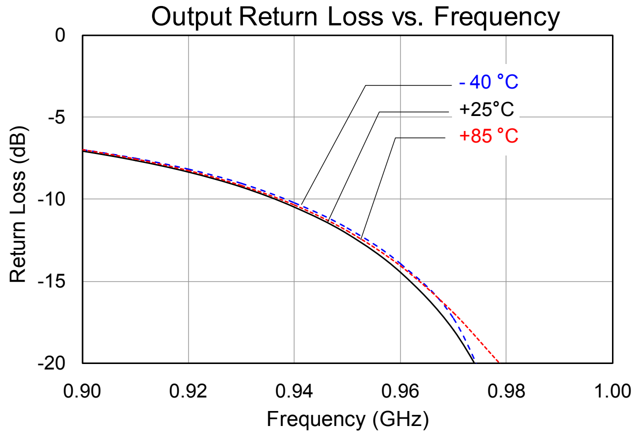
Notes:

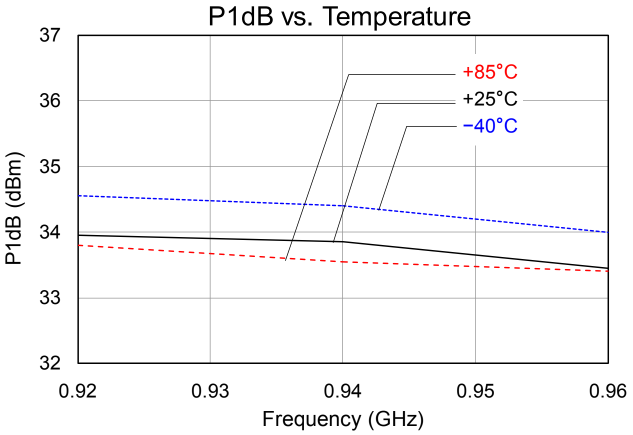
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 9.7 dB at 0.01% Prob.

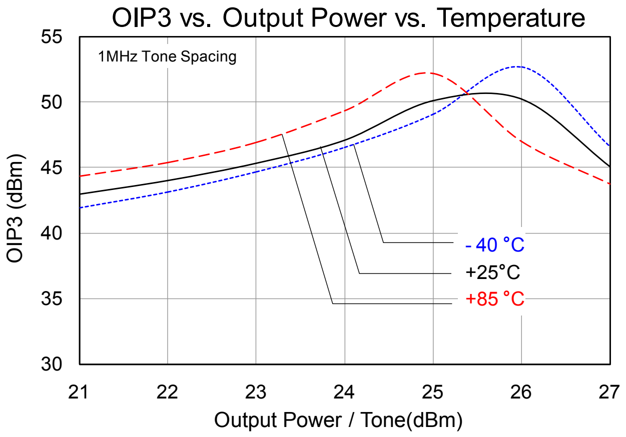
RF Performance Plots 920-960 MHz

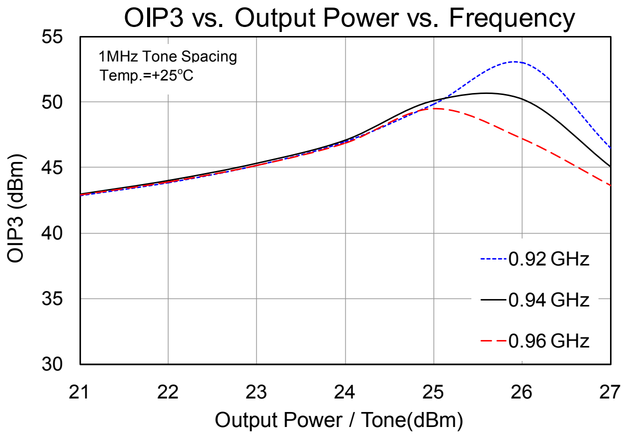


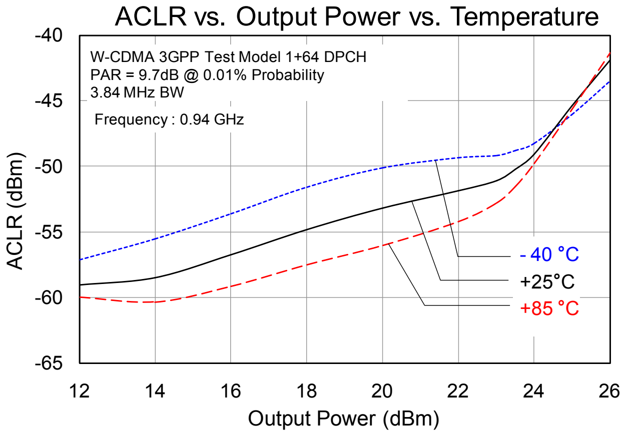


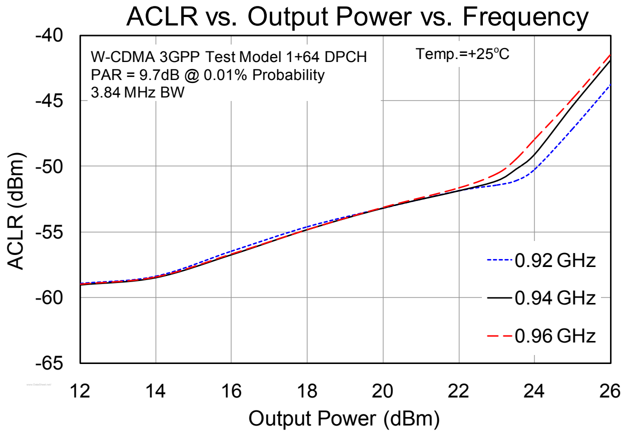


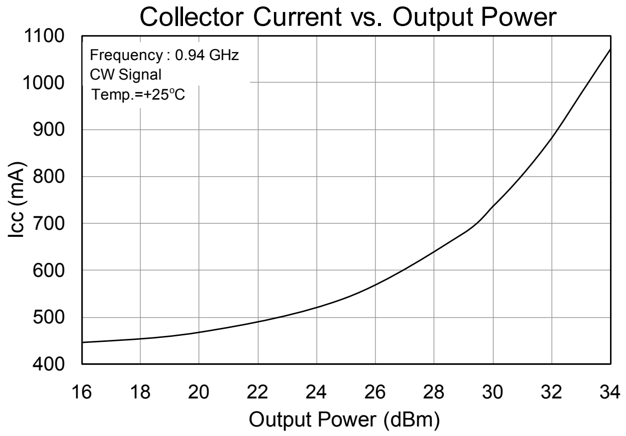



OIP3 vs. Output Power vs. Temperature

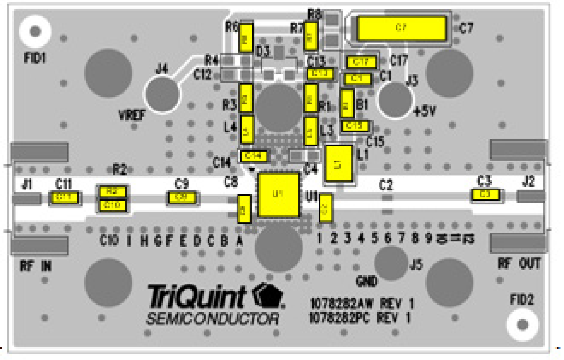

OIP3 vs. Output Power vs. Frequency

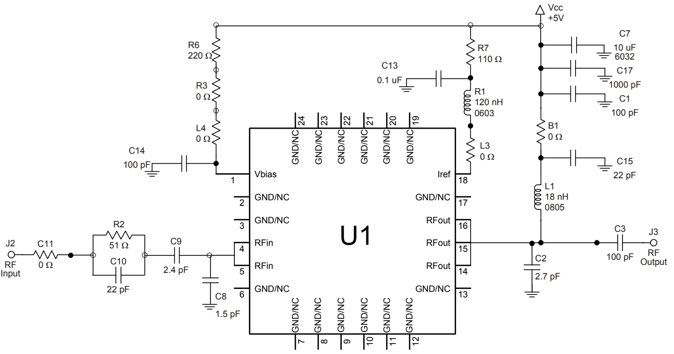

ACLR vs. Output Power vs. Temperature


ACLR vs. Output Power vs. Frequency


Collector Current vs. Output Power

Application Circuit 2110-2170 MHz (TQP7M9104-PCB2140)





Notes:

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   - Distance between center of C2 and TQP7M9104 (U1) device package is113 mil.
   - Distance between center of C9 and TQP7M9104 (U1) device package is 275 mil.

Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
U1	n/a	2W High Linearity Amplifier	TriQuint	TQP7M9104
n/a	n/a	Printed Circuit Board	TriQuint	1078282
C8	1.5 pF	Capacitor, Chip, 0603, ±0.05pF, 50V, Accu-P	AVX	06035J1R5ABSTR
C9	2.4 pF	Capacitor, Chip, 0603, ±0.05pF, 50V, Accu-P	AVX	06035J2R4ABSTR
C2	2.7 pF	Capacitor, Chip, 0603, ±0.05pF, 50V, Accu-P	AVX	06035J2R7ABSTR
B1, L3, L4, R3, C11	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
C10, C15	22 pF	Capacitor, Chip, 0603, 5%, 50V, NPO/COG	various	
C1, C14, C3	100 pF	Capacitor, Chip, 0603, 5%, 50V, NPO/COG	various	
L1	18 nH	Inductor, 1008, 5%, Ceramic	Coilcraft	1008HQ-18NXJL
C17	1000 pF	Capacitor, Chip, 0603, 10%, 50V, NPO/COG	various	
C13	0.1 uF	Capacitor, Chip, 0603, 10%, 50V, X5R	various	
C7	10 uF	Capacitor , Tantalum, 6032, 20 %, 50V	various	
R2	51 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R6	220 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R7	110 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R1	120 nH	Inductor, 0603, 5%	Toko	LL1608-FSR12J
R8, R4, C12, C4, D3	n/a	Do Not Place		

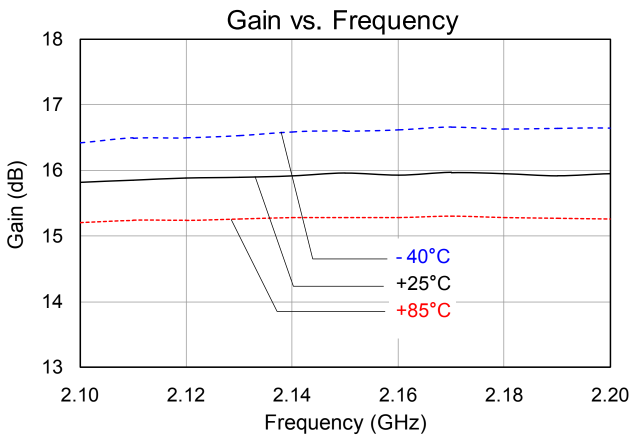
Frequency	MHz	2110	2140	2170

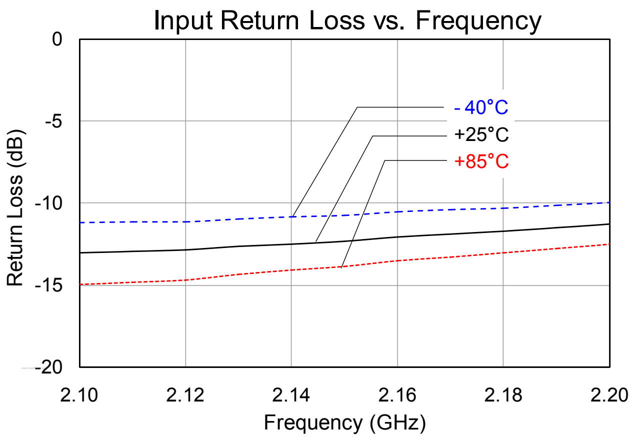
Gain	dB	15.8	15.8	15.8
Input Return Loss	dB	-12.4	-12.0	-11.8
Output Return Loss	dB	-8.7	-9.5	-10.5
Output P1dB	dBm	+32.9	+32.8	+32.8
Output IP3 (+17 dBm/tone, Δf = 1 MHz)	dBm	+49	+49.5	+50
WCDMA Channel power (at -50 dBc ACLR) [1]	dBm	+23.5	+23.8	+24.0
Noise Figure	dB	4.4	4.4	4.6
Supply Voltage, Vcc	V	+5		
Quiescent Collector Current, Icq	mA	435		
Reference Current , Iref	mA	19		

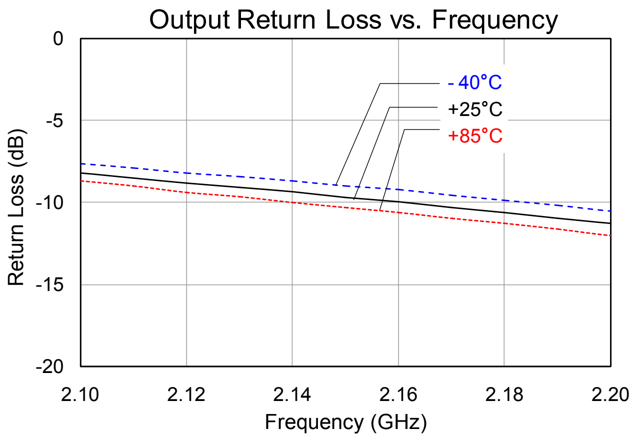
Notes:

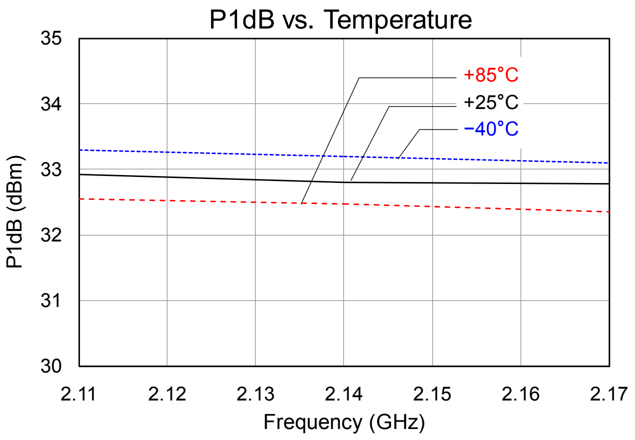
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 9.7 dB at 0.01% Prob.

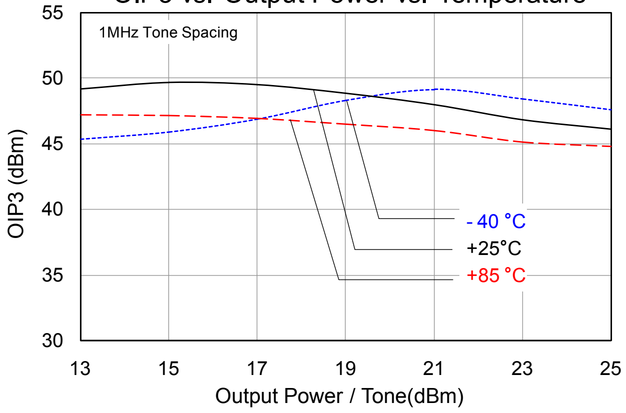
RF Performance Plots 2110-2170 MHz

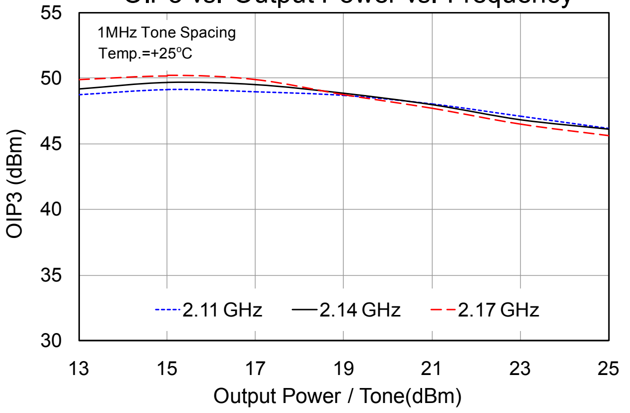

Gain vs. Frequency

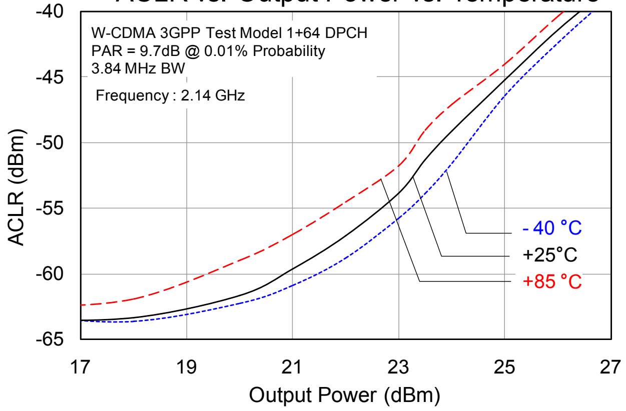

Input Return Loss vs. Frequency

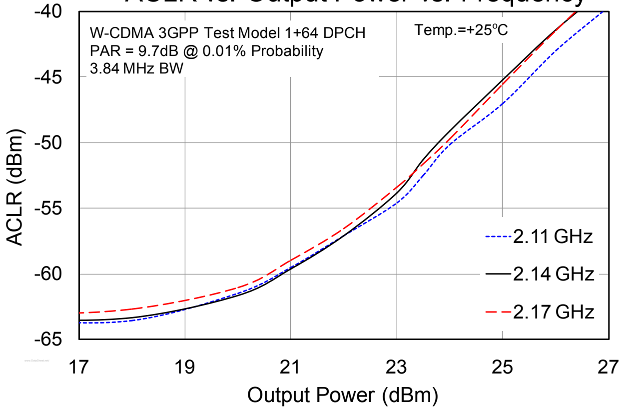

Output Return Loss vs. Frequency

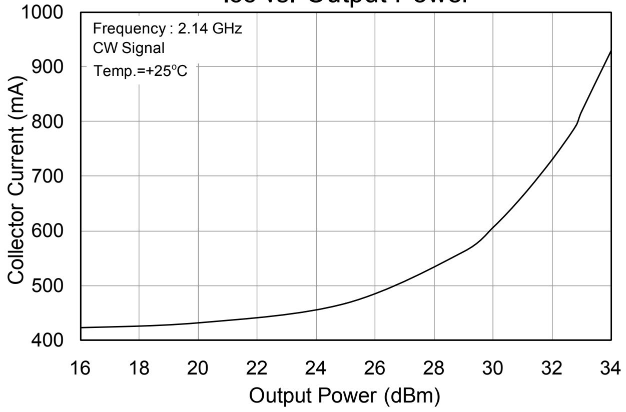

P1dB vs. Temperature

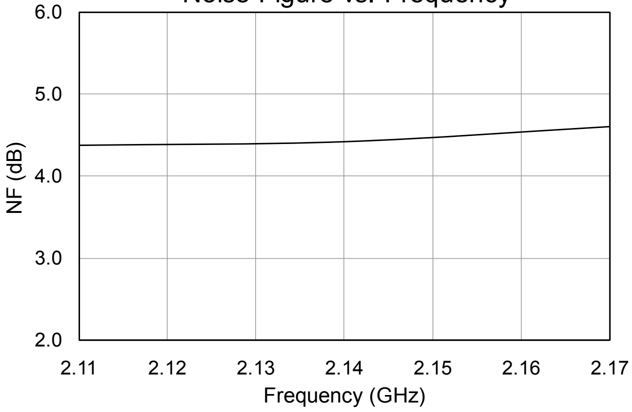

OIP3 vs. Output Power vs. Temperature


OIP3 vs. Output Power vs. Frequency

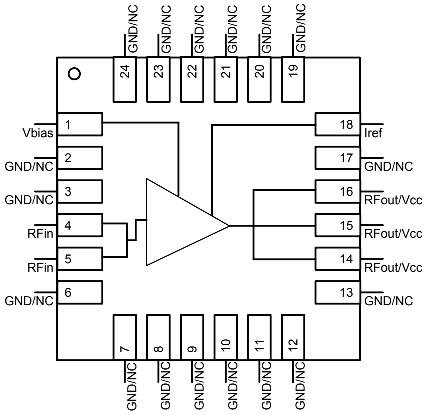

ACLR vs. Output Power vs. Temperature


ACLR vs. Output Power vs. Frequency


Icc vs. Output Power


Noise Figure vs. Frequency

Pin Configuration and Description



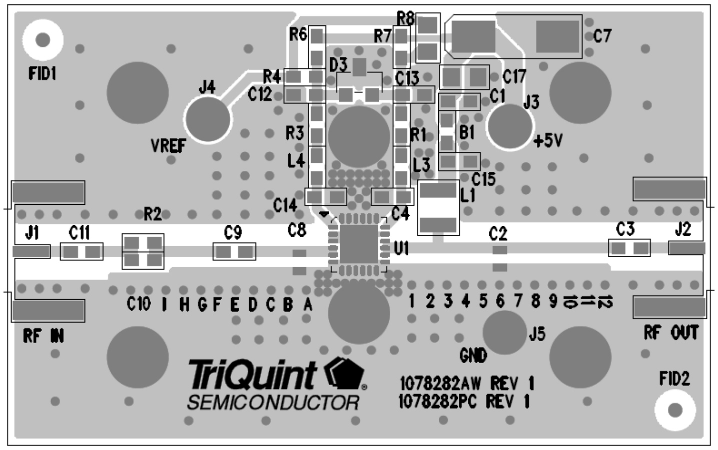
Pin	Symbol	Description
1	Vbias	Voltage supply for active bias for the amp. Connect to same supply voltage as Vcc.
2, 3, 6,7, 8, 9, 10, 11, 12, 13,17, 19, 20, 21, 22, 23, 24	GND/NC	No internal connection. This pin can be grounded or N/C on PCB. Land pads should be provided for PCB mounting integrity.
4, 5	RFin	RF Input. DC voltage present, blocking capacitor required. Requires external match for optimal performance.
14, 15, 16	RFout / Vcc	RF Output. DC Voltage present, blocking cap required. Requires external match for optimal performance.
18	Iref	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current. Also, can be used as on/off control.
Backside paddle	RF/DC GND	Multiple Vias should be employed to minimize inductance and thermal resistance. Use recommended via pattern shown under mounting configuration and ensure good solder attach for optimum thermal and electrical performance

Applications Information

PC Board Layout

PCB Material (stackup):

1 oz. Cu top layer
0.014 inch Nelco N4000-13, ε_r=3.7
1 oz. Cu middle layer 1
Core Nelco N4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006
50 ohm line dimensions: width = .028”



The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

Mechanical Information

Package Information and Dimensions

This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

The component will be laser marked with "7M9104" product label with an alphanumeric lot code on the top surface of the package.

NOTES:

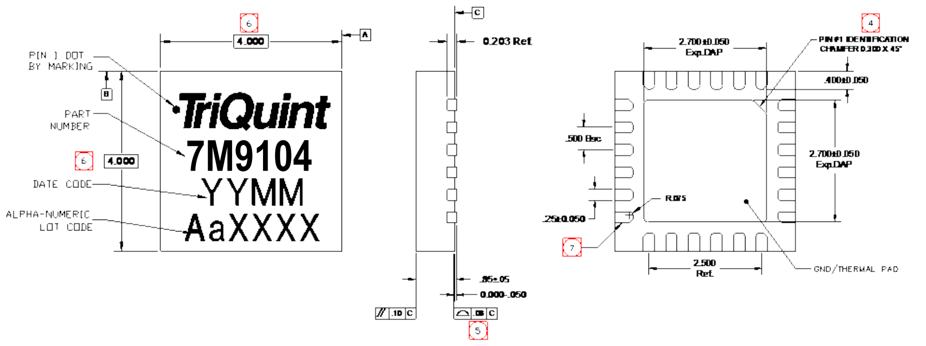
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VGGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4 THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.

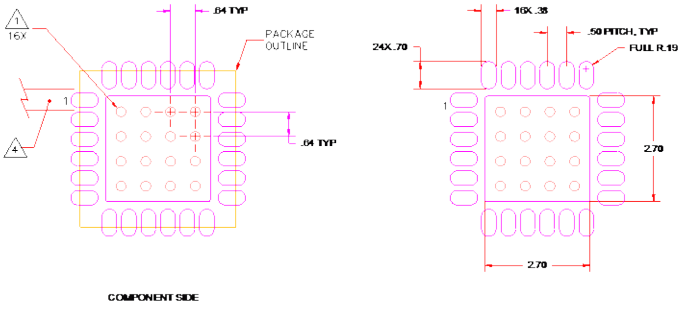
5 COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS

6 PACKAGE BODY LENGTH/WIDTH DOES NOT INCLUDE PLASTIC FLASH PROTRUSION ACROSS MOLD PARTING LINE.

7 DEVIATION FROM JEDEC STANDARD MO-229, ISSUE C, 12 LEAD COUNT NOT



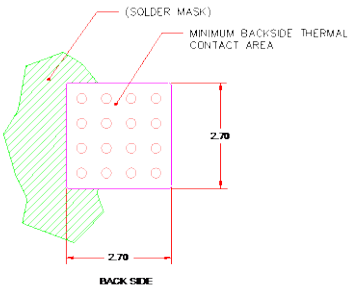
Mounting Configuration



All dimensions are in millimeters (inches). Angles are in degrees.

Notes:

1. Ground vias are critical for the proper RF performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.



NOTES:

1 GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL. PLATED THRU DIAMETER OF .25mm (.010").

2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.

3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL

4 RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.

5. USE 1 OZ. COPPER MINIMUM.

6. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: ≥ 1000 V and < 2000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: ≥ 1000 V min
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

The plating material on the pins is annealed matte tin over copper.
Compatible with both lead-free (maximum 260 °C reflow temperature) and tin/lead (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

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