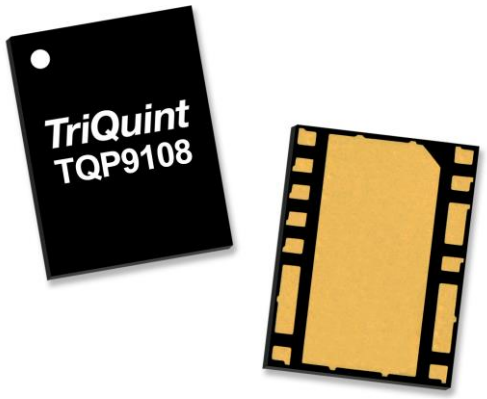
TQP9108

1.7-2.17 MHz 2-stage Power Amplifier

Applications

- Wireless Infrastructure
- Repeaters, Boosters, DAS
- High Power Amplifiers
- Small cell BTS

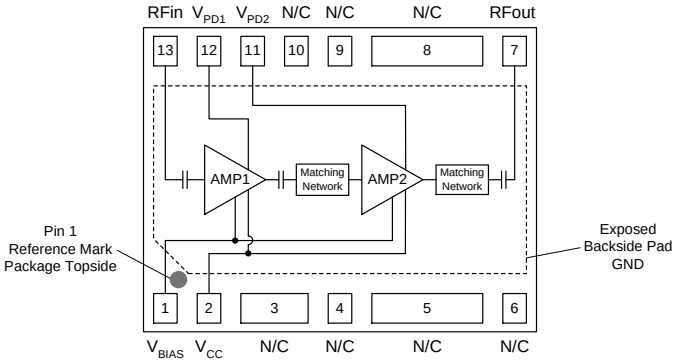


3.5x4.5 mm Leadless SMT Package

Product Features

- 1.71-2.17 GHz Frequency Range
- 30.5 dB gain
- +46 dBm Output IP3 @ 24 dBm/tone
- 39% PAE @ 27 dBm Pout
- Internally Matched
- Integrated interstage matching
- Bias Adjustable
- Low idle current

Functional Block Diagram



Top View

General Description

The TQP9108 is a high-efficiency two-stage power amplifier in a low-cost surface-mount package. The amplifier is able to achieve 39% power added efficiency at 27 dBm output power while operating with a low 65 mA idle current. The amplifier is designed to ensure that all odd-order IMD products are below -17 dBm at all output power levels below 24 dBm/tone.

The TQP9108 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9108 is available in a lead-free/RoHS-compliant 13-pin 3.5x4.5mm surface mount package package and is pin-compatible to the lower frequency band version in the family with the TQP9107 (699-960 MHz).

Pin Configuration

Pin No.	Label
1	V_{BIAS}
2	V_{CC}
3, 4, 5, 6, 8, 9, 10	GND or N/C
7	RFout
11, 12	V_{PD}
13	RF in
Backside Pad	GND

Ordering Information

Part No.	Description
TQP9108	1.71–2.17 GHz Power Amplifier
TQP9108-PCB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
Supply Voltage (V_{CC})	+6 V
RF Input Power, CW, 50 Ω, T=25 °C	+12 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC}, V_{BIAS}		+4.3	+5	V
V_{PD1}, V_{PD2}		+4.0	+5	V
T_{CASE}	−40		105	°C
Tj for >10^6 hours MTTF			+190	°C

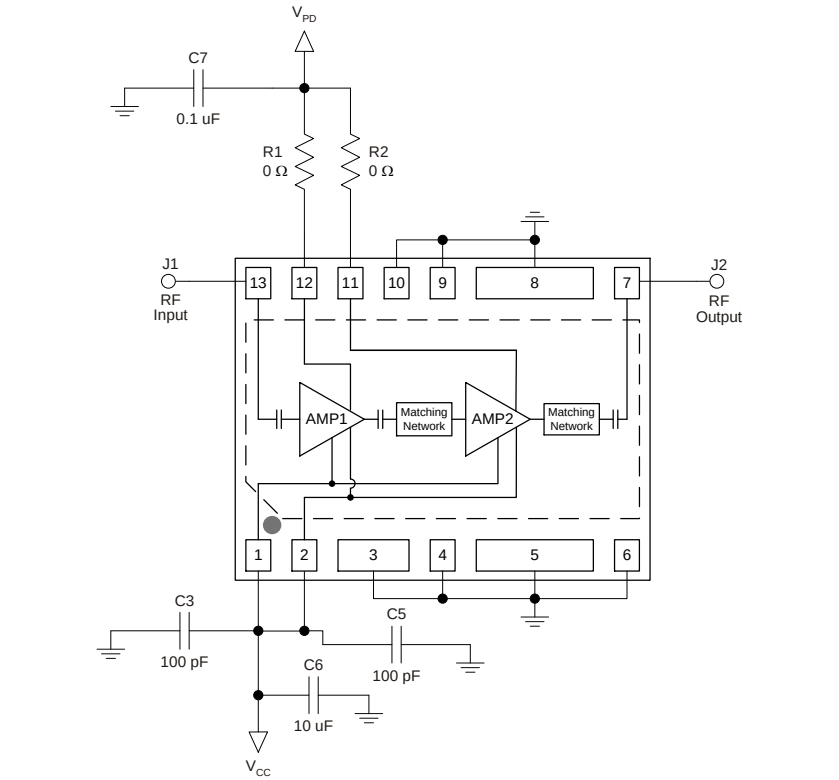
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

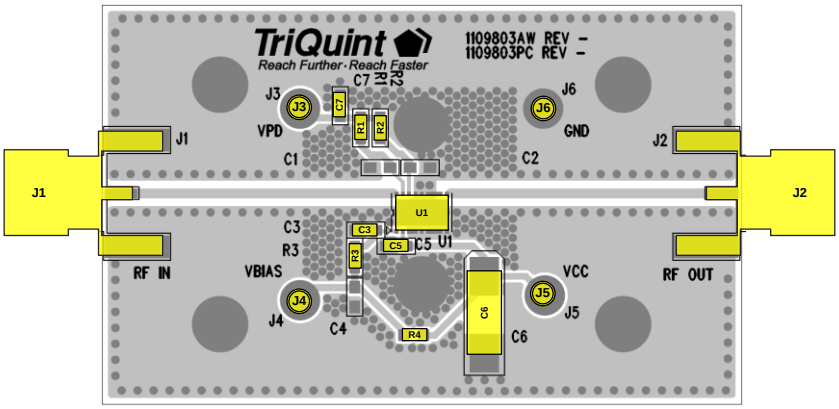
Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = V_{BIAS} = +4.3 V, V_{PD1} = V_{PD2} =+4.0 V, Temp = +25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1710		2170	MHz
Test Frequency			1915		MHz
Gain		28.8	30.5		dB
Noise Figure			5		dB
Output P1dB			+31.3		dBm
Output IP3	Pout = +23 dBm / tone, Δf = 600 kHz	+43	+46		dBm
IMD3, IMD5, IMD7	All power levels ≤ 23 dBm / tone			-17	dBm
Current, I_{CC}	Pout = +27 dBm		300		mA
Power Added Efficiency	Pout = +27 dBm		39		%
Idle Current	No RF Input Power		67		mA
VSWR Survivability	Pout = P1dB Signal : CW All Phases	10:1			–
VSWR Survivability	Pout = +28 dBm Signal : 20 MHz LTE 1C, PAR = 9.5 dB All Phases	6:1			–
Thermal Resistance, θ_{jc}	Junction to case		37.5		°C/W

Application Circuit Schematic and Layout





Bill of Material

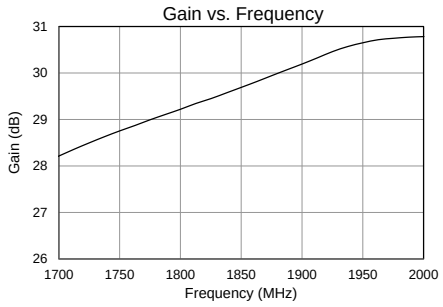
Reference Des.	Value	Description	Manuf.	Part Number
		Nelco FR4, PCB APP BOARD	TriQuint	1109803PC
U1		2-Stage Power Amplifier	TriQuint	TQP9108
C3, C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C6	10 uF	CAP, 6032, 20%, 50V, Tantalum	various	
C7	0.1 uF	CAP, 0603, 50V, X7R, 5%		
R1, R2, R3, R4	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	

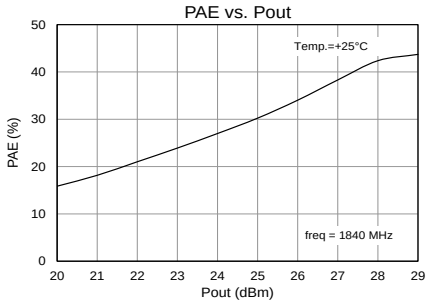
Typical Performance

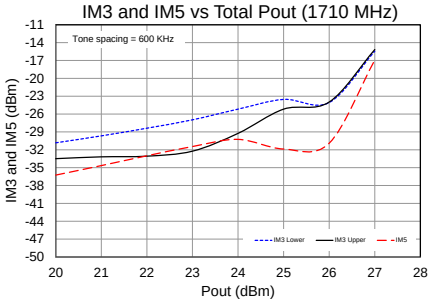
Test Conditions: V_{CC}=+4.3 V, Temp.=+25°C, 50Ω System

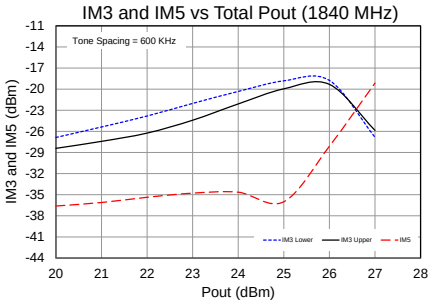
Parameter	Conditions	Typical Value				Units
Frequency		1710	1840	1920	1980	MHz
Gain		28.4	29.6	30.4	30.7	dB
IM3	Pout= +27 dBm, Δf= 600 KHz	-15.5	-26	-29	-17	dBm
IM5	Pout= +27 dBm, Δf= 600 KHz	-17	-19	-18	-15.5	dBm
Quiescent Collector Current, I_{CQ}	V_{PD} = 4V	67				mA

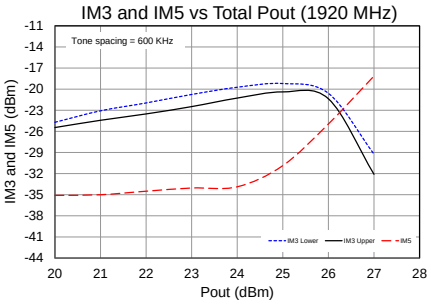
Performance Plots

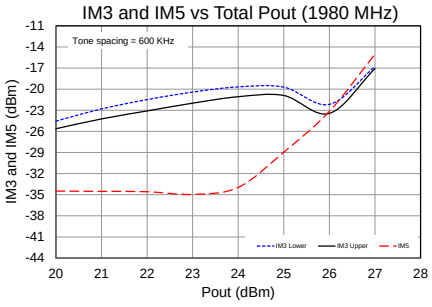


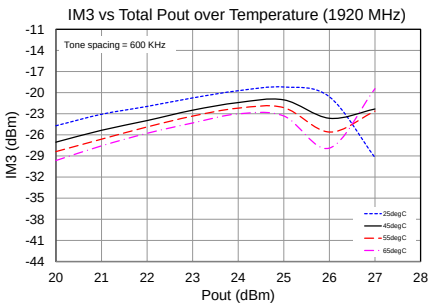


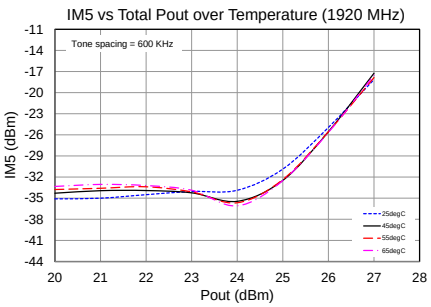


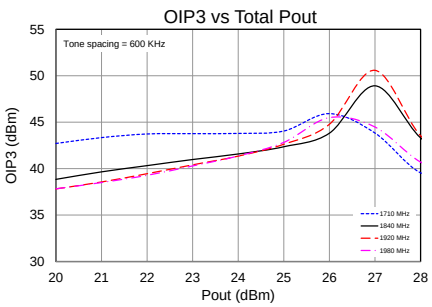










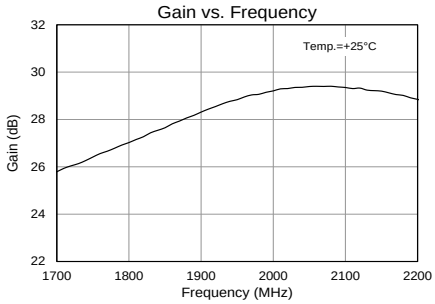


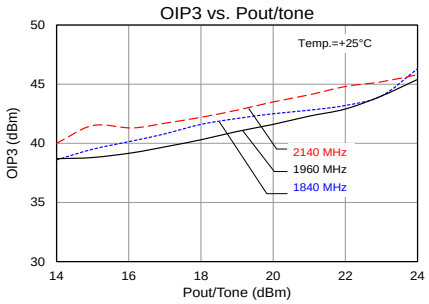
Typical Performance at Vcc = 5V

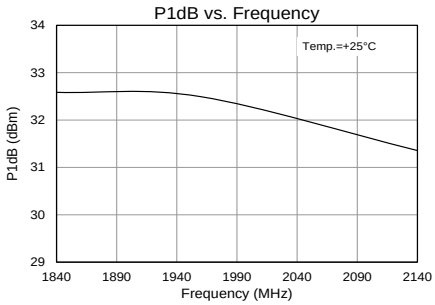
Test Conditions: V_{CC}=+5 V, Vpd=+4.3 V, Temp.=+25°C, 50Ω System

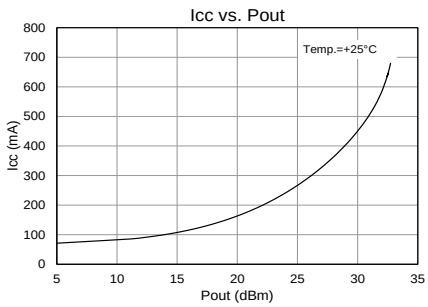
Parameter	Conditions	Typical Value			Units
Frequency		1840	1960	2140	MHz
Gain		28	28.5	29.4	dB
Input Return Loss		-12	-11	-9	dB
Output P1dB		32.3	32.3	32.3	dBm
Output IP3	Pout= +24 dBm/tone, Δf= 1 MHz	46.2	45.4	45.7	dBm
Quiescent Collector Current, I_{CQ}		68			mA

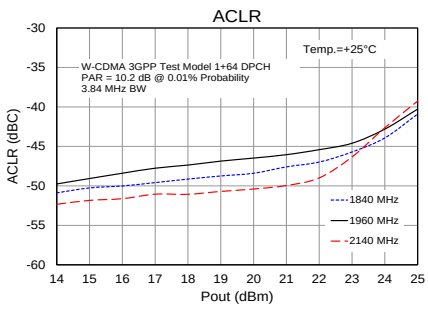
Performance Plots



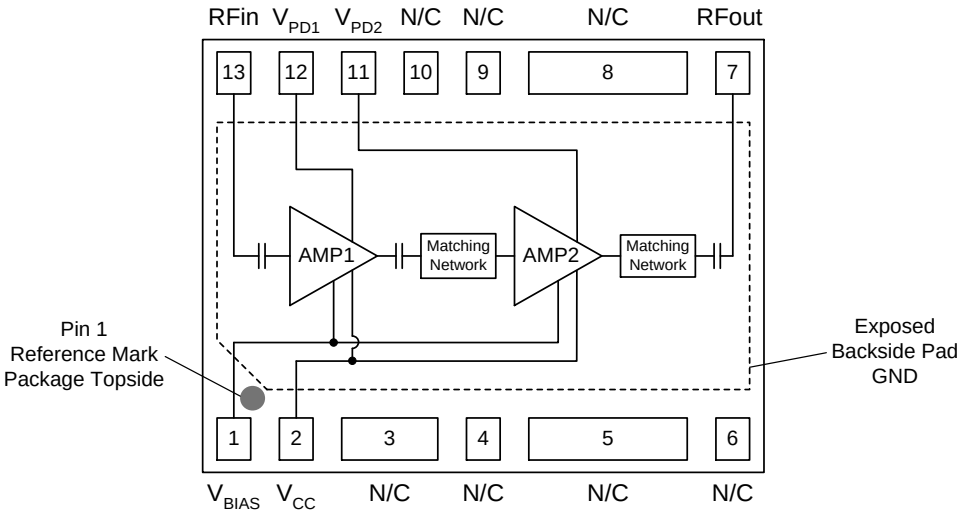








Pin Configuration and Description

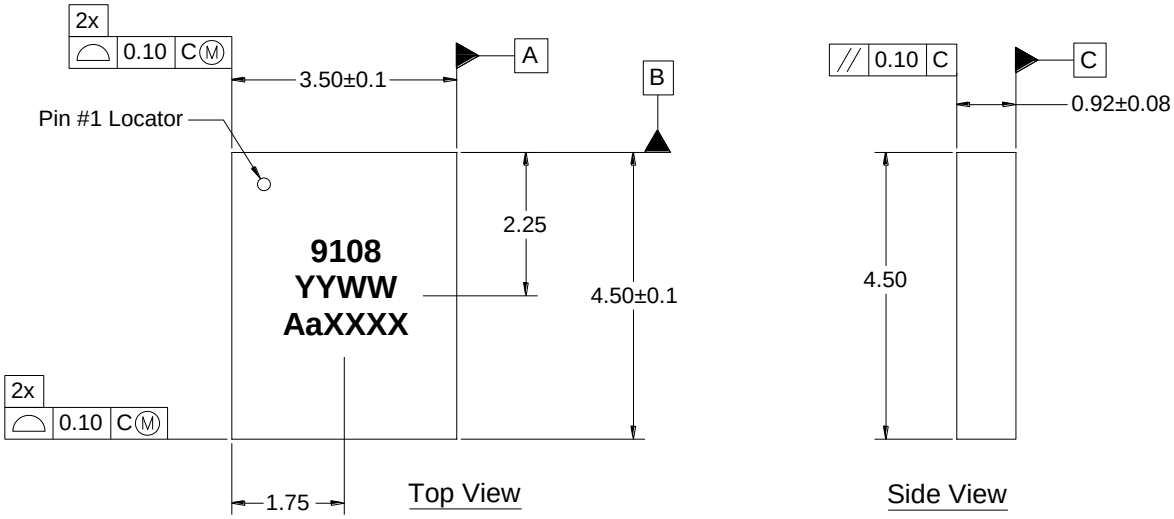


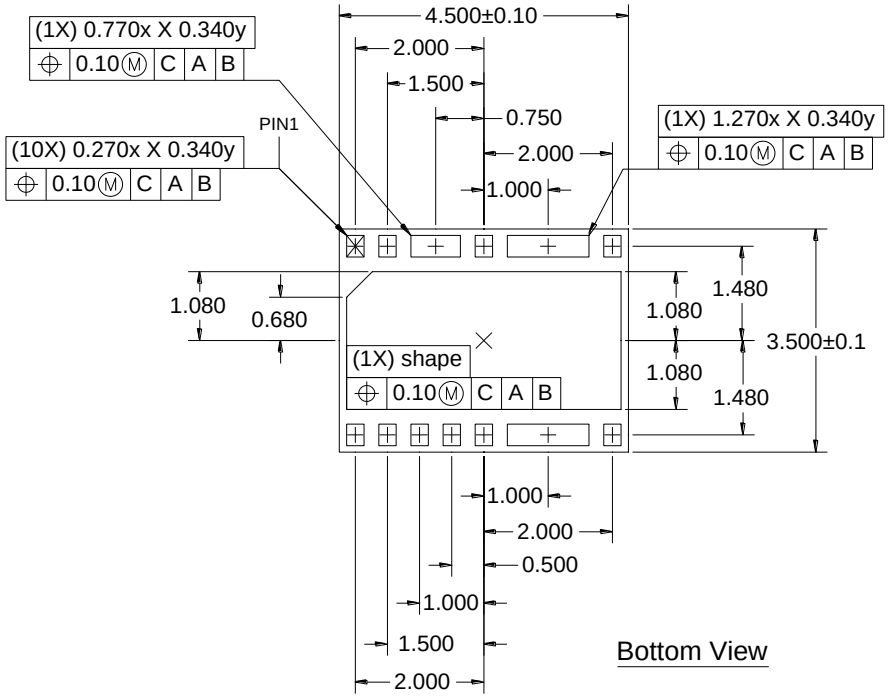
Top View

Pin No.	Label	Description
1	V_{BIAS}	Provides reference voltage for internal active biasing circuit
2	V_{CC}	DC voltage supply connection
3, 4, 5, 6, 8, 9, 10	N/C	No internal connection. Provide grounded land pads for PCB mounting integrity.
7	RF out	RF output pin. The DC is internally blocked at this pin.
11	V_{PD1}	Power down for Amp 1. This voltage adjusts for the current draw in Amp 1.
12	V_{PD2}	Power down for Amp 2. This voltage adjusts for the current draw in Amp 2.
13	RF in	RF input pin. The DC is internally blocked at this pin.
Backside Pad	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

Marking: Part number – 9108
Date - YYWW
Lot code – AaXXXX

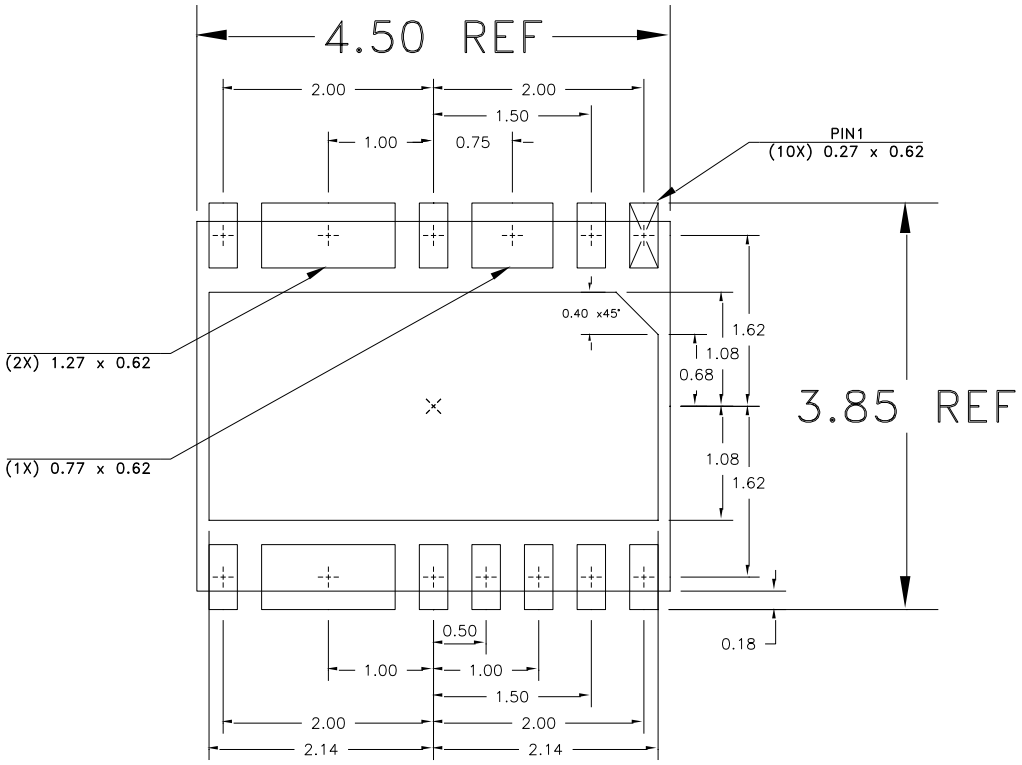




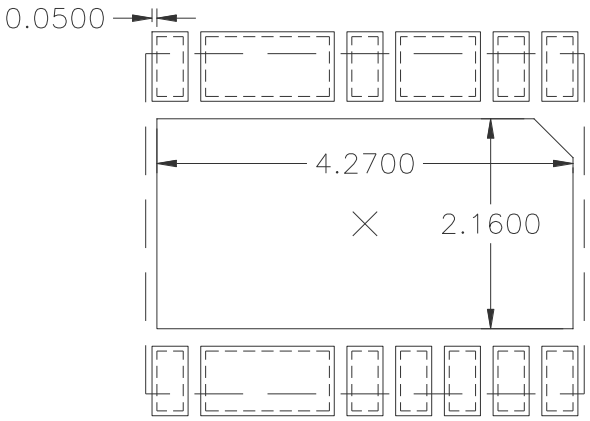
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



Recommended PCB solder mask opening (Top View)



Notes:

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: Passes ≥ 1000V to < 2000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: Passes ≥ 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead-free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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